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INTRODUCTION

ABOUT THIS MANUAL

The Emulator II is a powerful and complex instrument. E-mu Systems, Inc. intends this manual to be an aid to the experienced service technician only. While it will undoubtedly prove interesting to adventurous Emulator II owners, we do not recommend that even the most hardy owner attempt to repair the instrument. Of course, if you are an E II owner AND an experienced service technician, go ahead and enjoy yourself!

To service the Emulator II, you should be familiar with digital logic, the Z-80 family of microprocessor products, and analog electronics. The minimum equipment required to service the instrument is a digital multimeter, a 60 MHz dual channel oscilloscope, and basic service technician hand tools. We also recommend that you have a computer terminal or small portable computer such as a Radio Shack Model 100 to run Debug tests through the RS-232 interface.

The information contained in this manual is proprietary to E-mu Systems, Inc. The entire manual is protected under copyright and none of it may be reproduced by any means without written permission from E-mu. This manual is available only to approved service people and is the property of E-mu Systems. It is best to consider all of the data secret and use it only to service the Emulator II.

We feel obliged to remind you that any modification of an E II other than as specified by a factory authorized Engineering Change Order (ECO) will not only void its warranty, but probably make the instrument more difficult (and therefore more expensive) to service.

Please read this manual thoroughly before attempting to service the Emulator II. If you then feel unsure about working on the instrument at all, please contact our service department.

MANUAL ORGANIZATION

This manual has ten sections:

SECTION 1 is a brief summary of Emulator II operating controls.

SECTION 2 explains how the E II works.

SECTION 3 shows how to find your way around E II.

SECTION 4 outlines procedures for testing E II's operation.

SECTION 5 gives diagnostic tips. (optional)

SECTION 6 contains E II's specifications and E-mu conventions.

SECTION 7 contains the Emulator II schematic diagrams.

SECTION 8 is a place to keep your ECO's.

SECTION 9 is a parts listing.

SECTION 10 is a glossary of technical terms used in this manual.

If you encounter any errors in this manual, or have suggestions that might make it better, please let us know. We are interested in hearing how we might improve the quality of our services to you.

Thanks,
The Emuons

CONTROL SUMMARY

With the exception of brute functions like the power switch and the mix and sample pots, ALL Emulator II controls are interpreted and executed by software. That means these functions can and will vary with software revisions. The software revision level used with the instrument determines which functions are available and their method of operation. This summary is simply a general description of the basic functional intent of each control.

REAR CONTROL PANEL

POWER ON SWITCH

This useful switch is located on the rear of the Emulator II. On early models it is on the end of the instrument furthest from the disk drives. After about serial number 400, both the power supply and its switch are moved next to the disk drives.

VOLTAGE SELECTOR

Before turning an instrument on for the first time, be sure the voltage selector is set correctly for your part of the world. The selector is next to the power on switch. If it was set for another part of the world when it arrived, be sure to reset it before the customer takes it home.

D/A INPUT

The D/A input is for a foot pedal jack. The pot in the pedal is read by the E II Scanner CPU ADC.

FOOT SWITCHES

The Foot Switch inputs are, obviously, for foot switches. The switch in the pedal is read by the E II Scanner CPU through an inverting transistor; when the switch is on, the transistor is off. Foot Switch functions are controlled by software and are selected by the performer.

INTERFACES

The RS-232 interface is available for use during instrument diagnosis. Use a terminal or small computer to talk to E II when running the optional ROM based diagnostics.

MIDI

This interface allows the E II to communicate with other MIDI equipped instruments.

SMPTE

This interface allows E II to be synchronized with film and video equipment.

MIX OUT

This output goes to an amp or mixer.

CHANNEL OUTPUTS

These outputs are for separating the 8 channel outputs. They are always at full level.

MASTER CONTROL BLOCK

DISPLAY

The Emulator II uses the LCD to let you know what it's doing, to remind you of what you are doing or should be doing next, and to ask for information. Its method of prompting you will vary depending upon the function you are using. Most prompts are spelled out on the panel. Some are presented as bar graphs.

KEYPAD

The keypad looks a lot like the pad on your telephone and works similarly. You use it to enter numbers and answer YES or NO to questions put to you by the computer.

SLIDE POTS

These are used to control several different functions. They are read by the SCANNER CPU when appropriate to a function, and their effect on a parameter is displayed on the LCD. Moving them away from you (UP) increases the value of a parameter and moving them towards you (DOWN) decreases it.

MIX OUT VOLUME

This rotary pot is in the feedback loop of the Mix Out amplifier. It controls the mixed output volume of the Emulator II. It doesn't affect the volume of individual channel outputs.

DYNAMIC ALLOCATION

This makes all channels available to all voices, overriding previous keyboard voice assignments.

TUNE

This function allows you to alter keyboard tuning plus or minus 50 cents.

TRANSPOSE

This function allows you to change the key in which a voice is played by the keyboard. The maximum transposition is an octave up or down. If you transpose too far, the octave will wrap around.

DISK/SPECIAL

DISK

As we mentioned before, E II is a software intensive machine. Further, it contains in its Read Only Memory (ROM) only enough software to scan its controls and read a disk. Most of the software E II uses is stored on disk. By itself, E II is musically dumb. This is remedied by using the DISK function to load software and sounds into E II.

SPECIAL

This button allows you to read the catalog of special functions and use them. The catalog scrolls vertically on the display as you move a slider.

SAMPLE

SAMPLE

This control is used to tell E II when to digitize and store a sound sample. Sampling can be triggered manually or by threshold sensing.

GAIN

The sample function allows the performer to select nominal input gain levels. This pot provides an adjustment to set gain more precisely. It is not read by the Scanner CPU. It's a real analog control.

FILTER

This control is used to set filter characteristics such as Q and cut-off, filter keyboard tracking, and filter envelope characteristics for each channel. These parameters are set by moving the sliders as prompted. They can be controlled by keyboard velocity or by the positions of the control wheels or foot pedal, depending upon voice definition.

VCA/LFO

This control sets Voltage Controlled Amplifier envelopes for each channel. It also sets Low Frequency Oscillator rate, delay, variation and modulation depth for the VCA for each channel. These parameters are set by moving the sliders as prompted. They can be controlled by keyboard velocity or by the positions of the control wheels or foot pedal, depending upon voice definition.

VOICE DEFINITION

This controls options that allow a sample's length to be modified. The sample can be truncated, looped, or spliced to another sample, for example. It is also used to define other voice characteristics such as the effect keyboard velocity will have on VCA attack, frequency, filter Q and VCF attack. It assigns voices to channels and sets voice options.

PRESET DEFINITION

This module manipulates voice files and allows them to be assigned to keyboard ranges. You can catalog voices, presets and sequences as well as define MIDI and arpeggiator parameters.

REAL TIME CONTROL

This module assigns performance controls, such as the control wheels, foot switches, etc. to voice functions such as pitch, VCA gain, VCF cutoff and the like.

SEQUENCER

The EII sequencer allows the musican to play the keyboard and have the computer record it. It can be recorded directly or be auto corrected to different resolutions. It has 8 tracks and overdubbing is possible. It will also record the key velocity as well as the wheel, footswitch and footpedal positions. It can be externally clocked by MIDI, a click track or the SMPTE interface.

KEYBOARD

The keyboard has a double contact structure that allows velocity sensing for touch control. The scanner CPU scans the keyboard to see when a key is pressed and determine its velocity. There are procedures for replacing keys and removing the keyboard in section V.

THEORY OF OPERATION

EMULATOR II ARCHITECTURE

The Emulator II is an 8 voice polyphonic digital sampling keyboard instrument. All inputs from the performer are mediated by computer. Sounds are sampled and reproduced digitally, and all voice parameters are storable on digital diskettes. The operation of E II is entirely controlled by computer software.

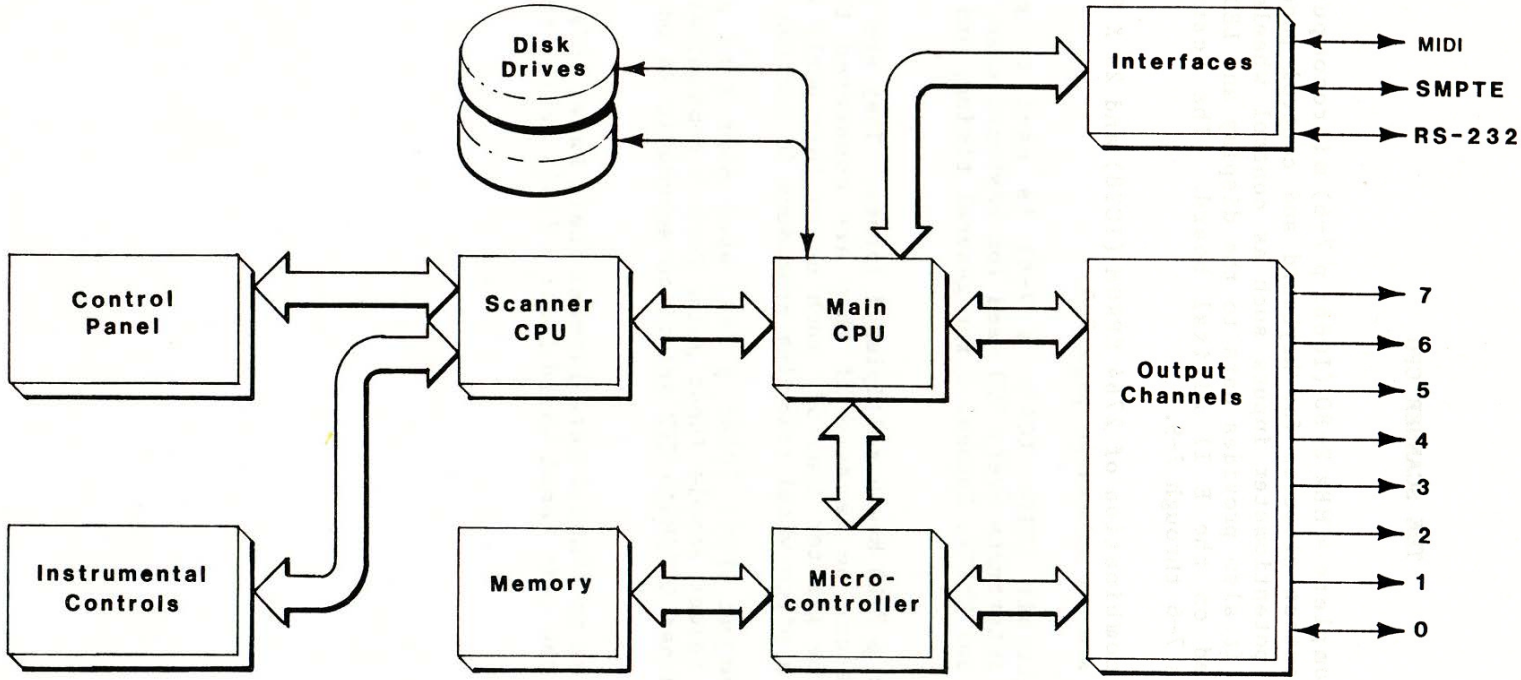
E II contains two microcomputers; the Scanner CPU, and the main CPU. It also contains a microcontroller which controls the addressing of sound memory.

The Scanner CPU mediates all performer input from the control panel and instrumental controls such as the keyboard, foot pedal, foot switches and pitch wheels. All instrumental controls are appropriately programmable as to function. The scanner CPU schematics are on pages 7-6 through 7-9.

The Main CPU handles all machine related input and output including interpreting scanner CPU commands and commands to the channel Microcontroller. It also controls the generation of envelopes and keyboard tracking for VCA and filter functions. MIDI, SMPTE, and RS-232 inputs are handled by the Main CPU. The Main CPU schematics are on pages 7-10 through 7-16.

The Microcontroller sends data to the output channels and controls the Dynamic RAM used for sound reproduction. The Microcontroller schematics are on pages 7-17 through 7-22.

Seven of the eight output channels are identical. Channel 0 has additional circuitry associated with it for the sampling functon of E II. Notice that the channels are numbered from 0 to 7. Musicians will generally count them as 1 through 8. The Output Channel schematics are on pages 7-39 through 7-53.


Disk Drives
Interfaces
MIDI
SMPTE
RS-232
Control Panel
Scanner CPU
Main CPU
Output Channels
7
6
5
4
3
2
1
0
Instrumental Controls
Memory
Micro-controller

THE SCANNER CPU

The Scanner CPU is a complete 4 MHz Z-80 (IC66: p 7-6) microcomputer. It is designed to sense contact closures for keyboard and control panel input and voltage levels for potentiometer inputs such as control wheels, slide pots and foot pedals. It also provides data to the display and LED's. The Scanner CPU is located on the E II Digital board. The Scanner CPU schematics are on pages 7-6 through 7-9.

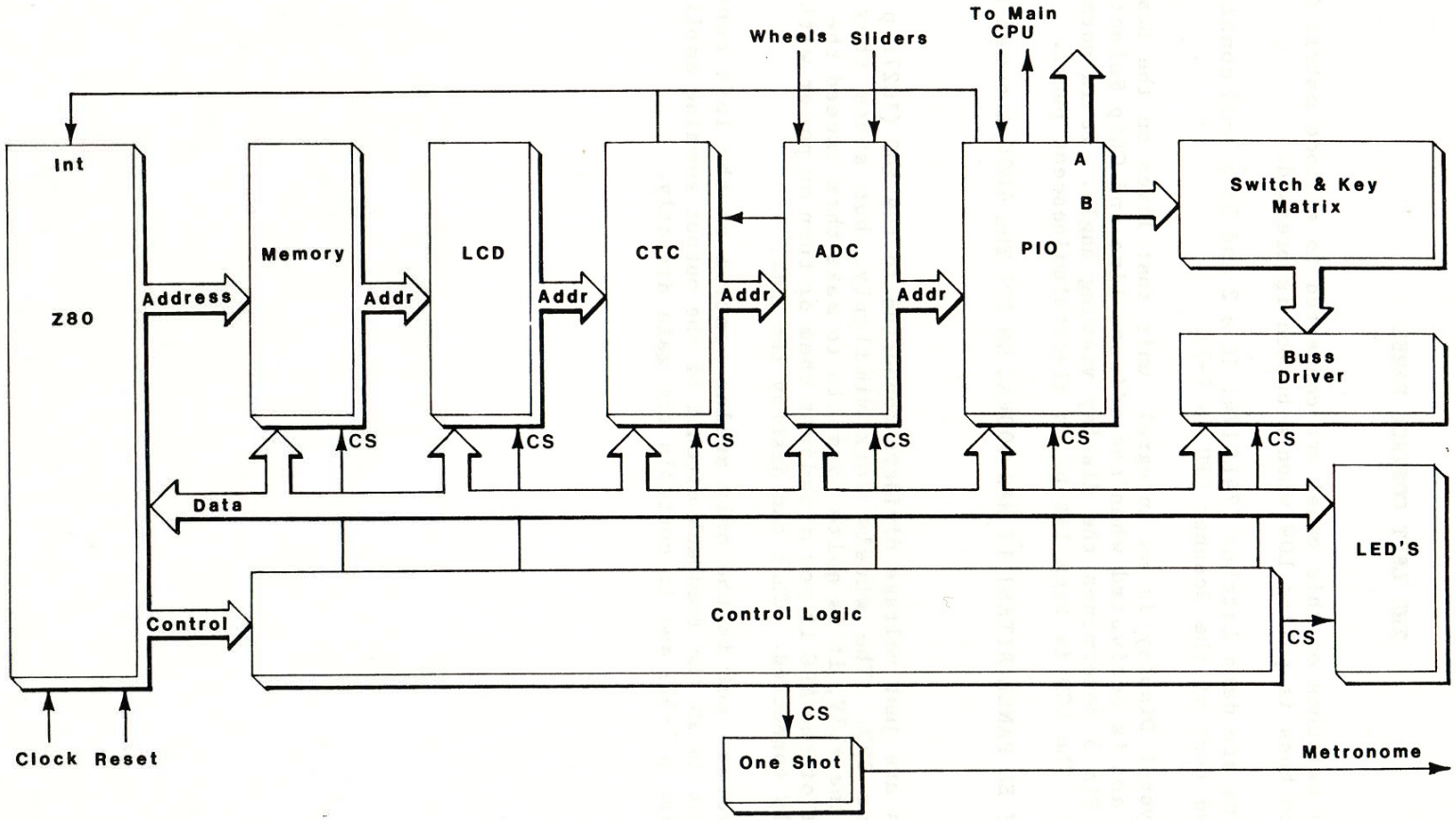
The local memory is a combination of 2764 EPROM (IC28) and 2K X 8 Static RAM (IC29). Both IC's are on schematic page 7-7.

The Counter Timer Circuit (CTC: IC45: p 7-6) is used to generate interrupts. Channel 0 interrupts every 500 used for keyboard scan, Channel 1 for sequencer timing and SMPTE, Channel 2 for general timing, and Channel 3 for ADC interrupts.

The ADC (ADC0809: IC27: p 7-8) has 8 multiplexed inputs. They are software selected. ADC inputs can be damaged if they are connected to a low impedance voltage source greater than 5V, such as an improperly adjusted pitch wheel. There is a pitch wheel trimming procedure in section V.

The Parallel Input/Output (PIO: IC46: p 7-9) uses port B to scan the key/switch matrix and select sample input gain. Port A communicates with the Main CPU. The Scanner CPU/Main CPU interface schematic is on page 7-14.

LED's are lit by writing to 74LS174 data latches (Left Panel IC's 2 and 3: p 7-36). A 74LS273 on the Left Panel board (IC1: p 7-36) drives the Right Panel LED's.


Wheels
Sliders
To Main CPU
Int
Z80
Address
Memory
Addr
LCD
Addr
CTC
Addr
ADC
Addr
PIO
A
B
Switch & Key Matrix
Buss Driver
CS
Data
LED'S
Control
Control Logic
Clock
Reset
One Shot
Metronome

THE LEFT CONTROL PANEL

The pushbutton switches on this panel are connected to a diode matrix (p 7-4). The common buss is pulled LOW when a button is pressed.

The LED drivers are data latches (74LS174: IC's 2 and 3: p 7-3) connected to the buffered buss of the Scanner CPU (p 7-7).

The Liquid Crystal Display is an integral unit that lives on the Scanner CPU data buss and is activated when the address line and Chip Select are valid (LOW). Pin 3 determines the display viewing angle. It is normally at about 0.25V. The LCD is back lit by an electroluminescent panel.

REMEMBER! THE EL PANEL BITES! IT HAS 400VAC ON IT! The 400VAC comes from VR1
(p 7-4).

The slide pots are just voltage dividers connected to the ADC (IC27: p 7-8) on the Scanner CPU. The wheels work similarly, but since they are connected to the +13V, it is quite possible to make them exceed the +5V maximum input of the ADC if you misadjust them or turn on power with the post improperly connected. That can destroy the ADC.

The Mix Out Volume pot is the only analog control on the left control panel. This pot is in the feedback circuit of the output summing amplifier (MC34004P: IC96: p 7-52) and it controls the gain directly.

THE RIGHT CONTROL PANEL

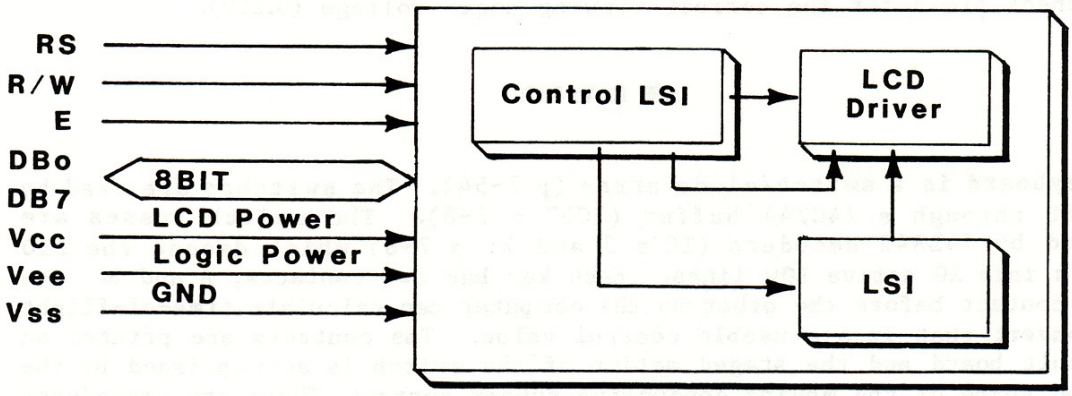
The Right Panel board is simply another diode array connected to pushbutton switches. The switches bring the common buss LOW (p 7-2). This would be the dullest board in the instrument except that it has the other analog control on it. The Sample Gain pot is connected to the sample input amplifier (S3528: IC86: p 7-42) controlling its gain trim.

THE DISPLAY (LCD)

The LCD is a single functional unit. If it gets sick, replace it, do not repair it. The functional diagram shows how it works. If it's hard to see, check pin 3 for the correct viewing angle voltage (0.25V).

THE KEYBOARD

The keyboard is a switch/diode array (p 7-54). The switches are read by the CPU through a 74C244 buffer (IC5" p 7-8). The switch busses are scanned by 74LS42 decoders (IC's 3 and 4: p 7-8) which decode the PIO outputs into 20 active LOW lines. Each key has two contacts, A and B. One makes contact before the other so the computer can calculate time-of-flight and convert that into a usable control value. The contacts are printed on a circuit board and the staged action of the switch is accomplished by the moulded shape of the moving conductive rubber contact. There are procedures for replacing keys and removing the keyboard in section V.



DBo-7 : Data BUS Lines
E : Enable
R/W : Read/Write
RS : Resistor Select

THE MAIN CPU

The Main CPU is a complete 4MHz Z-80 (IC21: p 7-10) microcomputer designed to handle disk operations, I/O, microcontroller commands, envelopes to sound channels, sampling and LFO functions. It lives on the Digital Board. Its memory consists of EPROM (2764: IC42: p 7-12), RAM (2K X 8: IC 59: P 7-12), and the low segment of Dynamic RAM (DRAM).

The CTC (IC80: p 7-13) generates interrupts to the Z-80. Channel 0 provides timing for the floppy disks. Channel 1 provides the interrupt vector for the USART (2651: IC107: p 7-16), and Channel 3 provides a housekeeping interrupt every 10 msec. Channel 2 is unused.

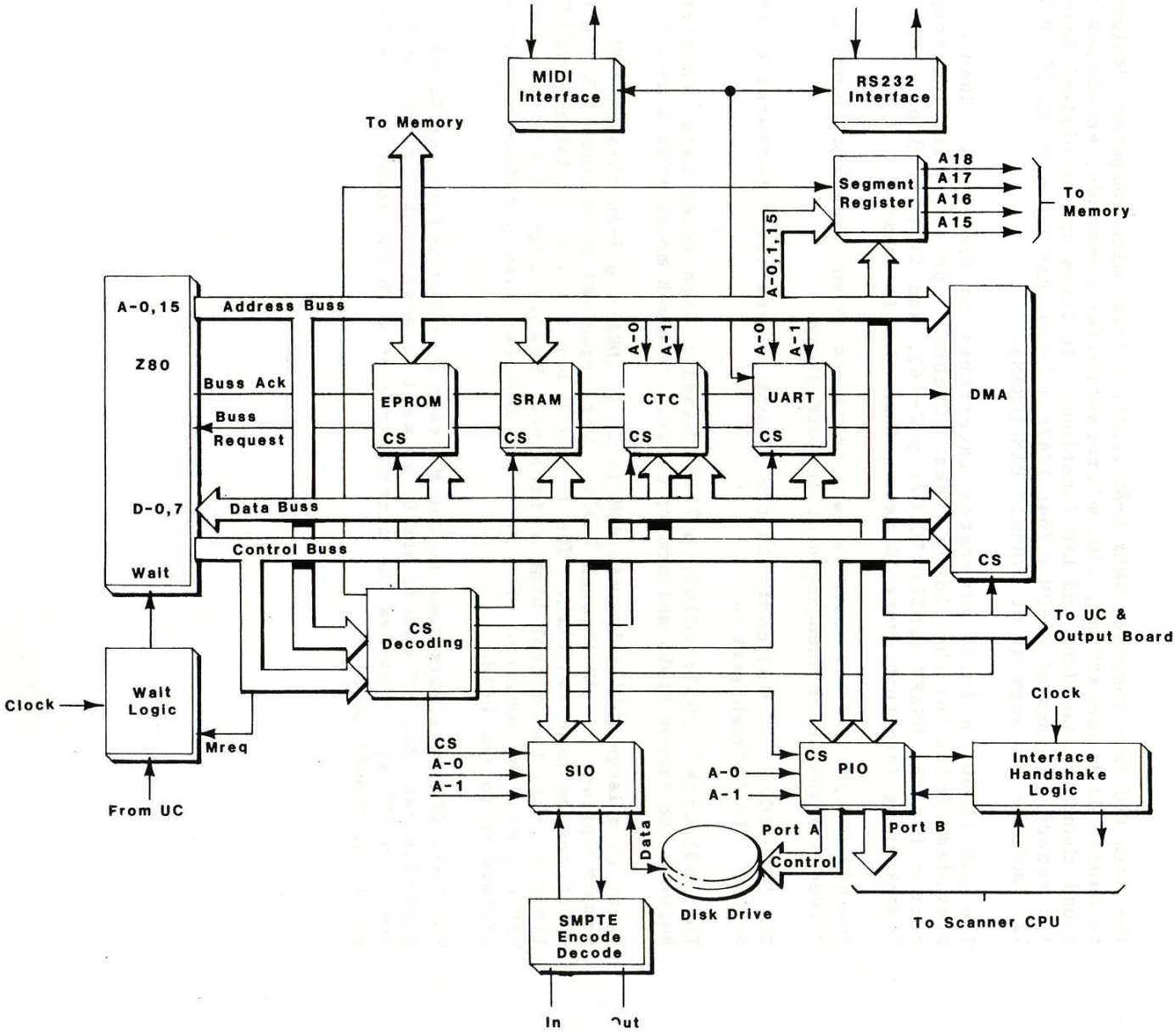
The SIO (IC128: p 7-15) controls data transfers to and from the floppy disk drives and the SMPTE encoding/decoding circuitry.

The PIO (IC24: p 7-14) controls the floppy drives and interfaces to the Scanner CPU through port A.

The 2651 USART (2651: IC107: p 7-16) handles high speed data transfers between the floppy disks and memory as well as block moves within memory.

There is a large (512K) dynamic RAM in E II. (DRAM: p 7-26 through 7-29 and Memory Option: p 7-32 through 7-37). It's organized as sixteen 32K blocks which can be bank switched. The Main CPU has a select register (74LS670: IC64: p 7-11) to control bank switching. Memory segment 0 is the Main CPU's operating memory. The Main CPU Address Buss provides low order addressing to the DRAM.

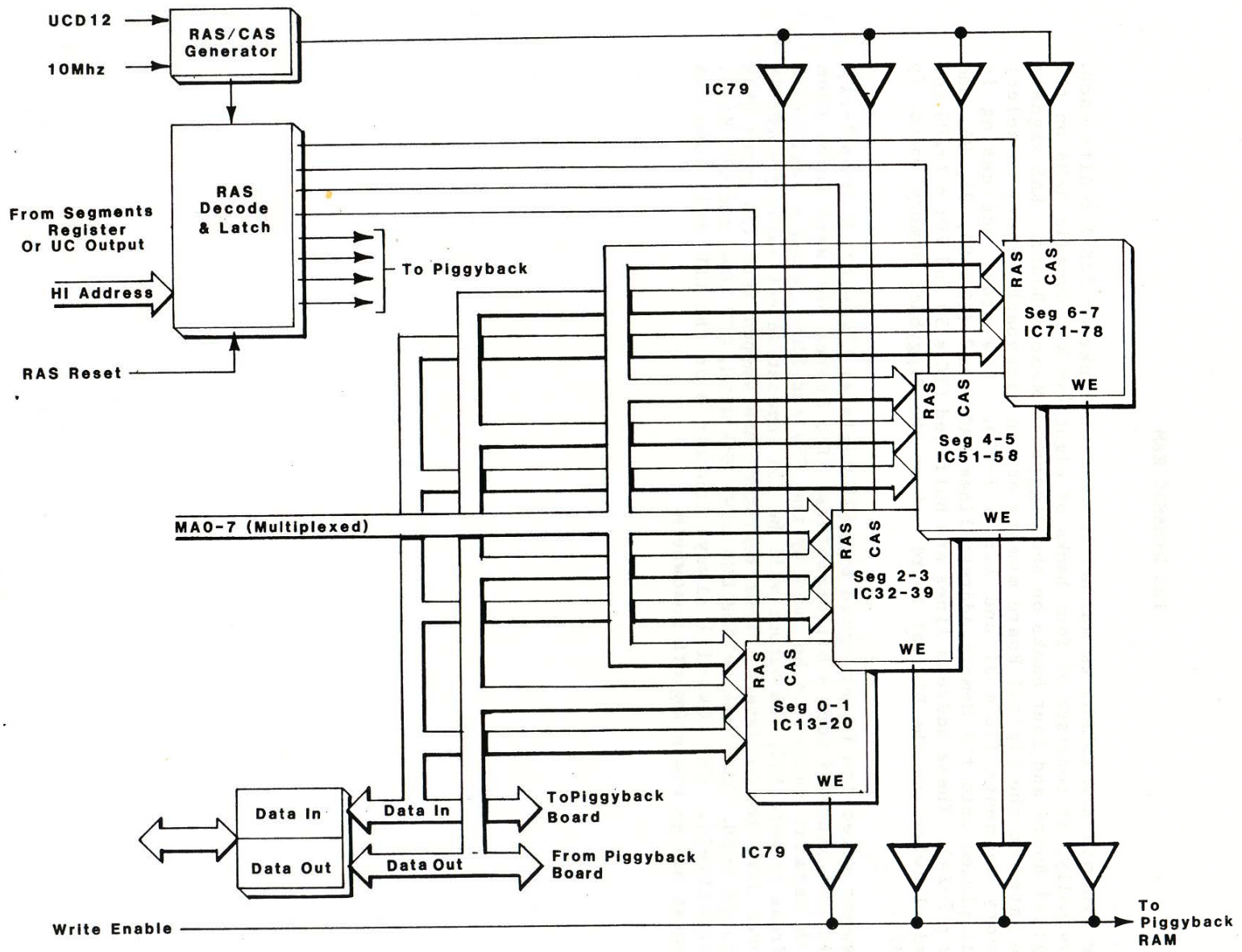
The Main CPU Data buss goes to the Microcontroller and Output Board. It provides data for VCF cutoff and Q, as well as envelopes for VCF and VCA. The Main CPU also provides the microcontroller with the locations and loop points of sounds in DRAM.


MIDI Interface
RS232 Interface
To Memory
Segment Register
A18
A17
A16
A15
To Memory
A-0,1,15
A-0,15
Z80
Address Buss
Buss Ack
Buss Request
D-0,7
Data Buss
Control Buss
Wait
EPROM
CS
SRAM
CS
CTC
CS
UART
CS
A-0
A-1
DMA
CS
To UC & Output Board
CS Decoding
Clock
Wait Logic
Mreq
From UC
CS
A-0
A-1
SIO
A-0
A-1
CS
PIO
Clock
Interface Handshake Logic
Data
Port A
Control
Port B
Disk Drive
To Scanner CPU
SMPTE Encode Decode
In
Out

THE DYNAMIC RAM

The Dynamic RAM (DRAM) is mapped as sixteen banks of 32K X 8 Bits each. Physically, it consists of four banks of eight 64K X 1 dynamic RAMs on the Digital Board and four banks on the Piggyback Memory Board. RAS signals are gated to the Digital Board memory or the Piggyback memory to select memory segments (IC's 31 and 12: p 7-23). Low order addressing is multiplexed onto the Memory Address lines MA0 - MA7 (IC's 94, 95, 96, and 69: p 7-24). These address lines are buffered (IC's 50 and 70: p 7-20) and used elsewhere on the Digital Board and on the Piggyback Memory Board. (p 7-32).

Segment selection is performed by a 4X4 register (74LS670: IC64: p 7-11). This is a block of four 4 Bit registers. The System software loads them with segment values to be used by the CPU and DMA. When a register's address is selected, its output will be the segment select value previously stored into the register. These registers are mapped into I/O ports 068H through 06BH. They are called DMA LOW, DMA HIGH, CPU LOW, and CPU HIGH, respectively. CPU LOW will always contain 0 or the CPU will lose its program and go wandering off somewhere.


UCD12
10Mhz
RAS/CAS Generator
IC79
RAS Decode & Latch
From Segments Register Or UC Output
HI Address
RAS Reset
To Piggyback
RAS
CAS
Seg 6-7 IC71-78
WE
Seg 4-5 IC51-58
Seg 2-3 IC32-39
Seg 0-1 IC13-20
MA0-7 (Multiplexed)
Data In
Data Out
Data In
Data Out
ToPiggyback Board
From Piggyback Board
IC79
Write Enable
To Piggyback RAM

THE PIGGYBACK RAM

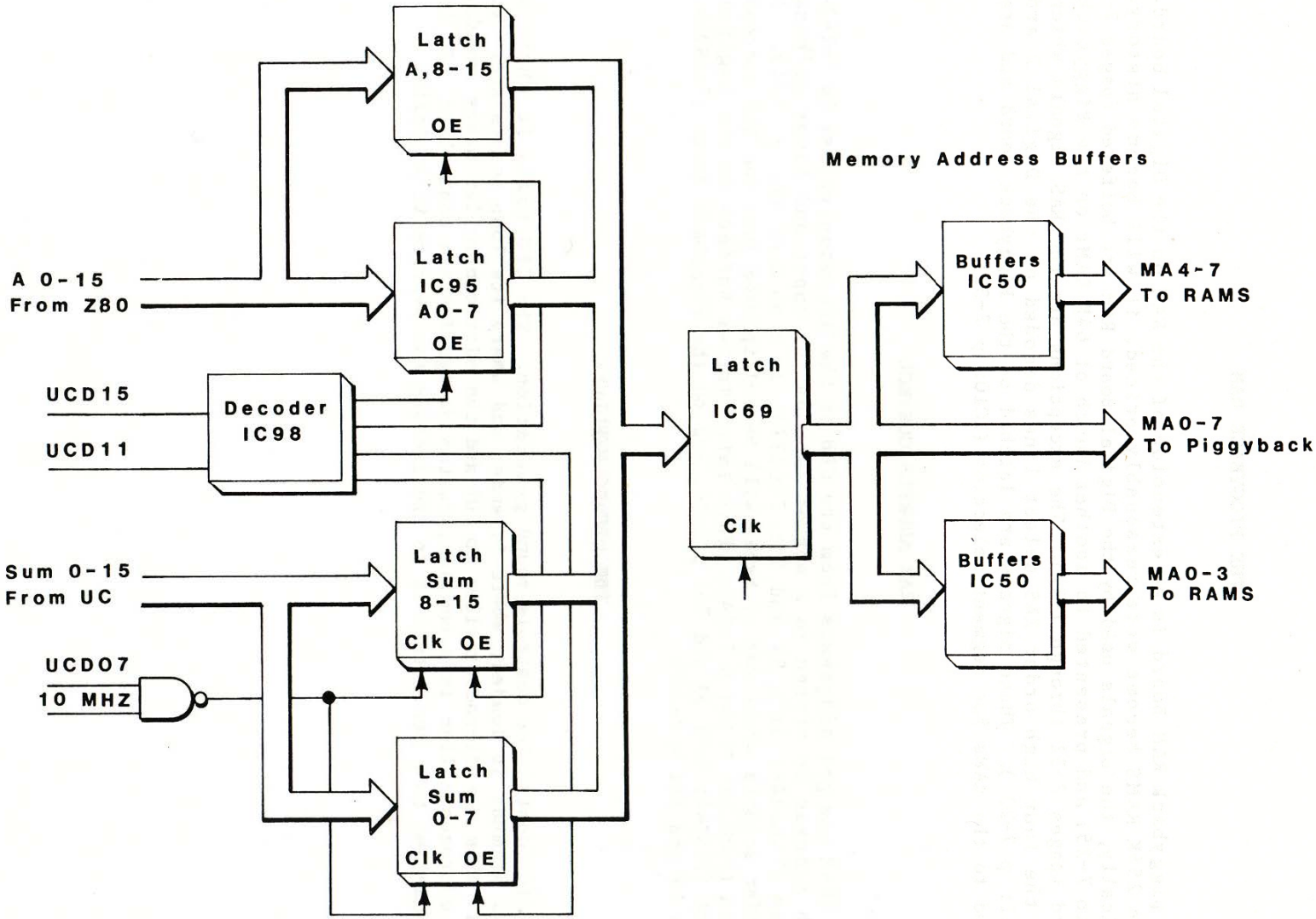
The piggyback RAM Board is an extension of the RAM on the Digital board. When 256K RAMS become more reasonably priced, it will become history. Basically, the signals used by the Digital Board RAM are buffered (pages 7-23 to 7-25) and presented to another bunch of 64K RAMs on the Piggyback Board (pages 7-32 through 7-37). The exceptions are the RAS signals which are the four high order RAS select lines decoded on the Digital Board (IC11: p 7-23). These signals are latched on the Piggyback Board and are gated to the RAMs for segment selection (IC10: p 7-32).

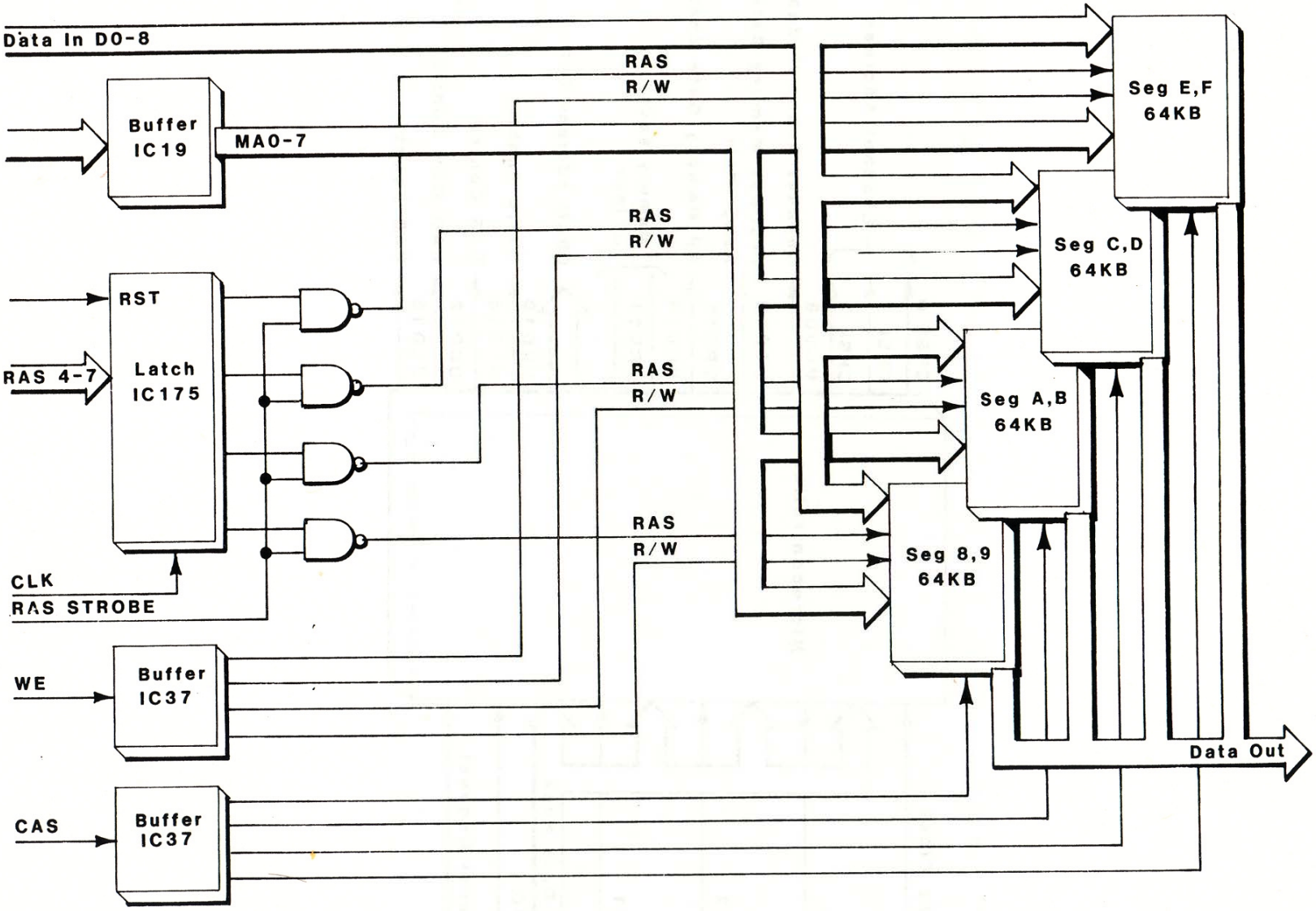
RAM ADDRESS CONTROL

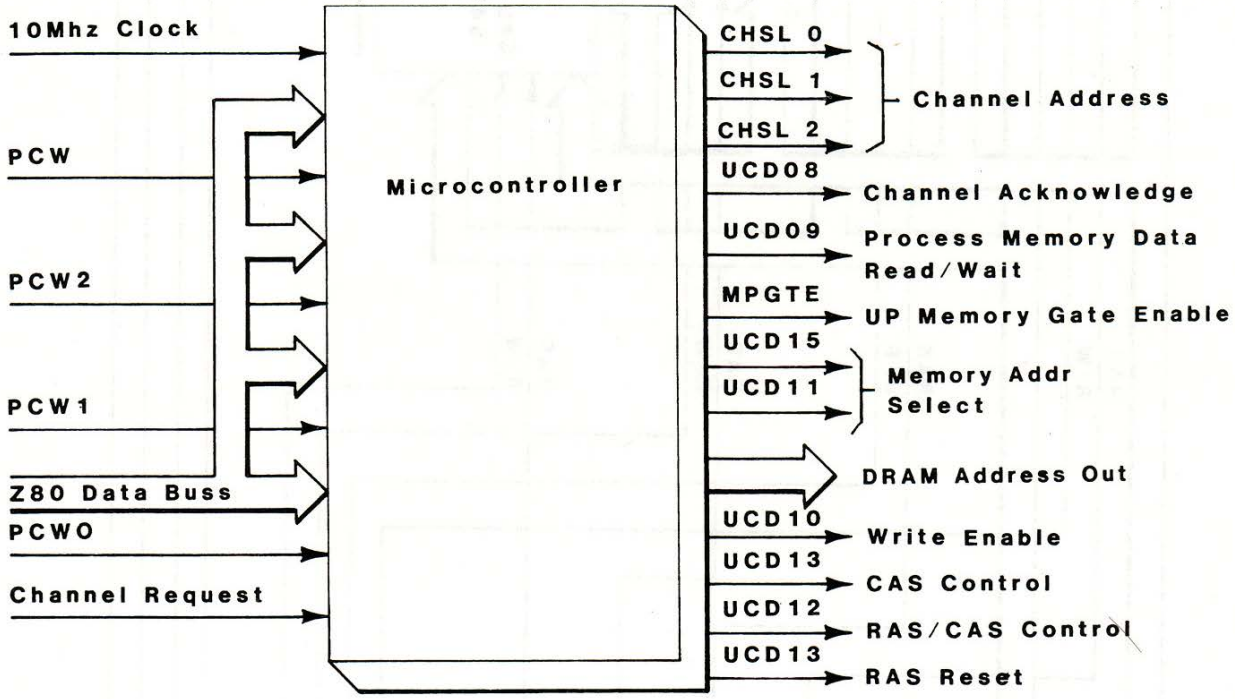
The DRAM can get addresses from the CPU or the Microcontroller (p 7-24). Each address is stored in a set of latches for upper and lower address bytes (74LS244: IC's 94 and 95: 74LS374: IC's 96 and 97: p 7-24). A decoder selects which set of bytes will be multiplexed into the RAM address latch (74S138: IC96: p 7-24). This latch drives buffers on the Digital Board (74S244: IC's 50 and 70: p 7-24) and on the Piggyback Board (74LS244: IC's 19 and 28: p 7-32).

THE MICROCONTROLLER

The microcontroller controls sound generation. The CPU tells it where a sound segment is loaded, where it ends, and where its loop points are. It then tells the Microcontroller to GO! and the Microcontroller makes sounds. The microcontroller is a complex, custom designed state controller. It is recommended that you return it to the factory for service if it fails.


Latch
A,8-15
OE
Memory Address Buffers
A 0-15
From Z80
Latch
IC95
A0-7
OE
Buffers
IC50
MA4-7
To RAMS
UCD15
UCD11
Decoder
IC98
Latch
IC69
Clk
MA0-7
To Piggyback
Sum 0-15
From UC
Latch
Sum
8-15
Clk OE
Buffers
IC50
MA0-3
To RAMS
UCDO7
10 MHZ
Latch
Sum
0-7
Clk OE


Data In D0-8
Buffer
IC19
MA0-7
RAS
R/W
RAS
R/W
RAS
R/W
RAS
R/W
RST
Latch
IC175
RAS 4-7
CLK
RAS STROBE
WE
Buffer
IC37
CAS
Buffer
IC37
Seg E,F
64KB
Seg C,D
64KB
Seg A,B
64KB
Seg 8,9
64KB
Data Out

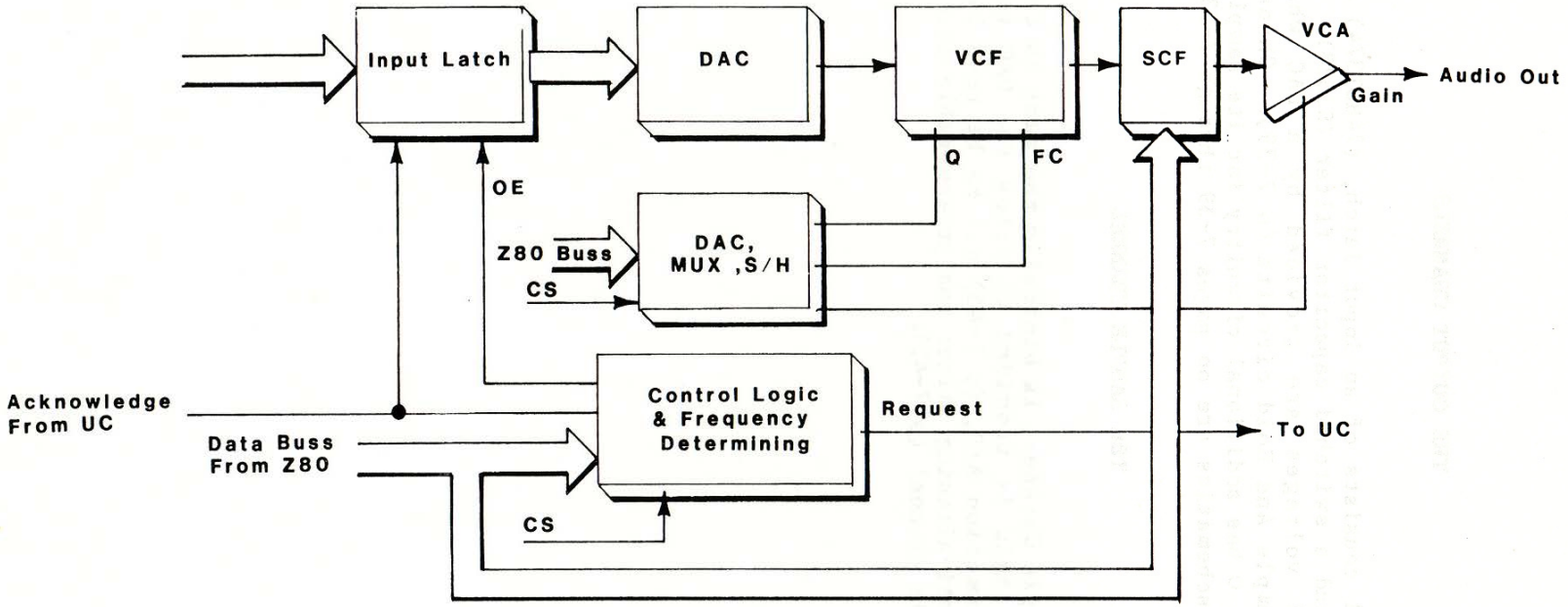

10Mhz Clock
PCW
PCW2
PCW1
Z80 Data Buss
PCWO
Channel Request
Microcontroller
CHSL 0
CHSL 1
CHSL 2
Channel Address
UCD08
Channel Acknowledge
UCD09
Process Memory Data Read/Wait
MPGTE
UP Memory Gate Enable
UCD15
UCD11
Memory Addr Select
DRAM Address Out
UCD10
Write Enable
UCD13
CAS Control
UCD12
RAS/CAS Control
UCD13
RAS Reset

THE OUTPUT CHANNELS

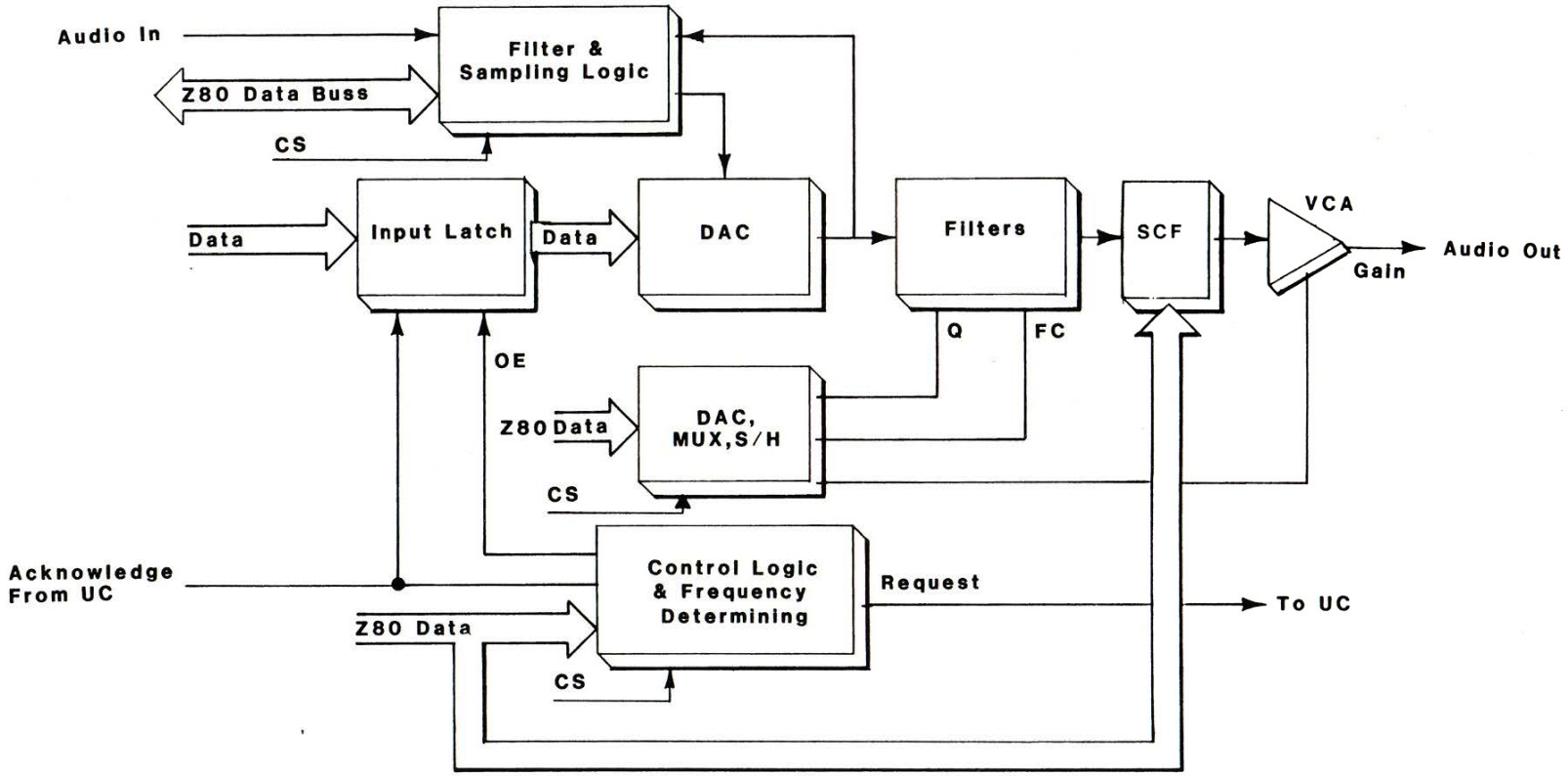
Each output channel consists of an input latch, (74HCT374) a DAC, (6072) a VCF/VCA (SSM2045) and a switched capacitor filter (S3528). The filter and amplifier control voltages are provided by a DAC whose output is multiplexed to Sample And Hold circuits (p 7-39). Channels 1 - 7 are identical. Channel 0 has additional circuitry for its sampling function (p 7-44). The output schematics are on pages 7-39 through 7-53.

THE SAMPLE CHANNEL

Channel 0, the Sample Channel, is basically the same as the other output channels. Extra logic is provided to allow the DAC to be used as a successive approximation A/D, (p 7-43) and to be read back by the CPU. There is also an anti-aliasing filter and programmable gain control in the analog input to this channel (p 7-42).



OUTPUT CHANNELS 1-7


Audio In
Filter &
Sampling Logic
Z80 Data Buss
CS
Data
Input Latch
Data
DAC
Filters
SCF
VCA
Audio Out
Gain
Q
FC
OE
Z80 Data
DAC,
MUX,S/H
CS
Acknowledge
From UC
Control Logic
& Frequency
Determining
Request
To UC
Z80 Data
CS

MECHANICAL PROCEDURES

THE SERVICING POSITION

Rest the instrument on its back panel.

Remove the bottom panel screws.

Remove the rear panel screws. If you intend to remove the printed circuit boards, remove the nuts from the jacks as well as the screws on the RS-232 connector.

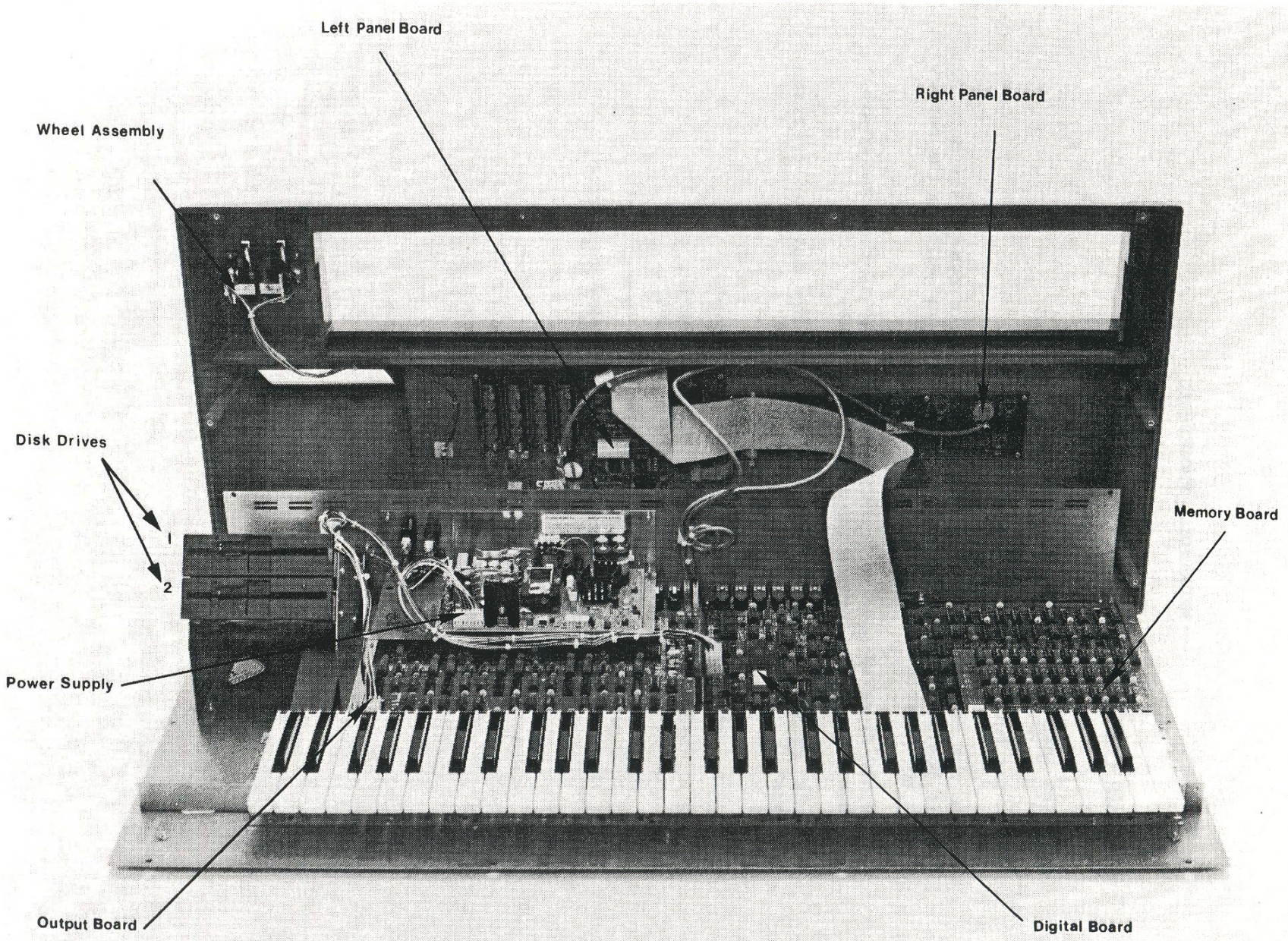
Facing the front of the instrument, lift the rear of the housing about 3 inches and pull it towards you until it is free.

Set the housing behind the instrument facing upwards (service position).

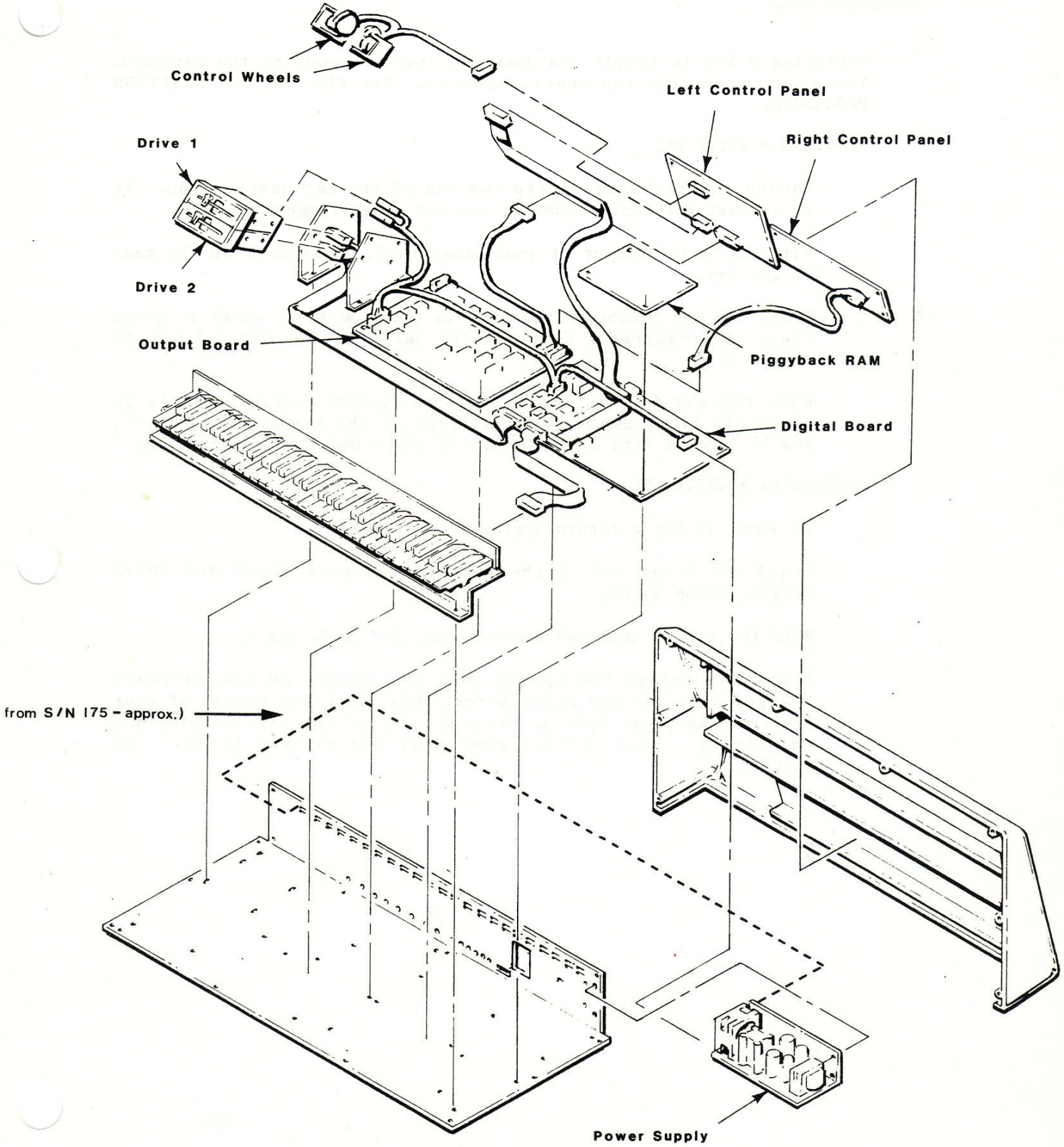
CAUTION!!

THE HOUSING IS SLIGHTLY UNSTABLE IN THIS POSITION AND CAN BE KNOCKED OVER EASILY!

Replace the housing by reversing the procedure above.



EMULATOR SERVICE POSITION


Control Wheels
Left Control Panel
Right Control Panel
Drive 1
Drive 2
Output Board
Piggyback RAM
Digital Board
from S/N 175 - approx.)
Power Supply

REPLACING KEYS

Replacing a key is simple and does not require removing the keyboard. You must remove the top cover, however. See the SERVICE POSITION PROCEDURE.

REMOVING A WHITE KEY

Facing the keyboard, grasp the end of the key nearest you. It is easiest with your thumb on top and index finger beneath.

With the index finger of your other hand, press down on the rear of the key.

Twist the key slightly from side to side, pulling, until it comes free. It requires a fairly hefty pull, but be careful not to overdo it.

When the key is out, check that its return spring is still in place (It lives under the small end of the key). If it isn't, you'll have to find it. It usually hides under an adjacent key.

INSTALLING A WHITE KEY

Be sure the key's return spring is in place.

Grasp the large end of the key between your thumb and index finger, thumb on top.

Hold the key at about 45 degrees with the small end up.

Place the end of the spring into the dimple on the keyboard bracket near the key pivot point. Use the index finger of your free hand to press down on the small end of the key, compressing the spring. Push the key away from you to seat it into the bracket.

REMOVING A BLACK KEY

Before a black key can be removed, the adjacent white keys must be removed. Follow the procedure for removing a white key.

Remove the black key in the same manner as the white ones.

INSTALLING A BLACK KEY

Grasp the key by the end opposite the spring, holding it between your thumb and index finger.

Hold the key at about 45 degrees with the spring end up.

Place the end of the spring into the dimple on the keyboard bracket near the key pivot point. Use the index finger of your free hand to press down on the small end of the key, compressing the spring. Push the key away from you to seat it into the bracket.

Install the adjacent white keys.

REMOVING THE CONTROL WHEELS

Place the instrument in the Service Position. See the SERVICE POSITION PROCEDURE.

Unplug the Molex connector from the Right Panel Board.

Cut the two cable ties.

Remove the 4 mounting screws.

The pots will come out along with the mounting bracket.

CAUTION!!

IF YOU REPLACE A POT, YOU MUST READJUST IT BEFORE APPLYING POWER TO THE INSTRUMENT OR THE SCANNER CPU ADC MAY BE DESTROYED! SEE THE CONTROL WHEEL TRIMMING PROCEDURE!

REMOVING THE CONTROL PANEL CIRCUIT BOARDS

Place the instrument in the Service Position. See the SERVICE POSITION PROCEDURE.

REMOVING THE RIGHT PANEL BOARD

Remove the Sample knob. It pulls off.

Disconnect the 16 pin ribbon cable.

Disconnect the audio cable from the Output Board.

Remove the 8 mounting screws.

The board can be removed.

Reinstall the board by reversing the procedure above.

REMOVING THE LEFT PANEL BOARD

Remove the slider knobs and the Mix Out knob. They pull off.

Disconnect the 16 pin ribbon cable.

Disconnect the 50 pin ribbon cable.

Disconnect the audio cable.

Disconnect the control wheel cable.

Remove the 6 mounting screws.

The board can be removed.

To reinstall the board, reverse the procedure above.

REMOVING THE MAIN PRINTED CIRCUIT BOARDS

SERVICE NOTE:

The two main PCB's must be removed together. On later production instruments, take off the power supply bracket first, which is on the left.

Disconnect the DC power cables from both boards.

Disconnect the 3 ribbon cables from the Digital Board.

Disconnect the 2 audio cables from the Output Board.

Remove the Piggyback Memory Board.

Remove the 5 mounting screws from the Output Board.

Remove the 6 mounting screws from the Digital Board.

SERVICE NOTE:

The NYLON SCREW must be used in its position next to the POWER CONNECTOR.

Grasp the boards as a single unit, placing a hand on each side, near the keyboard.

Lift the boards about an inch and pull until the jacks clear the rear panel.

Lift the boards until they clear the keyboard and pull them towards you. Be careful that the boards don't drag on the keyboard.

CAUTION!!

DRAGGING THE BOTTOM OF THE BOARDS ACROSS THE KEYBOARD CAN BREAK THE WIRES SOLDERED THERE AS WELL AS SCRATCH THE KEYBOARD. IF THE INSTRUMENT QUITS WORKING AFTER THIS PROCEDURE IT IS LIKELY THAT YOU HAVE BROKEN ONE OF THE WIRES ON THE BOTTOM OF A BOARD.

FIGURE # 1

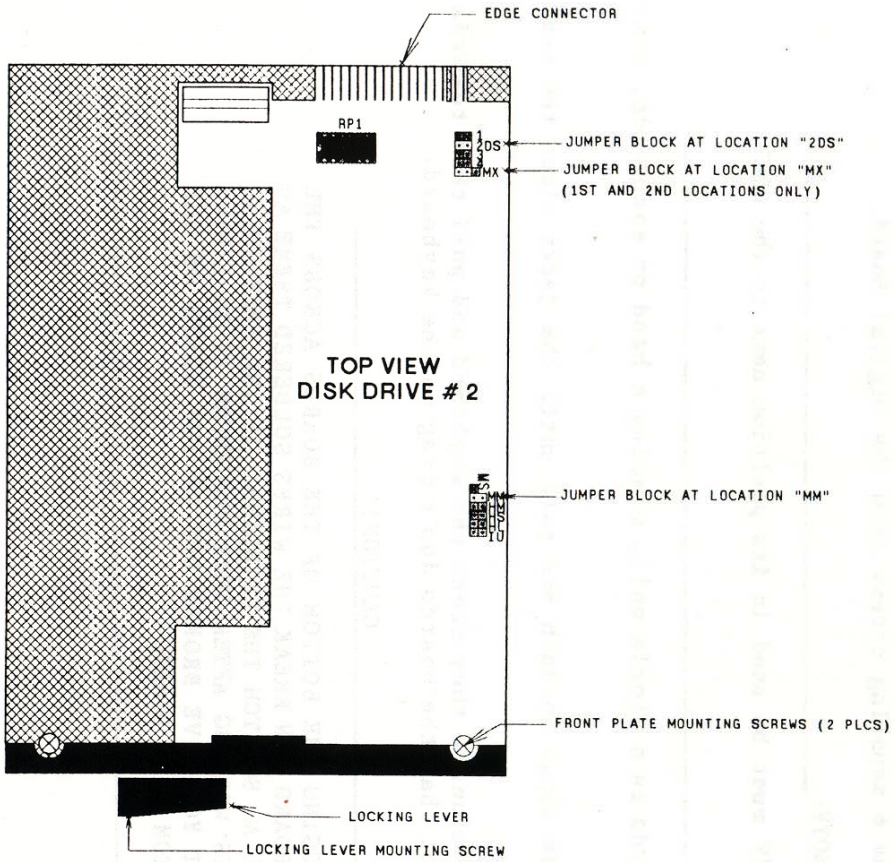


FIGURE # 2

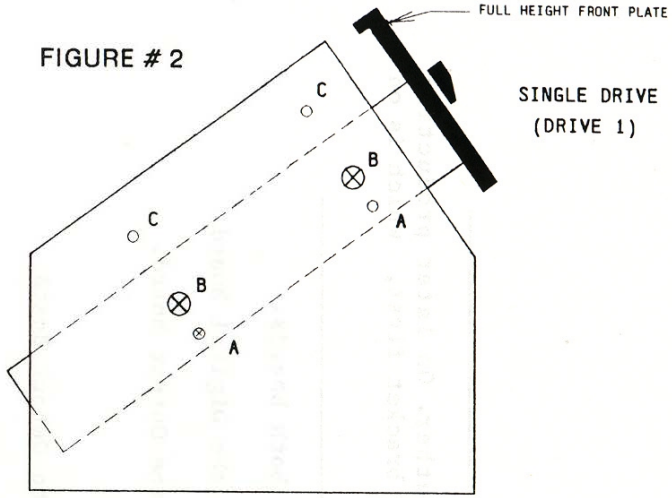
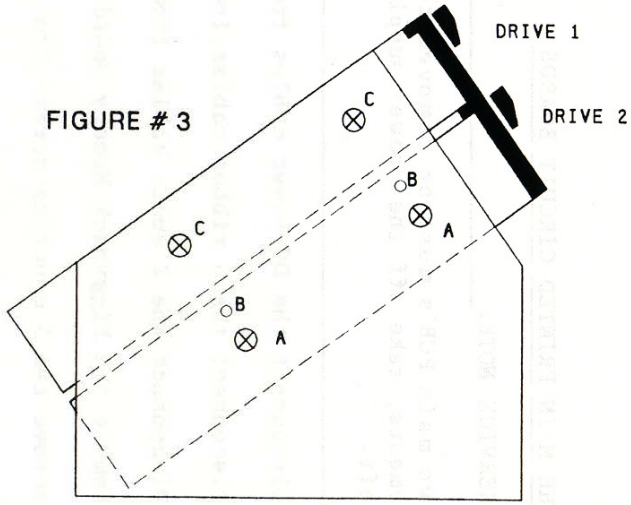


FIGURE # 3



E-mu Systems, Inc. "applied magic for the arts"		
EMULATOR 2 DUAL DRIVE RETROFIT DIAGRAM		
A SIZE SCALE = .5	REV B	DATE 850207
DOC. # A-6186-015	3-8	DRAWN BY: B.H.M.

REPLACING THE MAIN PC BOARDS

The boards must be joined at the mating connector and treated as a single unit during installation.

Hold the boards so that you are supporting the middle of the front of the Output Board, instead of its side.

Angle the board so that the jacks on the output board enter their holes first.

Reinstall the boards by reversing the removal procedure. Use only two mounting screws at the front center of each board to hold them in place temporarily.

Before installing the rest of the mounting screws, be sure the instrument works properly. If it doesn't, it is likely that a wire has been broken on the bottom of one of the boards.

Reinstall the mounting screws and replace the cover.

REMOVING THE DISK DRIVES

Place the instrument in the Service Position. See SERVICE POSITION PROCEDURE.

SERVICE NOTE:

The top disk drive (Drive One) must be removed before you can remove the lower one (Drive Two).

Disconnect the power and signal cables from the Disk Drive.

Remove the 4 mounting screws.

Slide the drive out of its mounting brackets.

To reinstall the drives, reverse the procedure above.

SERVICE NOTE:

The two disk drives are NOT identical. See the illustrations for differences in jumper positions, and the terminating resistor pack on Drive One. The instrument will not work if the drives are not configured as shown.

TRIMMING PROCEDURES

There are only 3 physical trimmers in the Emulator II. Two of these are for adjusting the left and right wheels. The 3rd is for adjusting the sample input offset.

There are two procedures for adjusting the wheel trims. The first procedure should be used when one of the wheels is out of calibration. The second procedure is only necessary if a wheel pot has been replaced.

WHEEL TRIM

PROCEDURE #1

This problem normally manifests itself as a pitch offset when the left wheel is selected in the Real Time Control Module.

To Test: Select Real Time Control Module, then alternately press 1:1, 1:0 while playing a key. Any pitch variation probably indicates an uncalibrated left wheel.

To Calibrate: First check the left wheel pot to see that it is tightly secured to the mounting bracket. This is the most common failure mode. If the pot is loose, simply rotate the pot until it passes the 1:1, 1:0 test described earlier. Then tighten. Removing the bracket from the housing will make this easier.

If the pot is not loose, refer to the Wheel Trim Procedure listed under Scanner Test in the Final Test Procedure of this manual.

INITIAL WHEEL TRIM PROCEDURE #2

SERVICE NOTE:

This procedure is necessary only when the control wheel pots are replaced.

Final trim is done using the Scanner Diagnositc Disk, which is part of the Final Test procedure.

CAUTION!!

IMPROPER TRIMMING OF THE CONTROL WHEELS CAN CAUSE THE SCANNER CPU A/D TO BE DESTROYED! THE POTS MUST BE PREADJUSTED BEFORE INSTALLING THEM TO PREVENT A/D DAMAGE!

TOOLS REQUIRED:

DIGITAL MULTIMETER	1/16" HEX WRENCH
SMALL SCREWDRIVER	RULER OR SPACER

SERVICE NOTE:
Use an Emulator I or Prophet V solid plastic pitch/mod wheel to make a spacer. Cut a pie-shaped segment from it so it will fit over the pot shaft between the wheel and bracket to set clearance.

RIGHT WHEEL TRIM

Set the meter to low resistance range.

Connect to the blue and green wires.

Holding the wheel as it would be mounted in the instrument, rotate the wheel to minimum position.

The resistance should be between 50 and 150 Ohms.

If the resistance is out of this range, calibrate the pot as follows:

Install the spacer, or measure the gap between the bracket and the wheel. It should be 1/4".

Tighten the hex screw just enough to keep the wheel and pot rotating together, but loose enough to allow them to slip for adjustment.

Position the wheel as it would be in the machine.

Turn the wheel towards you until it hits the bracket. This is the zero setting.

Holding the wheel and bracket as one unit, turn the pot shaft with the screwdriver until the resistance is 100 Ohms.

Turn the wheel far enough to gain access to the hex screw hole and tighten the screw.

Turn the wheel to the zero position. If the resistance is not between 50 and 150 Ohms, repeat the calibration procedure.

LEFT WHEEL TRIM

Remove the spring.

Connect the meter to the violet and green wires.

SERVICE NOTE:
The right wheel hex screw is accessible throughout the procedure, so you can tighten the screw immediately after calibration.

Follow the same procedure as for the right wheel to calibrate the pot.

SAMPLE OFFSET TRIM

This trim procedure is performed to eliminate clicks and thumps during sampling. It is done by measuring the difference between a sampled voltage and its playback value and adjusting the difference to less than ten millivolts.

TOOLS REQUIRED:

Digital Voltmeter
Small Blade Screwdriver

PROCEDURE:

1. Place the instrument in the Service Position (See Section 4).
2. Connect the Voltmeter ground (black lead) to the exposed metal of the Audio Output jack.
3. Make sure nothing is plugged into the Sample Input jack.
4. Power up the instrument with a regular disk.
5. Erase all the memory by pressing the following buttons in order:

   Preset Definition
   1
   6
   YES
   YES

6. Press the Sample button twice to load the Sample software from disk and return to normal.
7. Locate the trimmer and test point on the output PCB, near the middle of the instrument. The trimmer (RT1) is near the right edge of the board just above the connectors. The test point is on IC 75 pin 1, just to the left and above RT1.
8. Set the meter to the millivolt range.
9. Measure the voltage at the test point (IC 75-1).

10. Press the Sample button on the front panel. Measure the new voltage at the test point. If the voltage difference is greater than 10 mv. then make the following adjustment:

11. Adjust RT1 a small amount (1/8 turn) and measure the voltage at the test point.

12. Press Sample twice and note the difference in readings.

13. Repeat steps 11 and 12 until the difference is less than 10 mv.

FINAL TEST

The following is a list of the funcitons that must be tested on the Emulator II. They are divided into three sections.

1. Scanner tests

2. Listening tests

3. Misc. tests

I have purposely started with scanner funtions as they are easy to test using the scanner diagnostic disk and should be done first to verify buttons, keys and etc. all work ok. This will be impossible if the disk won't load but I am going to assume at this stage of the test the machine will do this. I will begin with a short tutorial on the scanner dianogistic disk then proceed on to the tests.

SCANNER DIAGNOSTIC DISK TESTS

When the disk is first booted, which happens rather quickly compared to a normal E II boot, the display will look like this:

```
| K#  v  f001  r |
| cd  a  b  c  d |
------------------
```

The display is ready to show the results of several of the scanner CPU's functions. They are listed below for your convenience.

All the following numbers will be hexadecimal.

K#----Number of last key pressed. Range is 00 to 3C

v-----Velocity of the key being pressed. Range is 0 to F

f----Digitized value of foot pedal. Range is 00 to 7F

r----Digitized value of right wheel. Range 00 to 7F

l----Digitized value of left wheel. Range 00 to 7F

cd----This will change according to what you are testing. If a front panel button is pressed then it will display "ppxx." The "pp" means that a button is being pressed and held. The "xx" denotes the button number. Range is 00 thru 1F (See last page for actual assignments). When the button is released the display changes to "rpxx." The footswitches are also displayed on this test.

When a key is released the display changes to "krxx" to indicate that key number "xx" was released. This is used in conjunction with the K# function above. The v directly after the K# displays the velocity value of the key pressed.

a----Digitized value of slider A. Range 00 to 7F

b----Digitized value of slider B. Range 00 to 7F

c----Digitized value of slider C. Range 00 to 7F

d----Digitized value of slider D. Range 00 to 7F

Notice that when the disk is first booted there are blanks after the function designators. The spaces will be filled in as those functions are used. As an example move slider A just after booting. The "a" will then show the value of slider A only without affecting the rest of the display.

The LED's are toggled on and off by their respective buttons and are tested in conjunction with the button.

When any button that does not have a LED for it is pressed the metronome output on the rear panel will beep.

SCANNER TEST LIST

1. All keys on the keyboard. Check for press, release and velocity.

2. All front panel buttons. Check for press, release and bounce or any kind of flakey triggering.

3. All LED's. They light when their function button is presed.

4. The four sliders. Do they go 00 to 7F? When wiggled does the value change?

5. Left and Right wheels. Do they go 07 or less, to 78 or greater? The wheels must be trimmed using the trimmers located on the left and right panel boards.

   Left wheel trimmer RT7
   Right wheel trimmer RT6

   The left wheel, which is spring loaded, must be trimmed to 40 when in the center. The right wheel should be trimmed at the maximum setting. Trim to 7E or as high as possible not to exceed 7E.

6. Footpedal. Does it go from 07 to 77 or greater?

7. Footswitch 1 and 2. Do they press and release OK?

8. Metronome output. Does it beep when any button without an LED is pressed.

Now that all the front and some of the rear panel functions have been checked we can go on to the listening tests.

LISTENING TESTS

Before the tests begin I recommend that the memory test be run. The reason for this is to eliminate the memory from being suspect if any problems in the sounds are heard. To do this, boot up a memory test disk and wait for the "memory good" message on the display. If the test fails, see section on diagnostics for more info. After the memory test is run, reboot the machine with the test sound disk. If you do not have one it is easy to make. All you have to do is sample a 1KHZ ramp (sawtooth) wave into the E2 and save it to a disk that has been formatted and had software written on it (see users manual if you don't know how to sample). Name the disk "Test Ramp."

1. Channel Test Do all channels and their separate outputs work? The easy way to test this is to use the footswitch as a sustain pedal. Play 8 keys while holding down the footswitch. Now plug into each of the 8 separate outputs and listen.

2. Mix Out Test. With audio cable in mix out jack play 8 keys and verify that all 8 voices can be heard. Turn mix out pot through its full range and listen for anything out of the ordinary like clicks, pops, sound dropout. Check the pot for a smooth action through its full range.

3. Filter/Q/VCA Test. Each output channel has a filter with two sample/holds and a VCA with one sample/hold. The filters S/H's are for the cutoff frequency and Q. The VCA S/H is for the gain. The test will check that all three S/H's work and that the filter and VCA also work. To test, boot up the ramp test sound. Each channel needs to be tested separately so the channel disable function is used. To do this press Special, then 1. The display will show which channels are disabled. Press 2 thru 8 to disable those channels. We can now test Channel 1. To enter the filter tests, press the filter button. The display will now read:

```
No current voice
   Play a key
```

Play the low A and press enter. The display will now read:

```
V01     Test Ramp
Add1    Voices Y/N
```

Press No on the keypad. The display will now read:

```
Filter    [0-3]
V01    Test Ramp
```

We can now select and test the filter function Channel 1. Press 1 on the keypad to select Freq. Q and envelope amount. The display will now show:

```
Freq    Q    Env
xxx     xx   xxx    (x=current value)
```

Adjust the Q to 99. Adjust the Env to 0. Now move slider A through its entire range while playing the low A. The key will have to be released and pressed after each slider movement to hear the change. Listen for the filter opening and closing as the slider is moved through its entire range. There should be very little signal at setting 0 and full signal at setting 120. When in the low end of the freq setting (20-50) you should hear a wah-wah pedal type of sound from the Q being at maximum. On some filters they will self-oscillate and a tone will also be heard. Adjust the Q to 0. Play the low A again. The wah-wah effect and tone should be gone. While playing the low A, run the Q through its full range and listen for its effect. Now set Freq, Q and Env to the following values.

```
Freq = 00     Slider A
Q    - 60     Slider B
Env  = 50     Slider C
```

Press 3 on the keypad to enter filter envelope mode. The display will show:

```
Atk  Dec  Sus  Rel
 xx   xx   xx   xx   (x=current value)
```

Set ASDR to the following values:

```
Atk = 01     Slider A
Dec = 01     Slider B
Sus = 32     Slider C
Rel = 01     Slider D
```

While playing the low A, change the sustain value from 0 to 32. At 0 there should be very little sound. At 32 there should be maximum. Set sustain to 0 and attack to 32. Play the A. Listen for a slow smooth attack. Set the ADSR to the following values.

Atk = 01
Dec = 01
Sus = 32
Rel = 31

4. Sample Test. Using a signal generator or synthesizer sample a 5 KHZ sine wave (see users manual on sampling for more information on how to do this). Play the sound back at the original pitch and listen for excessive noise or distortion. Play the sound at one octave above the original pitch and listen for noise and distortion and that the loudness of the signal is within 3 DB of the original pitch.

5. Disk Tests. The Debug EPROM can be used for this if you want to test the drives critically. To do a basic test take a blank disk and format it in Drive 1. Now write software and sounds on it. Put the disk in Drive 2 and turn the power off and back on and see if the machine loads the disk and plays the sound. See if it works in Drive 1. If you have a 1 drive machine the same procedure is done except that the disk is tested in the drive you made it in.

6. MIDI Test. To test, plug a MIDI cable from MIDI in to out. Play several keys and hold them. Pull either end of the MIDI cable out. Release the keys and they should continue to make sound (this is easier with a looped sound).

7. Computer Interface Connector. Use the Debug PROM for this (see section 6 for more info on the Debug PROM).

SCANNER BUTTON #'S FOR TEST DISK

The table below lists the value that will be displayed for pressed buttons and keys when using the scanner test disk.

Button or Key Pressed	Value Displayed (hexadecimal)
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
Dynamic Allocation	A
Tune	B
Transpose	C
Filter	D
VCA/LFO	E
Voice Definition	F
Preset Definition	10
Enter	11
Real Time	12
Disk	13
Sample	14
Special	15
Footswitch 1	16
Footswitch 2	17
Setup	18
Define	1A
Edit	1B
Record	1C
Play	1D
Select	1E
Stop	1F

KEYBOARD VALUE TABLE

	OCTAVE					
NOTE	0	1	2	3	4	5
C	0	C	18	24	30	3C
C#	1	D	19	25	31	
D	2	E	1A	26	32	
D#	3	F	1B	27	33	
E	4	10	1C	28	34	
F	5	11	1D	29	35	
F#	6	12	1E	2A	36	
G	7	13	1F	2B	37	
G#	8	14	20	2C	38	
A	9	15	21	2D	39	
A#	A	16	22	2E	3A	
B	B	17	23	2F	3B	

MEMORY TEST DISK INSTRUCTIONS

The memory test disk will test all of the Dynamic RAM and report the first failure that occurs. It reports the failing address, the bad data it read and the data it expected. This makes it easy to find and fix memory IC failures. To run the test, insert the disk in the top drive and apply power. The test will start by itself and give the following information on the display:

Memory Test in
Progress: Sgmt=1

As the test progresses the segment number will be updated to reflect the current segment under test. When a failure occurs, the display will change to inform you the address of the failure, the bad data and the data it expected. Below is an example failure that would be displayed if address 40910 had failed:

Error At 40910
Data: DE S/B: DF

NOTE: Data is what was read back. S/B is what the data should be.

Using the memory layout (see memory theory of op) we can determine which row the bad IC is in. Address 40910 corresponds to Memory board IC 2-9. This is the piggyback board that sits on top of the digital board. Now that the bad row has been isolated the IC can be found. This is done by determining which bit is bad using the information on the display. We must first convert the good and bad data to binary then compare them as shown below:

Data DE = 11011110
S/B DF = 11011111

This shows us that data bit 0 is 0 when it should be 1. We can now use the schematic to find which IC is bit 0. Refer to page 3 of 6 for the memory option board and we see that IC 2 thru 9 are on this page. To find bit 0 look at pin 14 of each IC until the signal name for bit 0 (MDOBO.D) is found, which is IC 9. Replace IC 9 to fix the problem.

NOTE: MDOBO.D stands for Memory Data Output Bit 0 . Digital.

THE MAIN DEBUG EPROM

The debug program is meant to aid technicians in debugging and testing the E II. It is especially useful for testing and diagnosing the Main CPU SRAM. When the program runs, it will give a sign on message and wait for commands. To use it, you need a terminal and an RS-232 cable. The terminal must be set for 1 start bit, 7 data bits, 1 stop bit, no parity, auto line feed. It must also be set for 9600 Baud.

The cable must conform to the following:

TERMINAL	E II
pin 1	pin 1
pin 2	pin 2
pin 3	pin 3
pin 4	pin 4
pin 5	pin 5
pin 6	pin 6
pin 20	pin 20

DEBUG COMMAND SUMMARY

HELP
Explains each command.

SET
Sets a single memory location or register to a value.

DISPLAY
Displays single or multiple memory locations or user register set.

FILL
Fills a block of memory with a byte value.

MOVE
Moves a block of data from one area of memory to another.

COMPARE (CP)
Compares the data in two blocks of memory and displays differences.

INPUT
Gets a byte from an input port and displays it.

OUTPUT
Sends a byte to an output port.

CALL
Runs a user entered program.

RETURN
Jumps to a user entered program on NMI or RST.

PUTDISK
Moves a block of data from memory to disk.

GETDISK
Moves a block of data from disk to memory.

TEST
Tests memory and disk drives.

EXERCISE
Exercises disk drives, memory, and I/O ports.

DEBUG COMMANDS

SERVICE NOTE:

Commands are terminated by `RETURN´. All numbers are hexadecimal unless otherwise noted.

HELP — HE [command]

example:
```
HE T      explains the TEST command.
HE S      explains the SET  command.
```

SET
```
S  M  [address]  [data]
S     [register] [data]
```

example:
```
S  M  8000 FF  sets  memory location 8000 to FF.
S  HL FF       sets user HL register pair to FF.
```

SERVICE NOTE:

The E II has OF (Decimal 16) blocks of RAM. Each block is 8000 bytes long (Decimal 32K). The SET command can address any 2 byte address. Addresses below 8000H (32K) are reserved as program area. You should only modify memory above 8000H (32K) or you risk crashing the program. To select a particular segment of RAM, write its segment number into the segment register using the OUTPUT command (O 6B segment number). See Theory of Operation for further explanation of RAM operation. See OUTPUT command, below.

The SET Register command does not actually alter the Z-80 registers. There are RAM locations reserved as user registers. The data in these locations are loaded into Z-80 registers when a CALL command is executed. The previous contents of the Z-80 registers are saved first. When the user program ends with an RST, the original Z-80 register contents are restored.

DISPLAY D M [start address] [end address]
D P [start address]

example: D M 8000 9000 displays memory from 8000 to 9000.
D M 8000 displays a page (100 bytes, 256 Decimal) of memory starting at 8000.

SERVICE NOTE:

The E II has OF (Decimal 16) blocks of RAM. Each block is 8000 bytes long (Decimal 32K). The DISPLAY command can display any range of addresses from 0000H to FFFFH (Decimal 65K). To select a particular segment of RAM, write its segment number into the segment register using the OUTPUT command, below.

FILL F [start address] [end address] [byte]

example: F 8000 9000 FF fills memory from 8000 to 9000 with FF.

MOVE M [from] [to] [length]

example: M 8000 9000 2F moves a block 2F bytes long from its present location, starting at 8000 to a new location starting at 9000.

COMPARE CP [start] [start] [length]

example: CP 8000 9000 2F compares 2 blocks of memory 2F bytes long, one starting at 8000 and one starting at 9000. Differences will be displayed on the terminal.
NOTE: both memory blocks must be in the same RAM segment.

INPUT I [port #]

example: I 6B reads port 6B and displays its data byte.

OUTPUT O [port #] [byte]

example: O 6B 1A writes 1A to port 6B.

CALL CALL [address]

example: CALL 8000 runs the user routine at address 8000.

RETURN RE [address]

example: RE 8004 runs the routine at address 8004 when a Nonmaskable Interrupt (NMI) or a restart (RST 38) has been executed.

PUTDISK P [track#] [address] [#tracks]

example: P 1 6 000 1 puts 1 track of data (each track holds E00 bytes) onto track 1. The data starts at address 60000 (address 8000 in Segment C). NOTE: there must be a space after the first digit of the address. The debug monitor calculates the segment value for the address you specify (See memory map, p 7-34).

GETDISK G [track#] [address] [#tracks]

example: G 1 6 000 1 gets a track of data (each track holds E00 bytes) from track 1. The data is stored starting at address 60000 (address 8000 in segment C). NOTE: there must be a space after the first digit of the address. The debug monitor calculates the segment value for the address you specify.

SERVICE NOTE:

track# con be from 0 to 9F.

address can be from 0 0000 to 7 FFFF.

#tracks can be from 0 9F.

DO NOT GO BELOW 8000H OR YOU WILL CRASH DEBUG.

TEST T [option] [parameter list]

options:
- D test disk
- B test burst timing
- C test drive's compatibility
- M test memory

Test Disk T D [drive] [#passes]

example T D 0 5 tests drive 0 (the top one) 5 times. #passes can be any number up to FF. FF passes take abut 8 hours to complete. Error counts are displayed as shown below:

CRC:	CR1:	WT:	XFR:
0000	0000	0000	0000

NOTE: CRC means cyclic redundancy check. It is a data validity test. SIO reports a CRC error if the data from the disk is invalid. If it fails on 10 consecutive read attempts, a fatal disk error message is displayed.

CR1 means a CRC error on the first attempt to read data from the disk. This is not unusual as the E II exceeds the drive specifications on a first read. This is done to gain disk speed. If E II gets a CR1, it makes another attempt to read data.

WT means wrong track error. This is usually a drive problem.

WT1 means wrong track on the first try. See CR1, above.

XFR means transfer error. A block of memory is written to the disk, then read from the disk into a different area of memory. The two memory blocks are compared. If they don't match, Debug logs a transfer error.

FATAL DISK ERROR CODES

Sometimes the disk test won't run at all. The fatal error codes help to clarify what went wrong. The display will show:

Fatal Disk Error Cn

(n is the error code as explained below.:)

C2 - Drive not ready. No disk. Unable to read track ID or unable to read sync mark on disk.

C3 - Write protected error. Unable to write to disk because there is a write protect tab on the diskette.

C4 - Not used.

C5 - Read track number error. Misread track number more than twice.

C6 - Fatal CRC error. Read disk incorrectly 10 times.

C7 - Drive not there.

Test Burst T B [drive#]

example: T B tests drive 0 (the top one)

This test displays drive burst (Index) timing. The value is displayed in hexadecimal and must be between 60 and 70. A displayed value of 6E would be within specifications.

Burst Timing Specifications:

Minimum	Typical	Maximum
60	69	70

Burst timing is adjustable. You must have an oscilloscope and a special calibration diskette. In most cases it is much simpler to swap out the disk drive.

SERVICE NOTE:

The burst timing test will fail if you use a diskette formatted on any out of spec drive. Format a diskette on the drive you want to test. See the EXERCISE command.

Test Compatibility T C [drive#]

example: T C 1 tests compatibility of drive 1 (the bottom one).

This test requires a special disk.

Test Memory T M [segment#] (0-F optional)

example: T M B tests memory starting with segment B.

T M tests the entire memory.

Exercise E [device] [location] [data]

example: E D 0 5 exercise disk 0 5 times.

E M 6 0000 exercise memory location 60000.

E I 22 exercise input port 22 (read).

E O 11 FF exercise output port 11 (write FF).

E IO FF exercise port FF (read/write).

NOTE: The disk exercise formats the entire diskette, then verifies it. It repeats the number of times specified in the command. Use this command to format a disk for other tests.

The memory exercise alternates writing AA and 55 to the specified location. The location is exercised continuously.

The port exercises are continuous. You must reboot DEBUG to perform another test.

.pa

Emulator II Specifications

Controls

Master Control

Select dynamic allocation
Tune keyboard
Transpose keyboard
Mix output volume
Sliders A-D (set parameters)
Keypad (select preset, select menu function, enter data)

Filter

Frequency
Resonance
LFO mod depth
Keyboard tracking
Envelope mod amount
Filter ADSR parameters

VCA/LFO

VCA ADSR parameters
LFO rate
LFO delay
LFO random variation
LFO mod depth (VCA)

Voice Definition

Voice truncation
Voice looping
Bidirectional looping
Sound splicing
Display sound length (bytes)
Velocity control destinations:
  VCA level; VCA attack; VCF frequency; VCF attack; VCF resonance
Vibrato depth
Voice level
Voice tuning
Solo mode
Loop in release
Backwards mode
Digitally combine voices
Realtime control enable
Save voice to disk

Preset Definition

Get voice from disk
Copy/rename voice
Erase voice from memory
Erase sequence from memory
Erase preset from memory
Erase bank from memory
Catalog voices in bank
Catalog sequences in bank
Catalog presets in bank
Display memory remaining
Create preset
Assign voice to keyboard
Edit voice assignment
Deassign voice from kybd
Create velocity switch
Create velocity crossfade
Create positional crossfade
Nontransposition mode
Arpeggiator parameters
MIDI parameters
Copy/rename preset
Replicate preset

Realtime Controls

Continuous control sources:
  Left wheel; Right wheel; Footpedal; MIDI controls A, B, C
Destinations: Pitch; Filter Fc; Level; LFO → pitch; LFO → Fc; LFO → level; ADSR attack rate
Switch control sources:
  Footswitches 1 and 2
Destinations: Sequencer control; Sustain; Release; Sustenuto; Advance preset; Sample

Disk

Get bank from disk 1
Get bank from disk 2
Disk space remaining
Copy disk
Catalog voices
Erase voice from disk
Save bank to disk
Format disk

Special

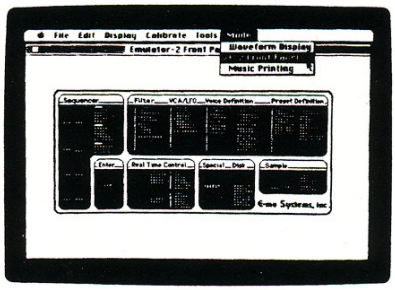
Catalog current special functions

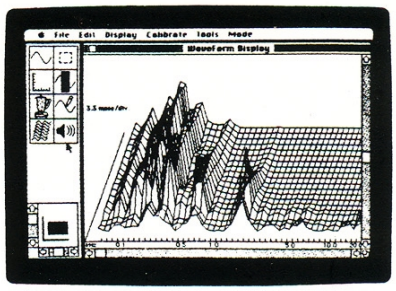
Sequencer

Select sequence
External clock
Define
  Create sequence
  Set time signature
  Set sequence length
Setup
  Select track
  Set tempo
  Set autocorrect
  Select cue tracks
  Set SMPTE start
  Set countdown
Edit
  Erase track
  Punch in
  Bounce tracks
  Store controls
  Reassign preset
  Append sequence
Record
Play
Stop

Sample

Gain set
VU display
Define voice
Threshold set
Sample length
Arm sampling
Force sampling
Stop sampling





The Digidesign Macintosh sound lab system turns your Emulator II into a complete computer music system.

Specifications

Computer

Sample length - 17 seconds
Channels - eight
Playback frequency range - 20Hz-20kHz
Dynamic range - 96dB
Power requirements - 115v/230v; 60Hz/50Hz; 150W max

Keyboard

Range - 5 octave/61 key, C to C
Velocity sensing - programmable sensitivity
Splits - up to 60, programmable

Analog Processing

VCF - 4 pole lowpass filter, one per channel
VCA - one per channel
Envelope generator - ADSR, two per channel
LFO - one per channel

Data Storage

Medium - 5¼" floppy diskettes, soft sectored, double sided, double density
Storage capacity - approx. 500k bytes per diskette
Drives - double sided, half height. One standard, second drive optional

Inputs

Sample; SMPTE clock; MIDI; Voltage A/D (footpedal); Footswitch 1; Footswitch 2

Outputs

Mono mix; Individual channels (8); SMPTE clock; MIDI; Metronome

Computer Interface

RS-422

Standard Accessories

Footpedal
Footswitches (2)
10 diskettes

Optional Accessories

Second floppy disk drive
Macintosh sound lab system
Winchester hard disk storage system

E-MU Systems, Inc.
applied magic for the arts
2815 Chanticleer, Santa Cruz, CA 95062
(408) 476-4424

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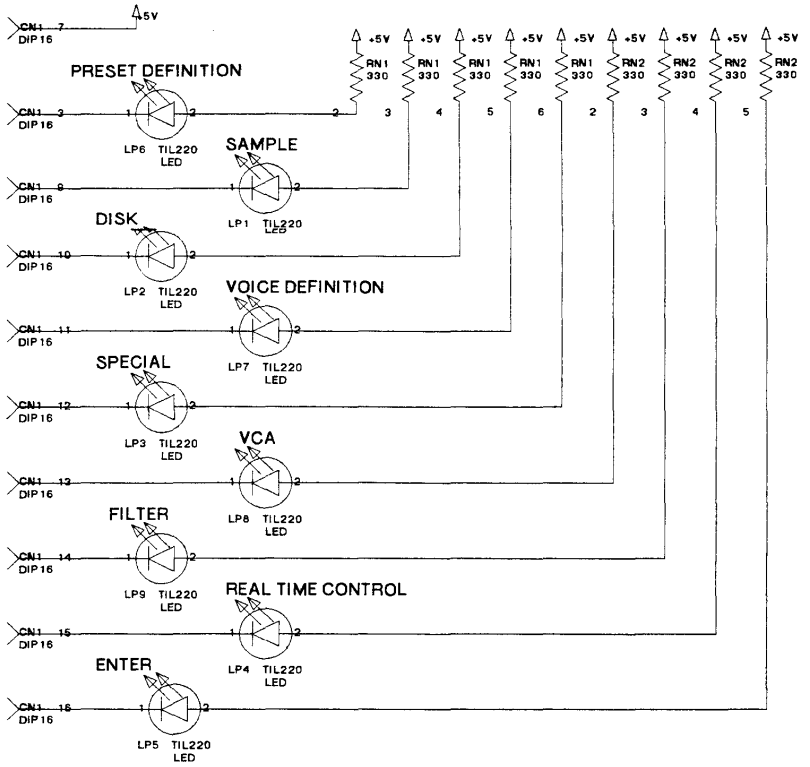
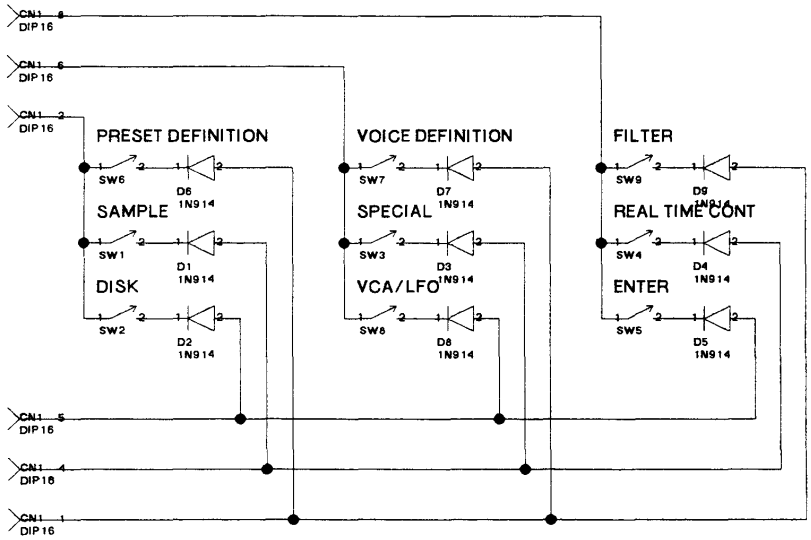
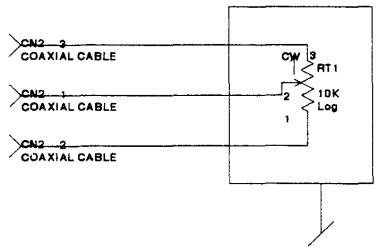
EMULATOR II

SCHEMATICS

EMULATOR II SCHEMATICS

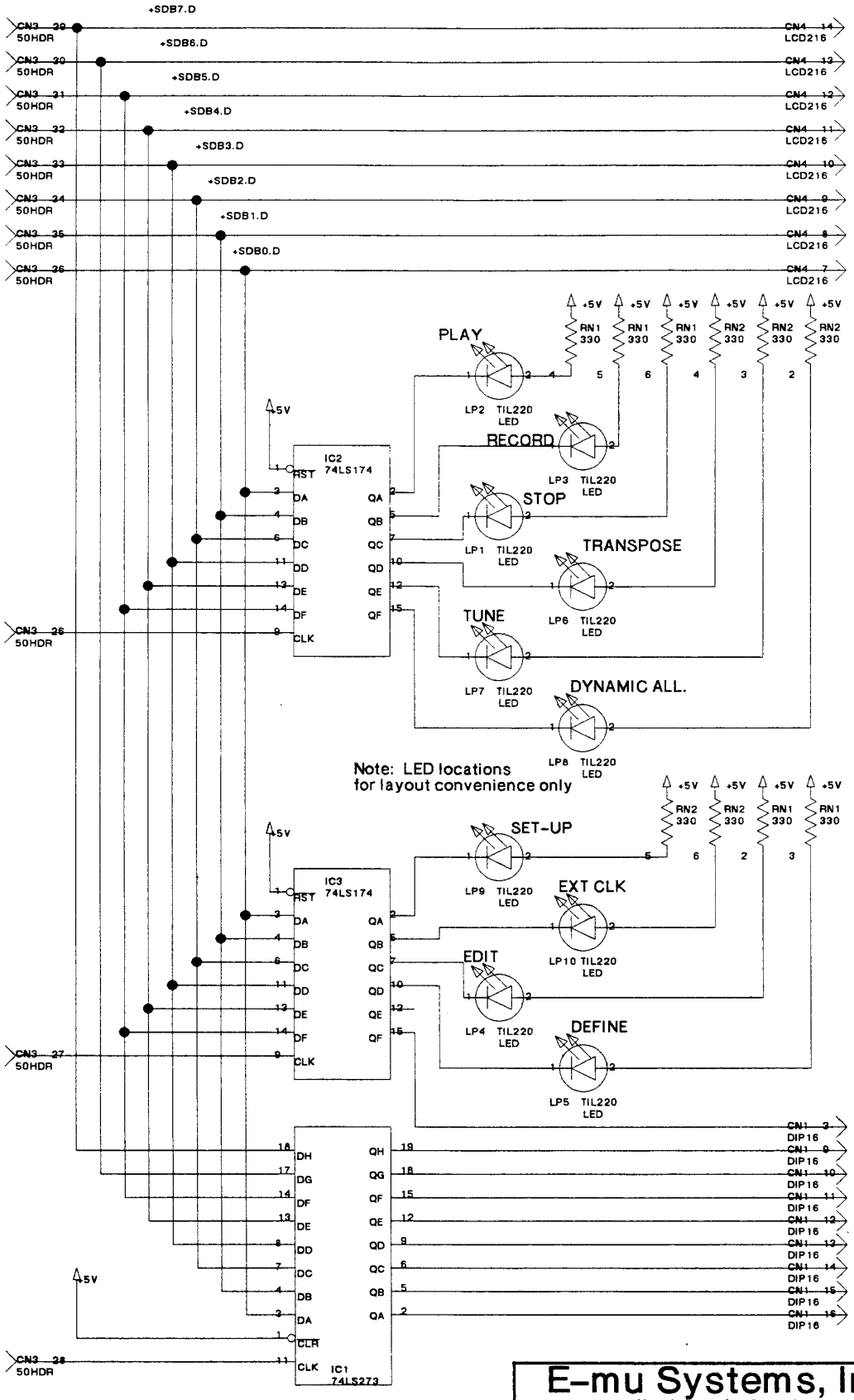






Note: LED's and Switches are located for convenience in layout only.

E-mu Systems, Inc. applied magic for the arts		
Emulator 2 Right Panel		
DRAWN BY DPR	DOC NO S-6155-001 PAGE 1 OF 1	
REV 1.A	DATE 850813	7 - 2

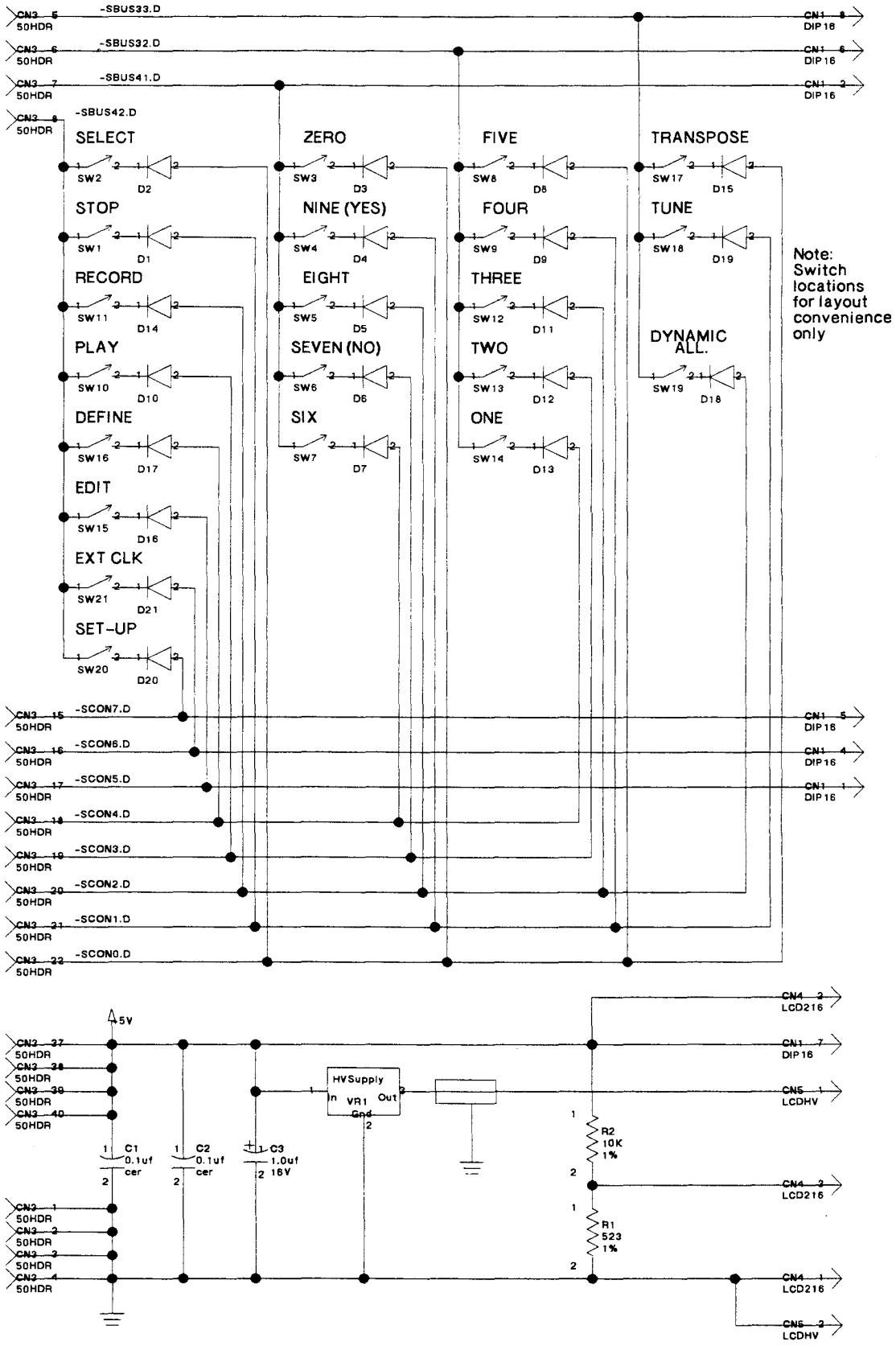


E-mu Systems, Inc.

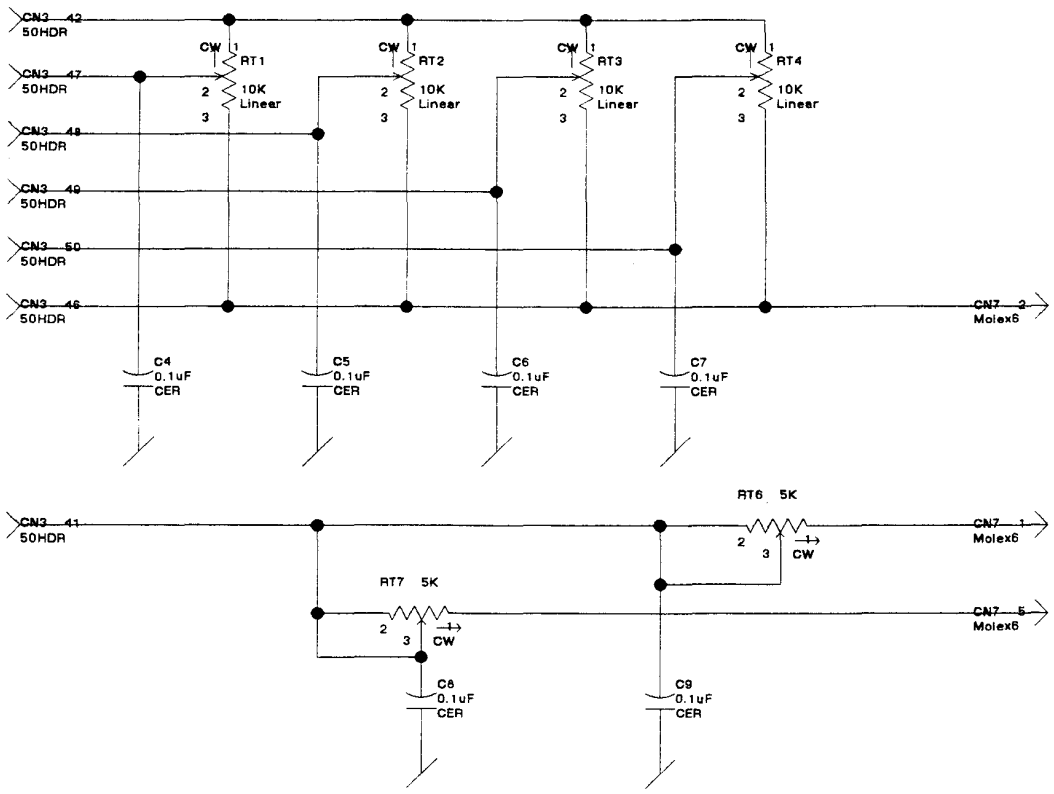
applied magic for the arts

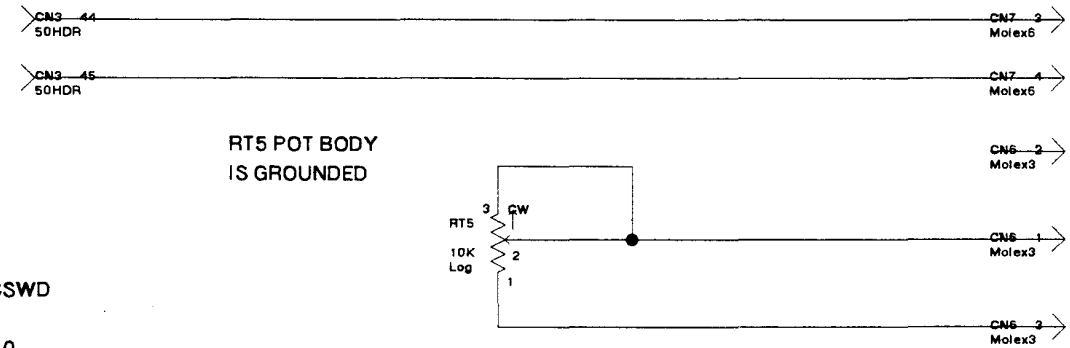
Emulator 2 Left Panel – LED drivers

DRAWN BY: DPR	DOC NO. S-8153-001 PAGE 1 OF 3	
REV. 1.A	DATE 850613	7 - 3



E-mu Systems, Inc.	
Emulator 2 Left Panel - PB's & supplies	
DOC NO. S-6153-001 PAGE 2 OF 3	7 - 4



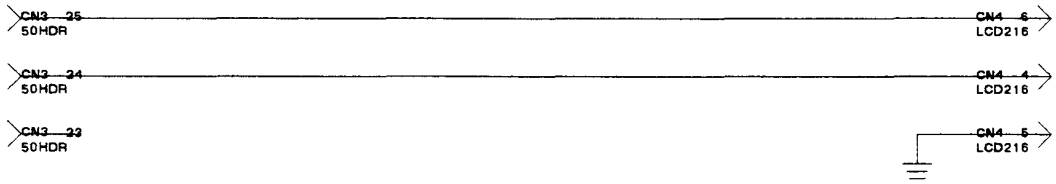


RT5 POT BODY
IS GROUNDED

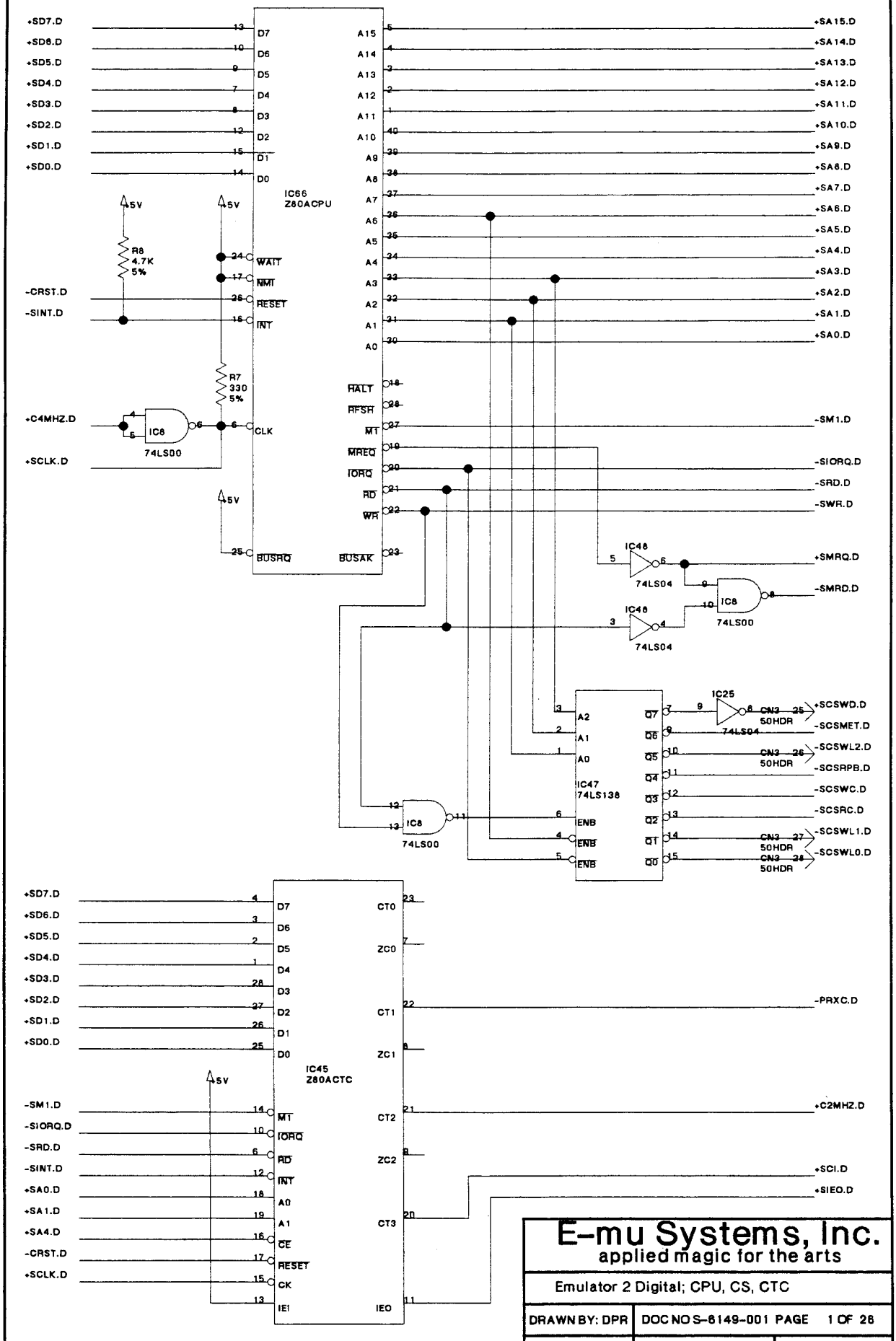
SCSWD

SA0

SA1



E-mu Systems, Inc.	
Emulator 2 Left Panel - Sliders & Wheels	
DOC NO. S-6153-001 PAGE 3 OF 3	7 - 5



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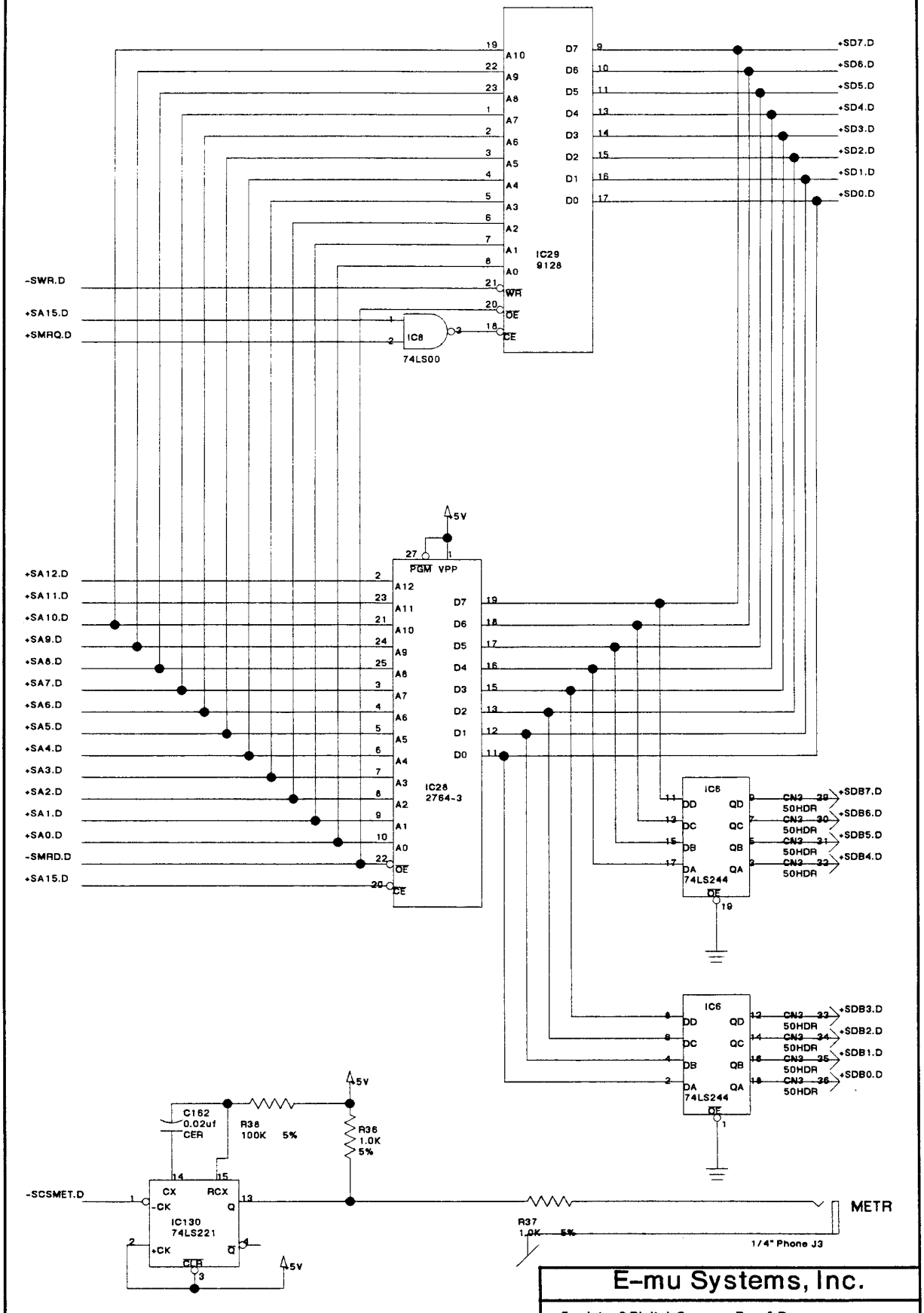
Emulator 2 Digital; CPU, CS, CTC

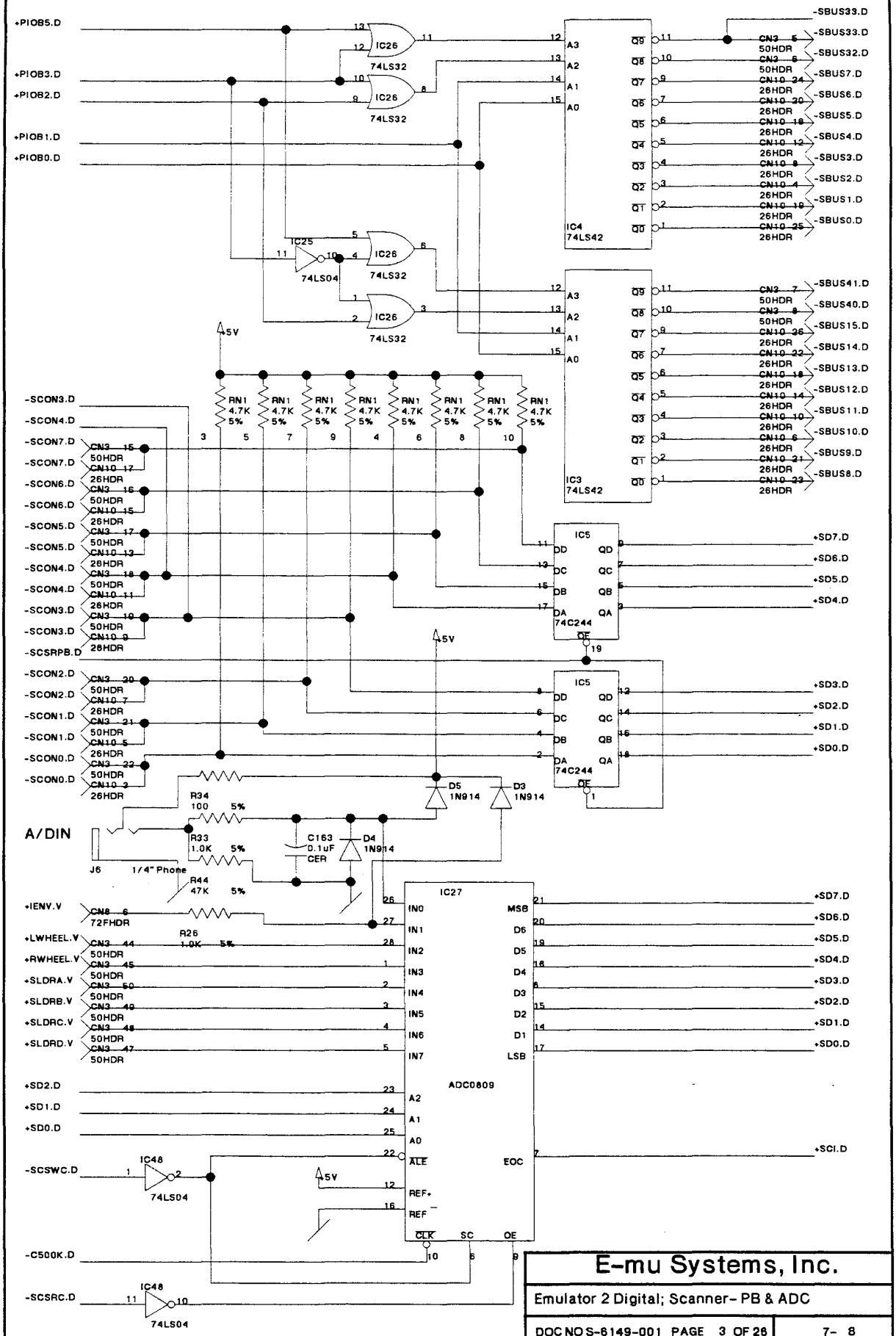
DRAWN BY: DPR	DOC NO S-6149-001 PAGE 1 OF 28	
REV 0.D	DATE 850605	7- 6



E-mu Systems, Inc.

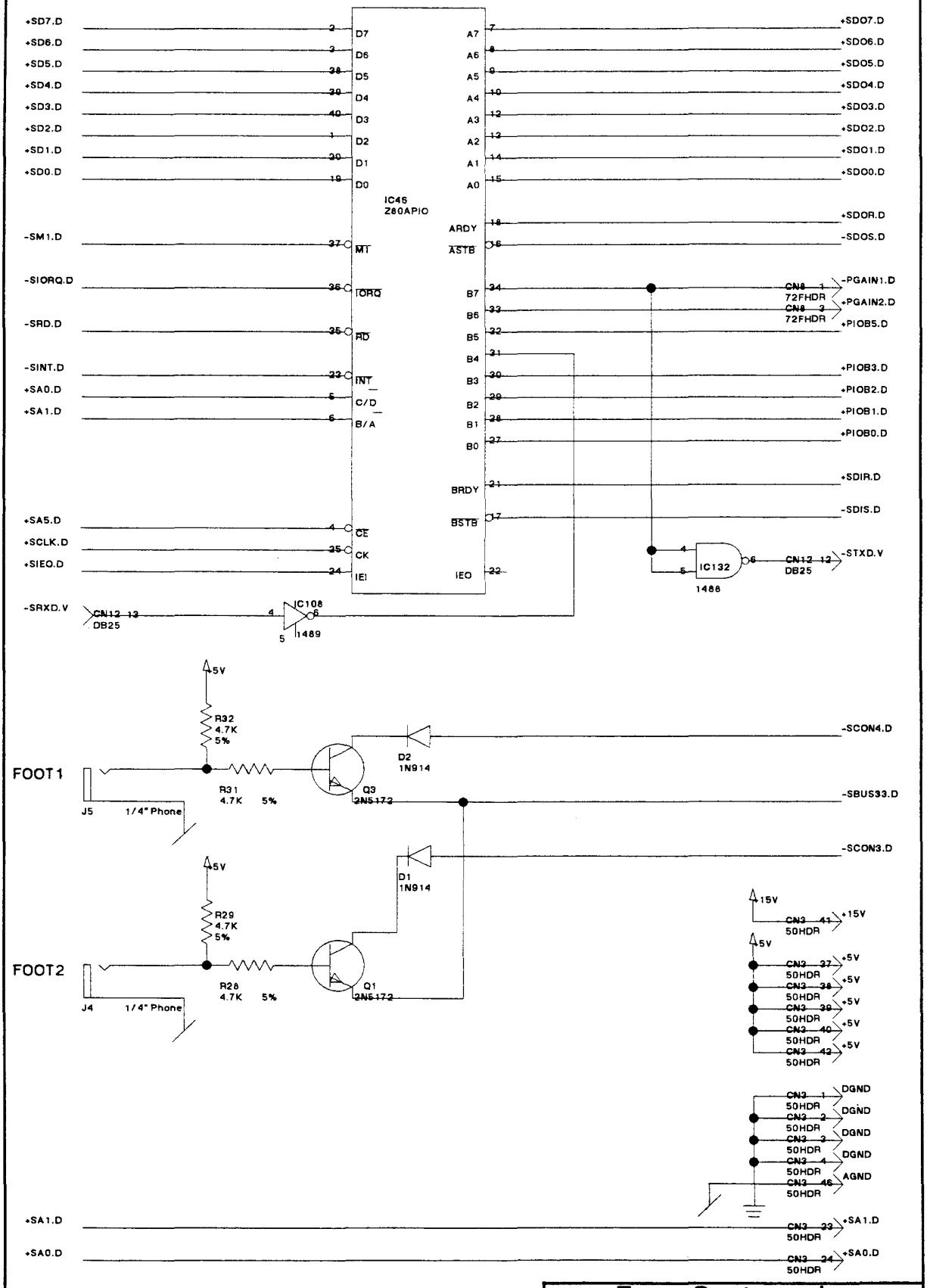
Emulator 2 Digital; Scanner-Ram & Rom

DOC NO S-6149-001 PAGE 2 OF 26 | 7- 7

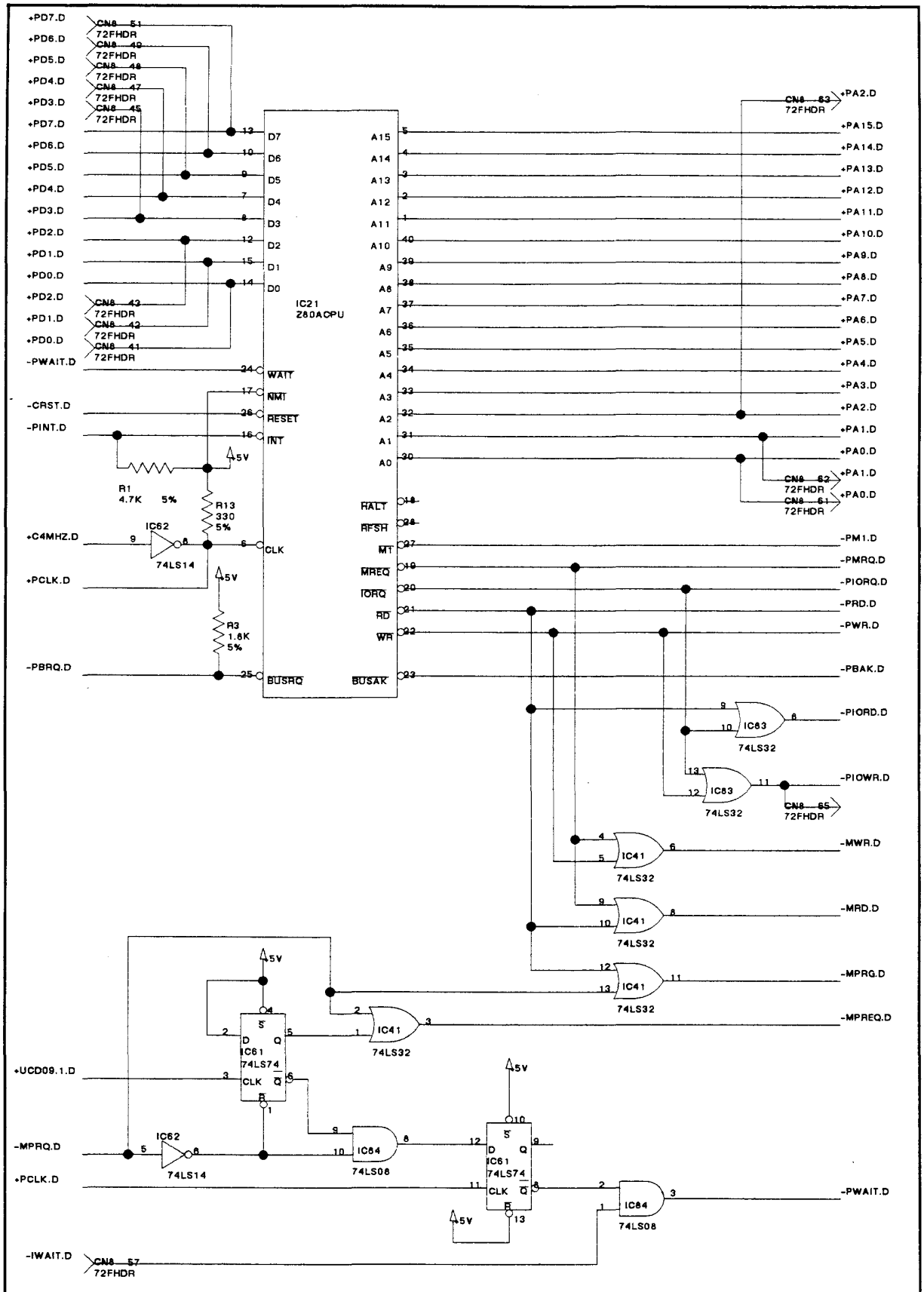


E-mu Systems, Inc.

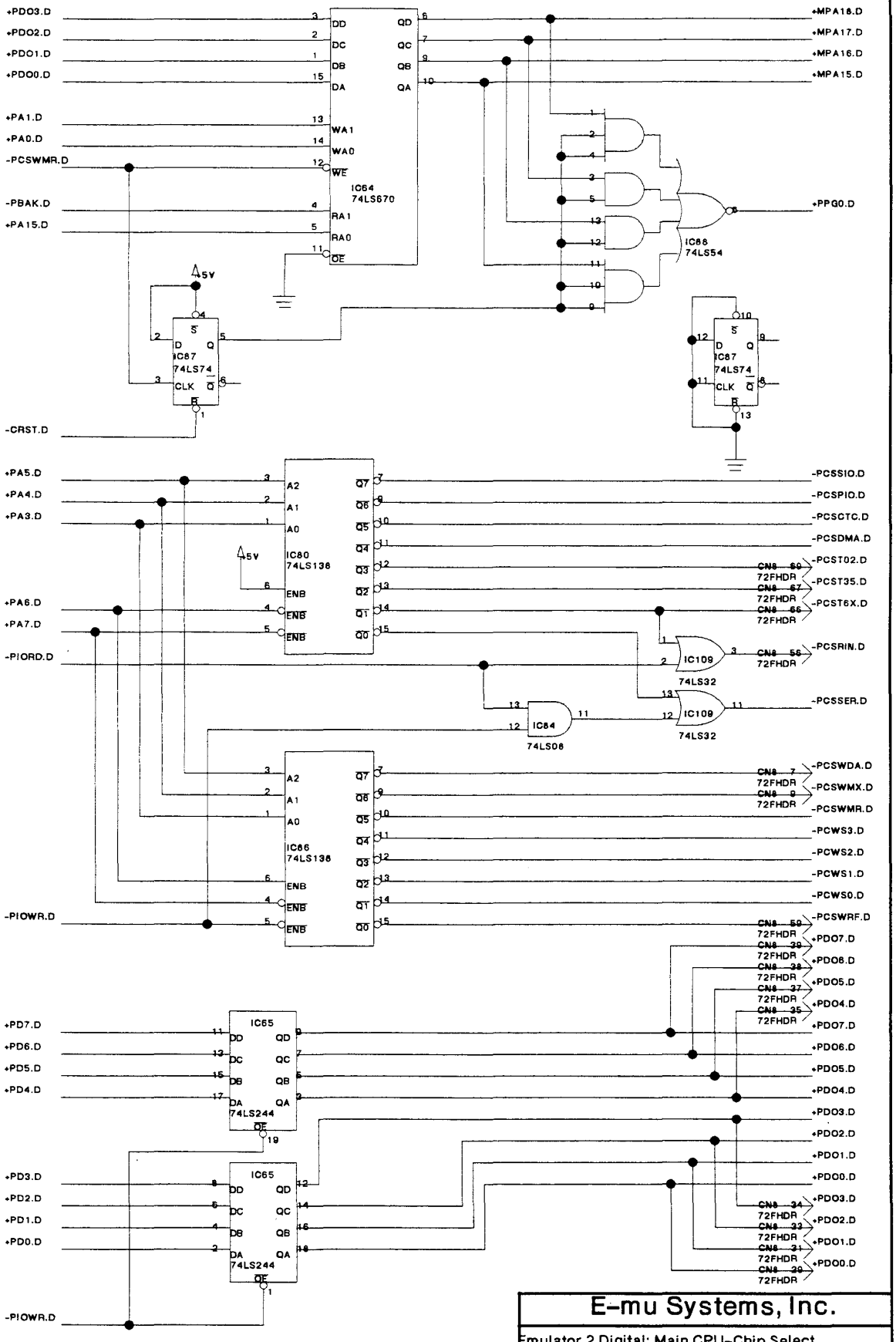
Emulator 2 Digital; Scanner- PB & ADC



E-mu Systems, Inc.	
Emulator 2 Digital; Scanner- Main Intrfc	
DOC NO S-6149-001 PAGE 4 OF 26	7- 9

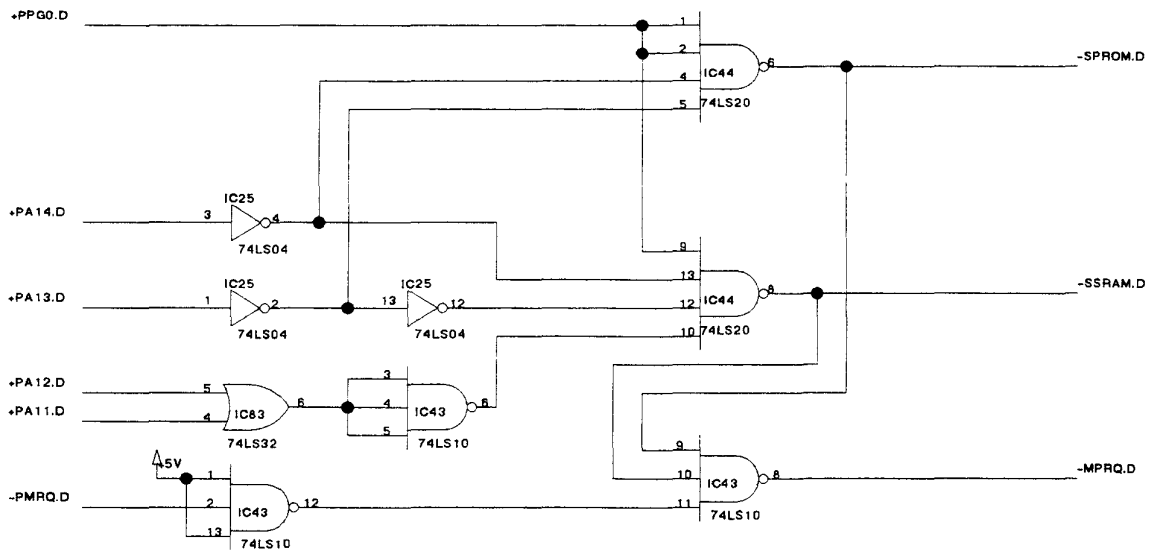


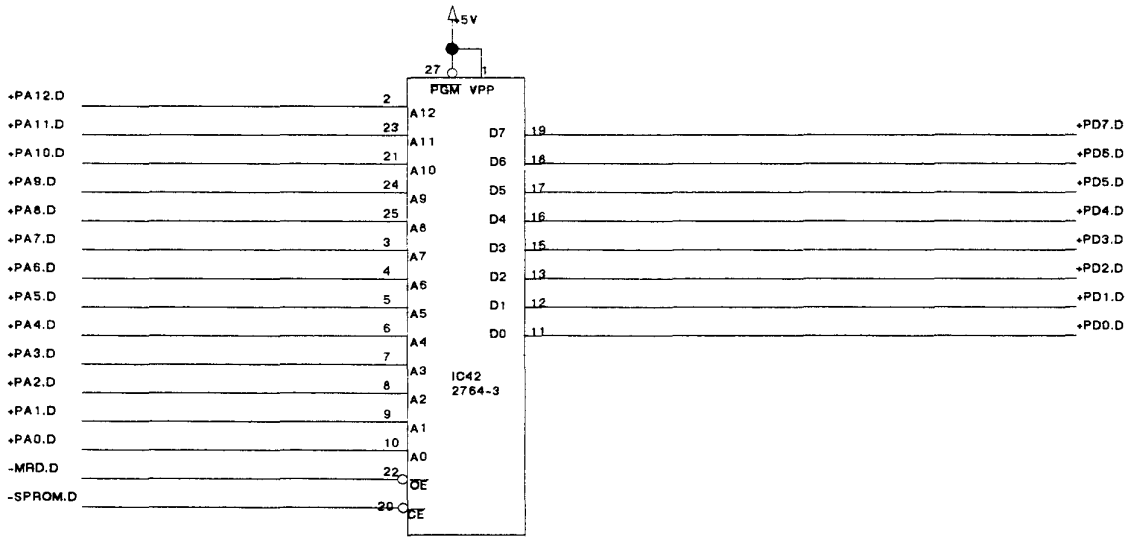
E-mu Systems, Inc.	
Emulator 2 Digital; Main CPU/Dcdr	
DOC NO S-6149-001 PAGE 5 OF 26	7-10

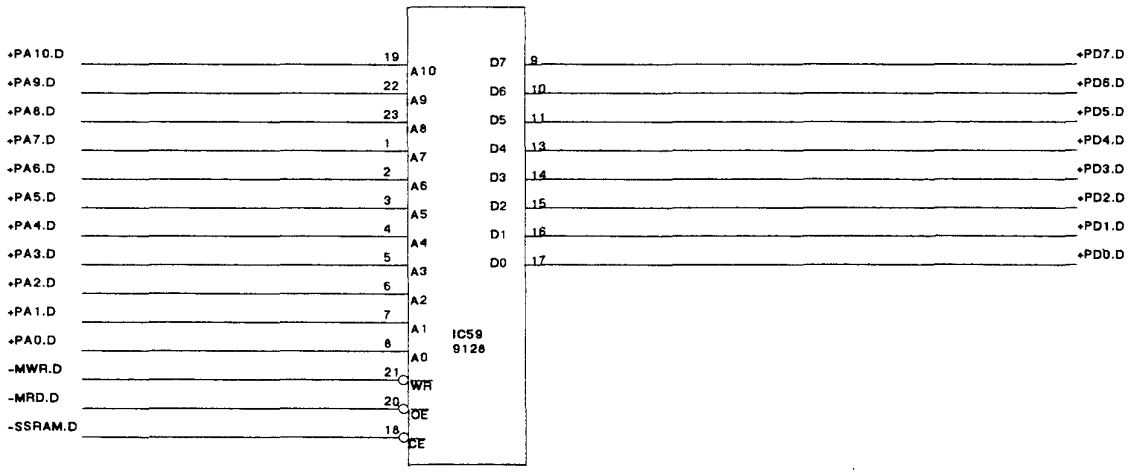


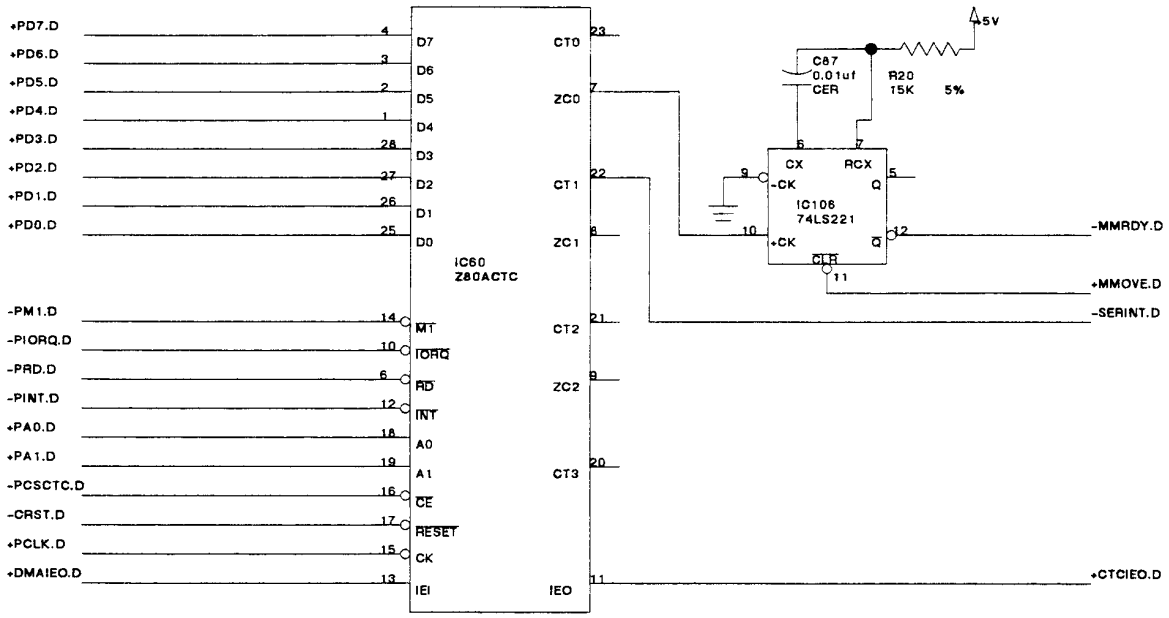
E-mu Systems, Inc.

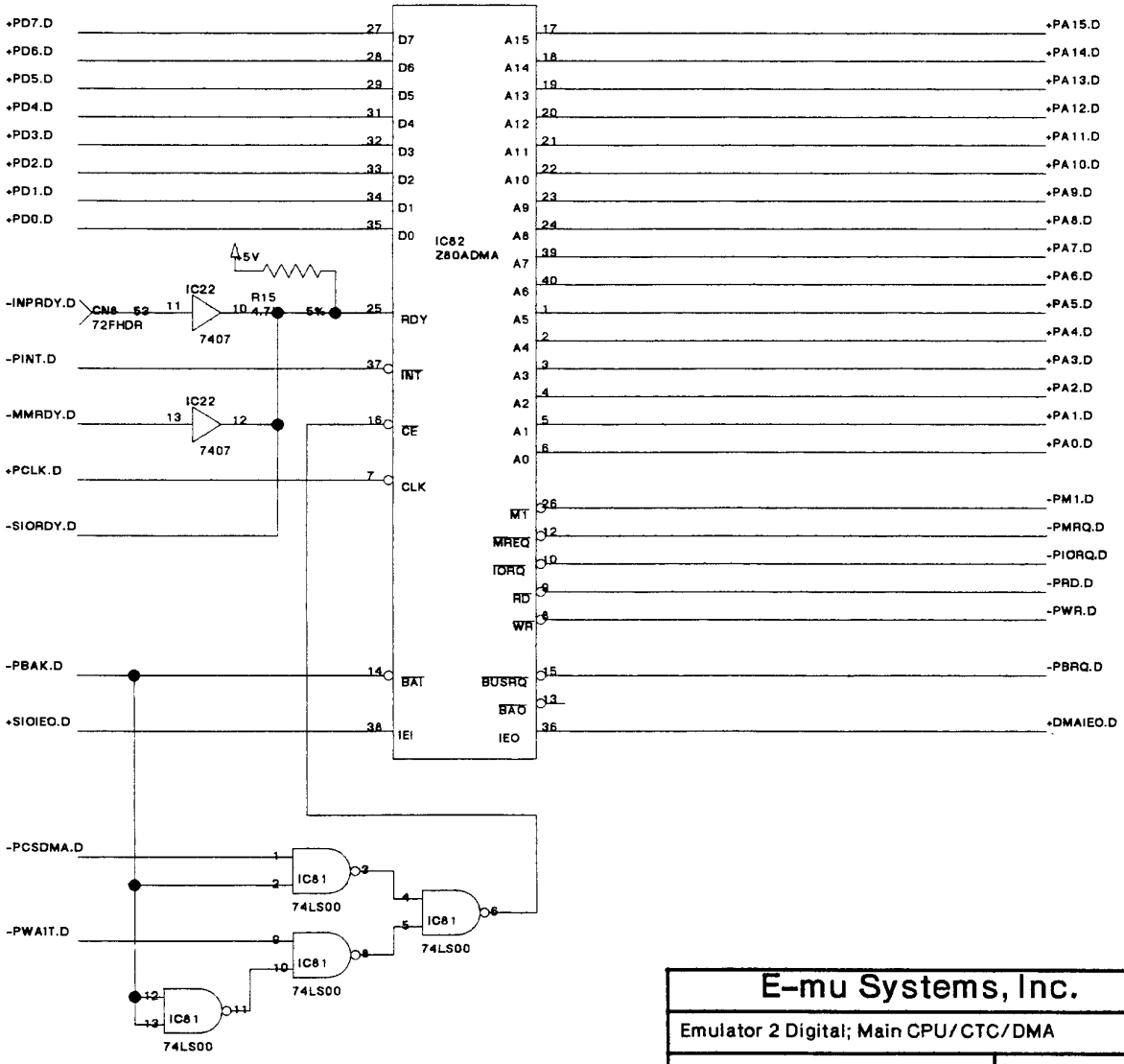
Emulator 2 Digital; Main CPU-Chip Select


+PPG0.D
-SPROM.D
IC44
74LS20
+PA14.D
IC25
74LS04
+PA13.D
IC25
74LS04
IC25
74LS04
-SSRAM.D
IC44
74LS20
+PA12.D
+PA11.D
IC83
74LS32
IC43
74LS10
5V
-PMRQ.D
IC43
74LS10
-MPRQ.D
IC43
74LS10

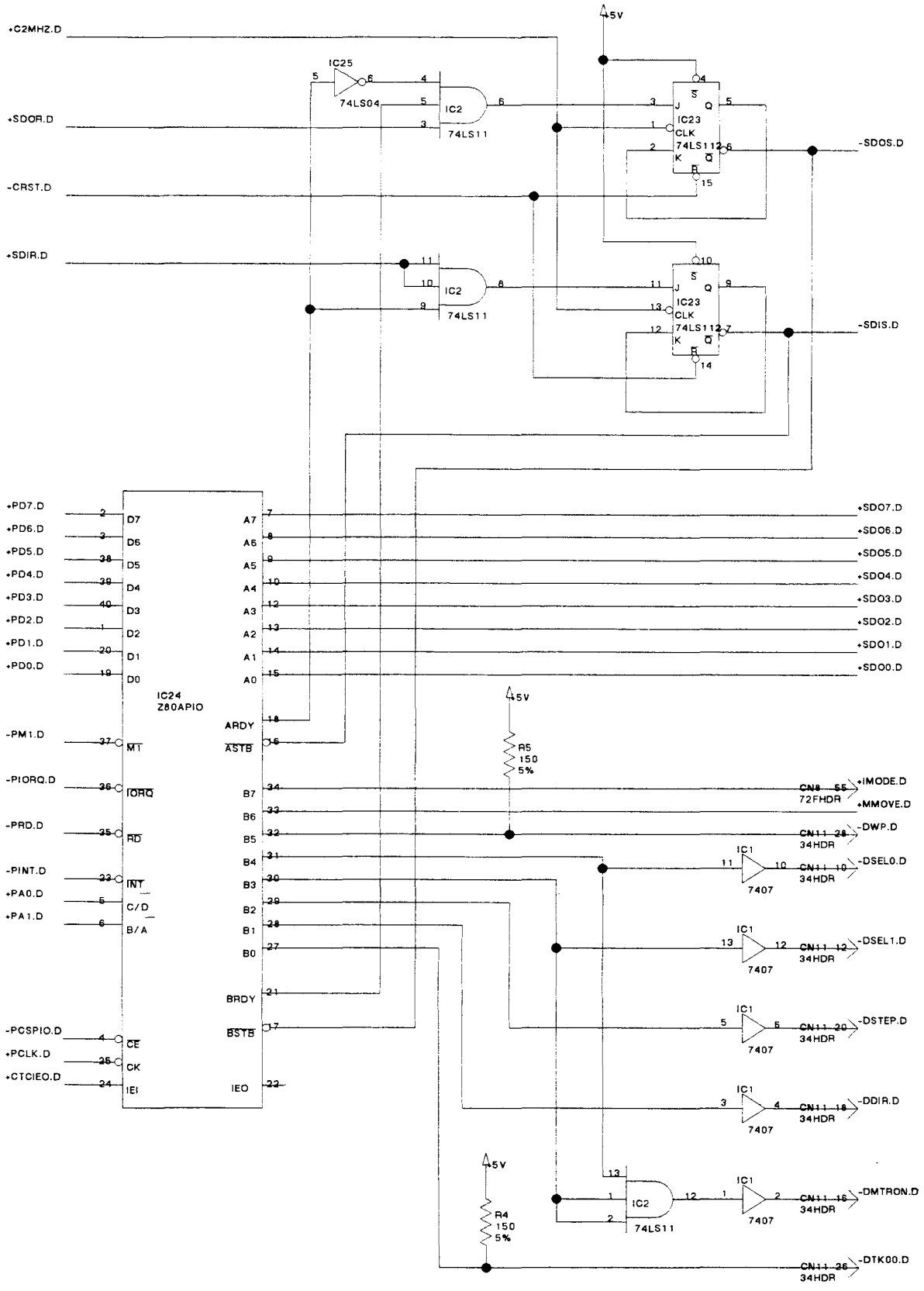

5V
PGM VPP
+PA12.D
+PA11.D
+PA10.D
+PA9.D
+PA8.D
+PA7.D
+PA6.D
+PA5.D
+PA4.D
+PA3.D
+PA2.D
+PA1.D
+PA0.D
-MRD.D
-SPROM.D
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
OE
CE
IC42
2764-3
D7
D6
D5
D4
D3
D2
D1
D0
+PD7.D
+PD6.D
+PD5.D
+PD4.D
+PD3.D
+PD2.D
+PD1.D
+PD0.D


+PA10.D
+PA9.D
+PA8.D
+PA7.D
+PA6.D
+PA5.D
+PA4.D
+PA3.D
+PA2.D
+PA1.D
+PA0.D
-MWR.D
-MRD.D
-SSRAM.D
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WR
OE
CE
IC59
9128
D7
D6
D5
D4
D3
D2
D1
D0
+PD7.D
+PD6.D
+PD5.D
+PD4.D
+PD3.D
+PD2.D
+PD1.D
+PD0.D

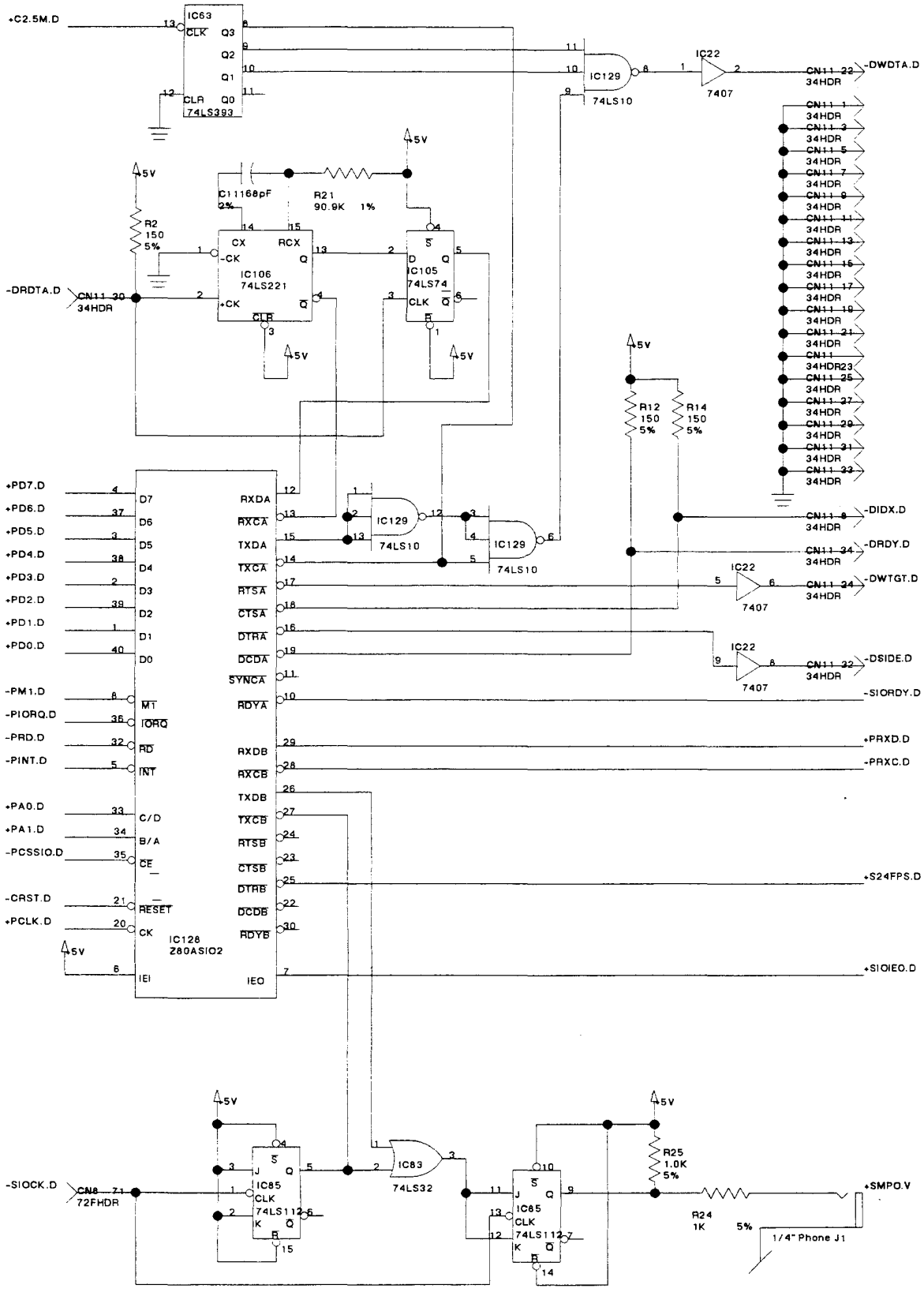




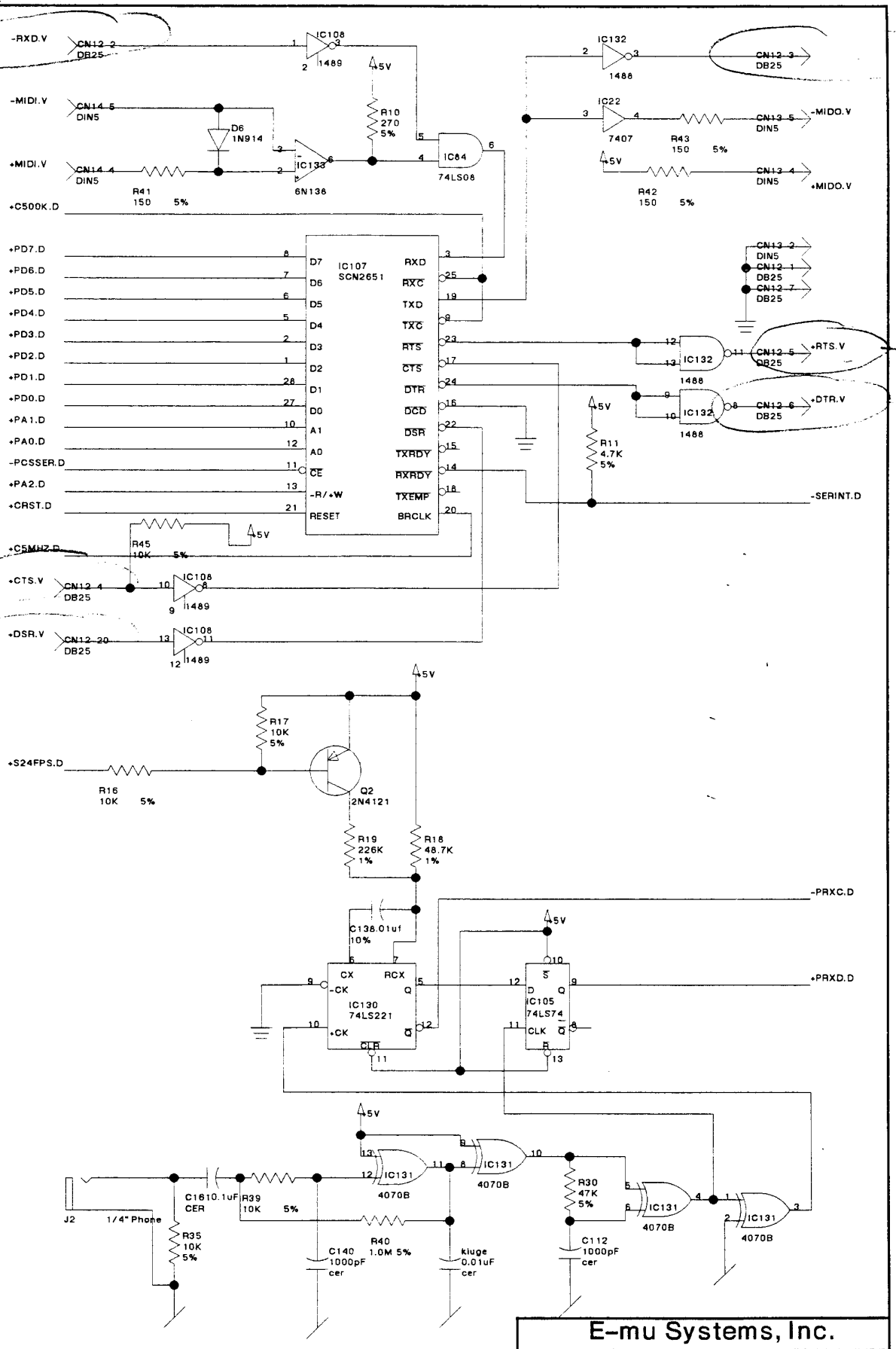
E-mu Systems, Inc.	
Emulator 2 Digital; Main CPU/CTC/DMA	
DOC NO S-6149-001 PAGE 8 OF 26	7-13



E-mu Systems, Inc.	
Emulator 2 Digital; Main CPU Scan Intrfc	
DOC NO S-6149-001 PAGE 9 OF 26	7-14

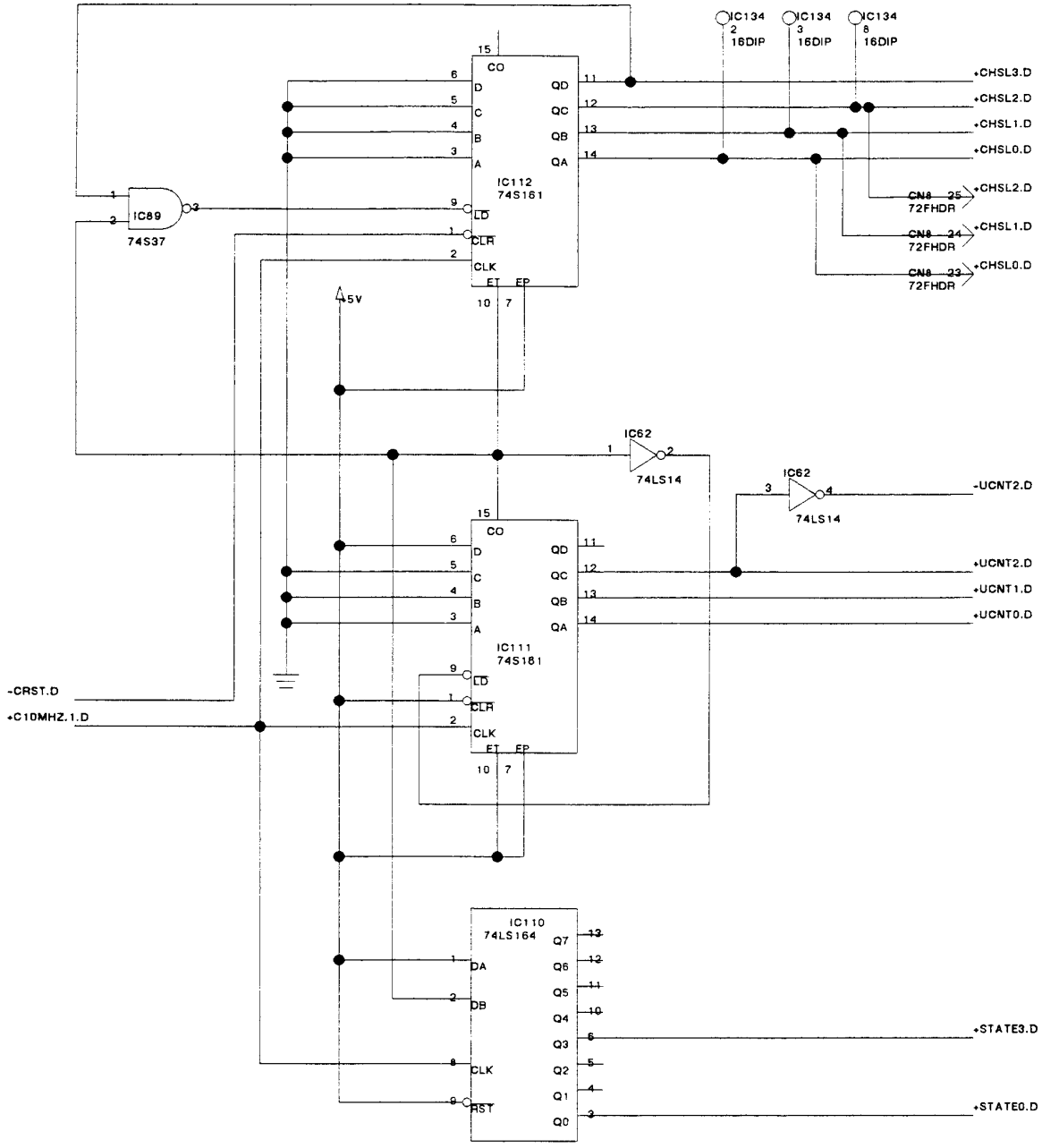


E-mu Systems, Inc.	
Emulator 2 Digital; Disk Interface	
DOC NO S-6149-001 PAGE 10 OF 26	7-15

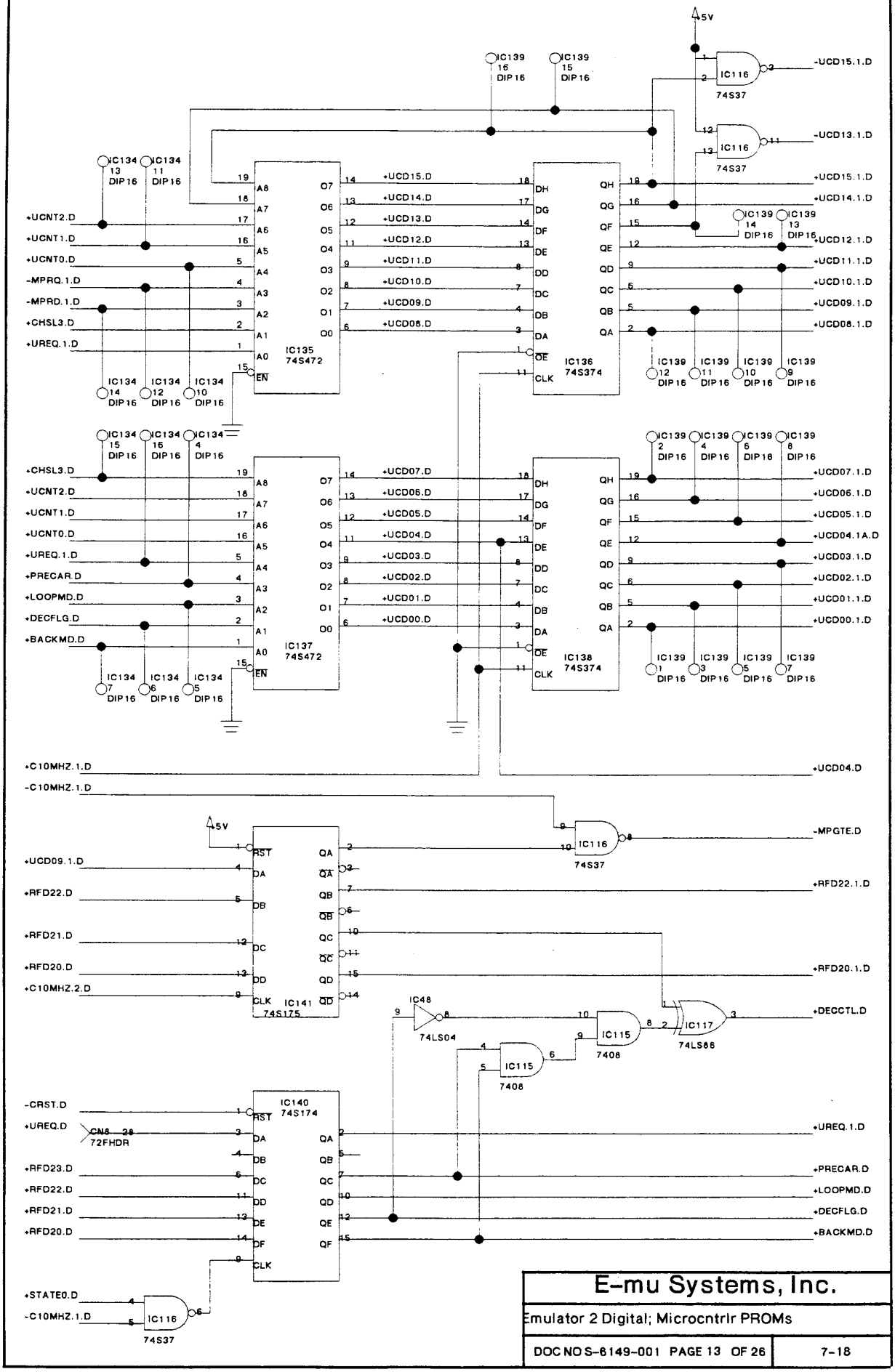


Note: Ground of 4070B to be AGND.

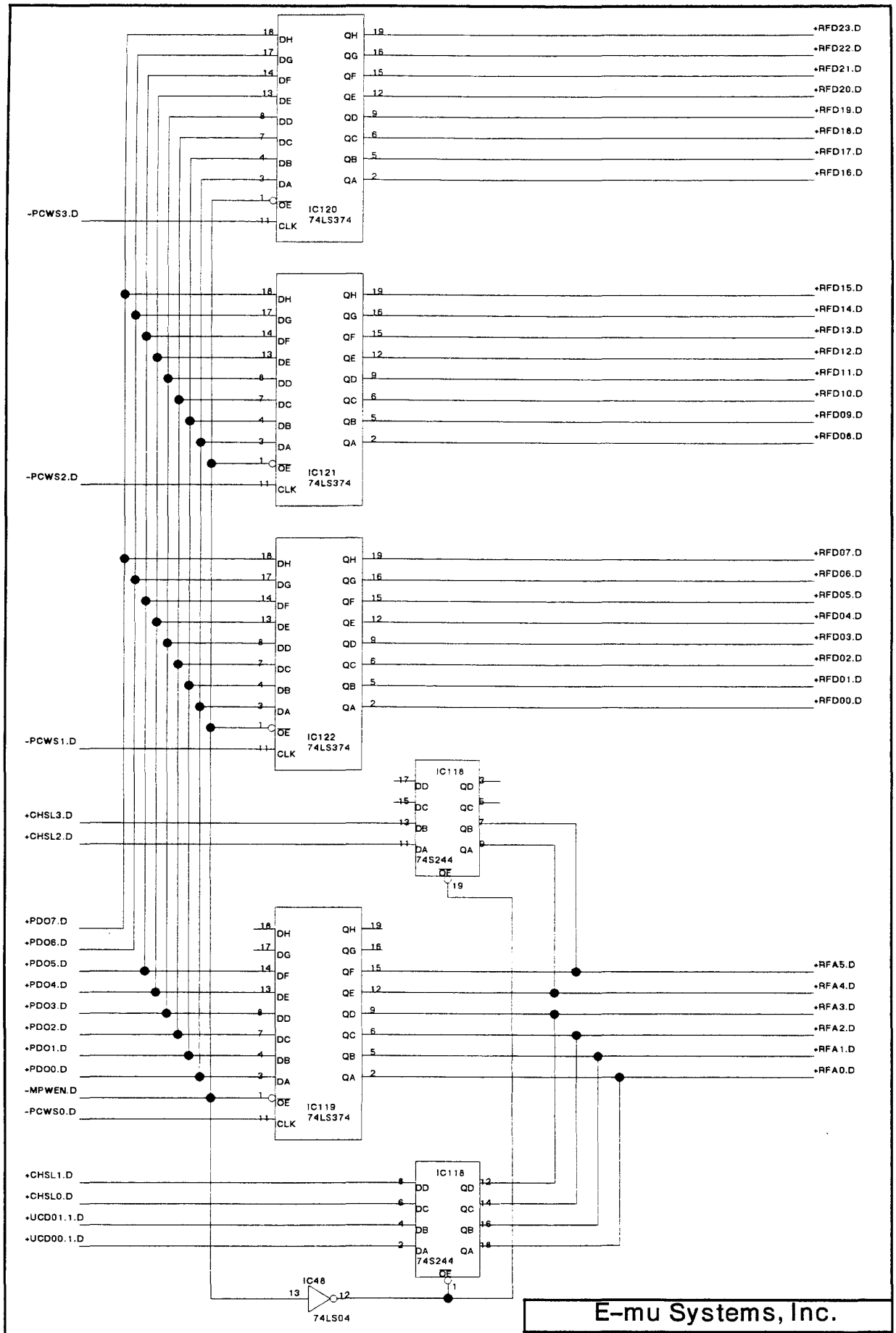
E-mu Systems, Inc.	
Emulator 2 Digital; Serial Interfaces	
DOC NO S-6149-001 PAGE 11 OF 26	7-16



E-mu Systems, Inc.	
Emulator 2 Digital; Microcntrlr State Ctr	
DOC NO S-6149-001 PAGE 12 OF 26	7-17

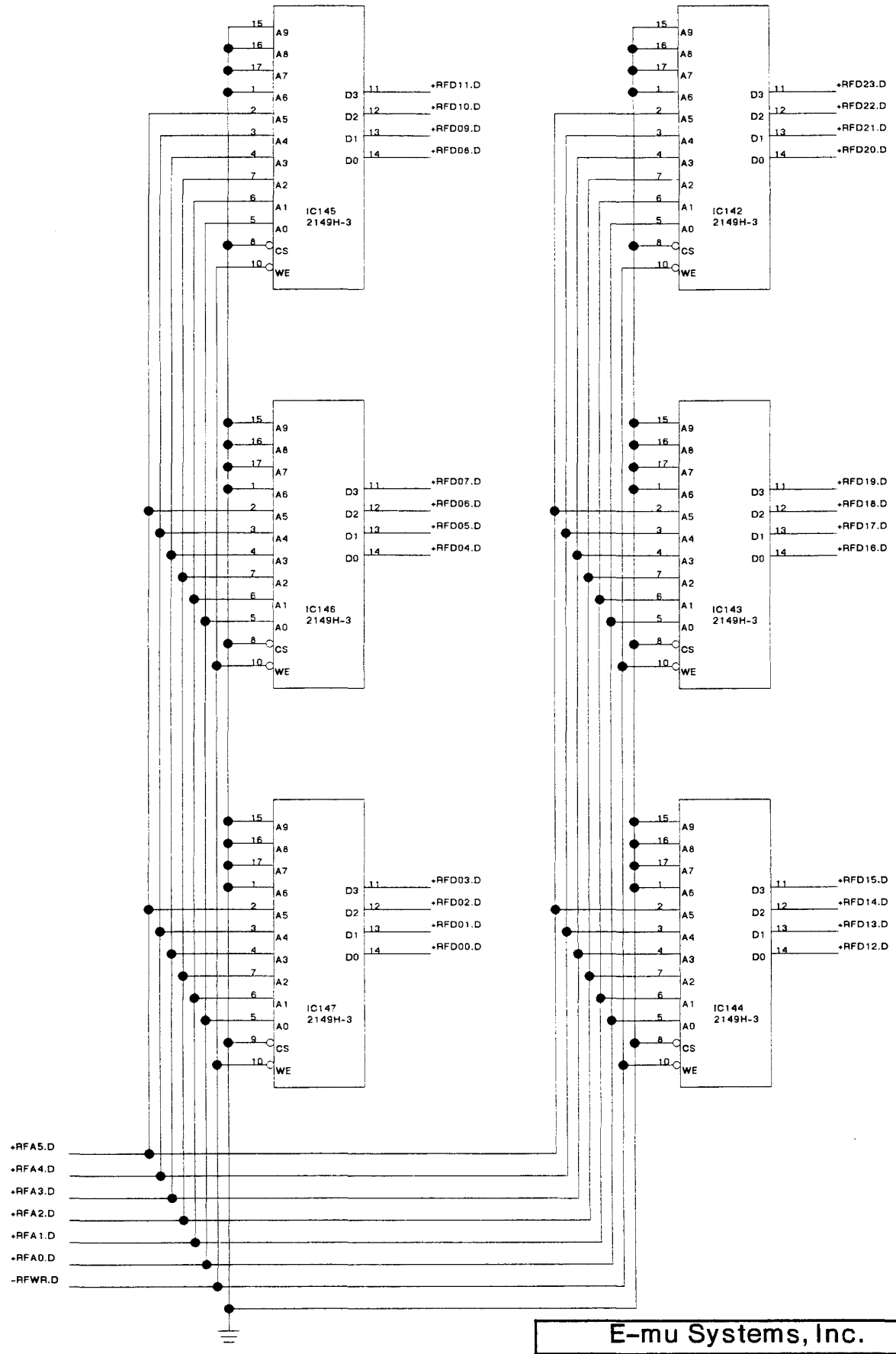


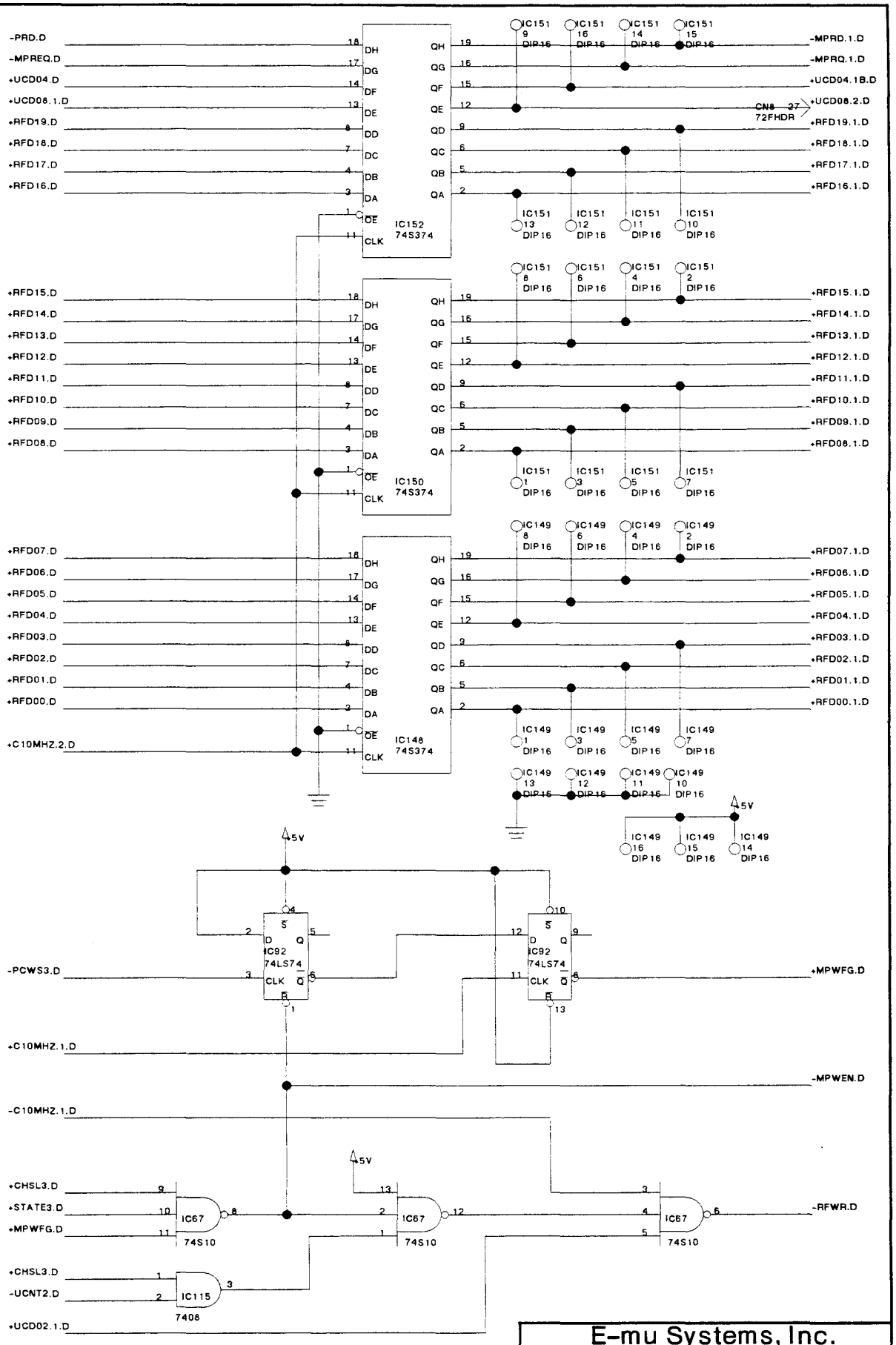
E-mu Systems, Inc.	
Emulator 2 Digital; Microcntrlr PROMs	
DOC NO S-6149-001 PAGE 13 OF 26	7-18



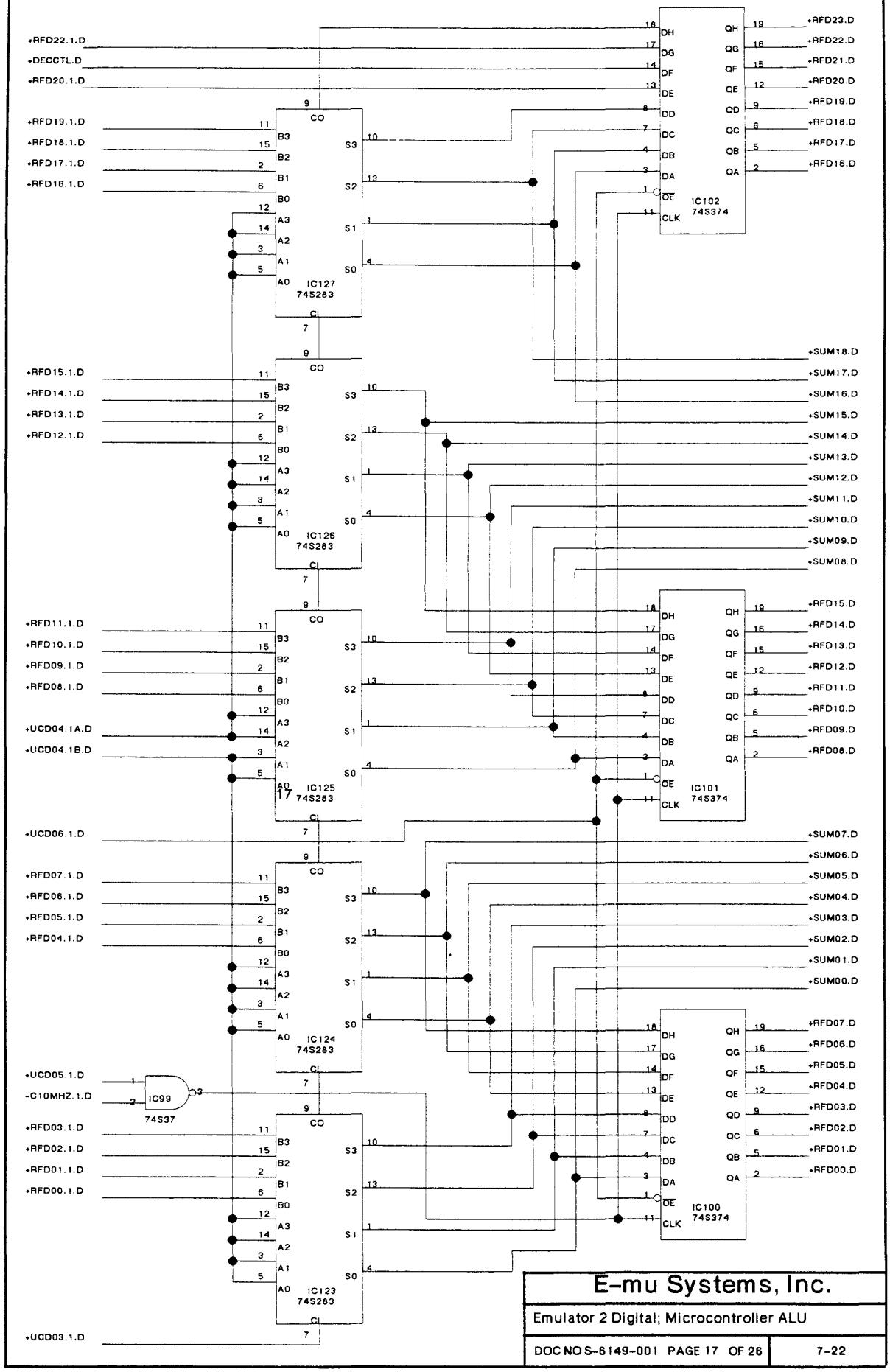
E-mu Systems, Inc.

Emulator 2 Digital; Microcntrlr/CPU Intrfc

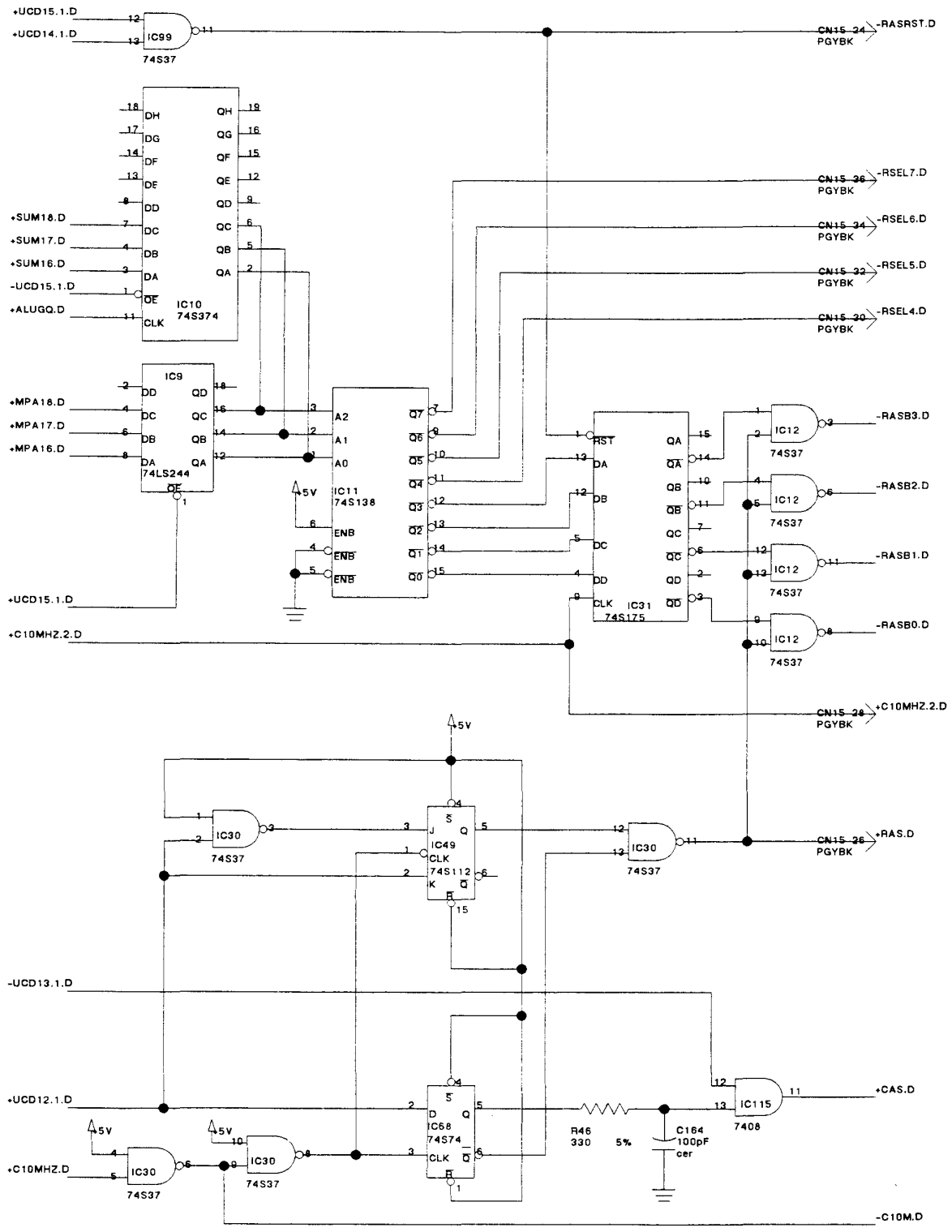

IC145
2149H-3
IC142
2149H-3
IC146
2149H-3
IC143
2149H-3
IC147
2149H-3
IC144
2149H-3
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CS
WE
D3
D2
D1
D0
+RFD11.D
+RFD10.D
+RFD09.D
+RFD08.D
+RFD23.D
+RFD22.D
+RFD21.D
+RFD20.D
+RFD07.D
+RFD06.D
+RFD05.D
+RFD04.D
+RFD19.D
+RFD18.D
+RFD17.D
+RFD16.D
+RFD03.D
+RFD02.D
+RFD01.D
+RFD00.D
+RFD15.D
+RFD14.D
+RFD13.D
+RFD12.D
+RFA5.D
+RFA4.D
+RFA3.D
+RFA2.D
+RFA1.D
+RFA0.D
-RFWR.D



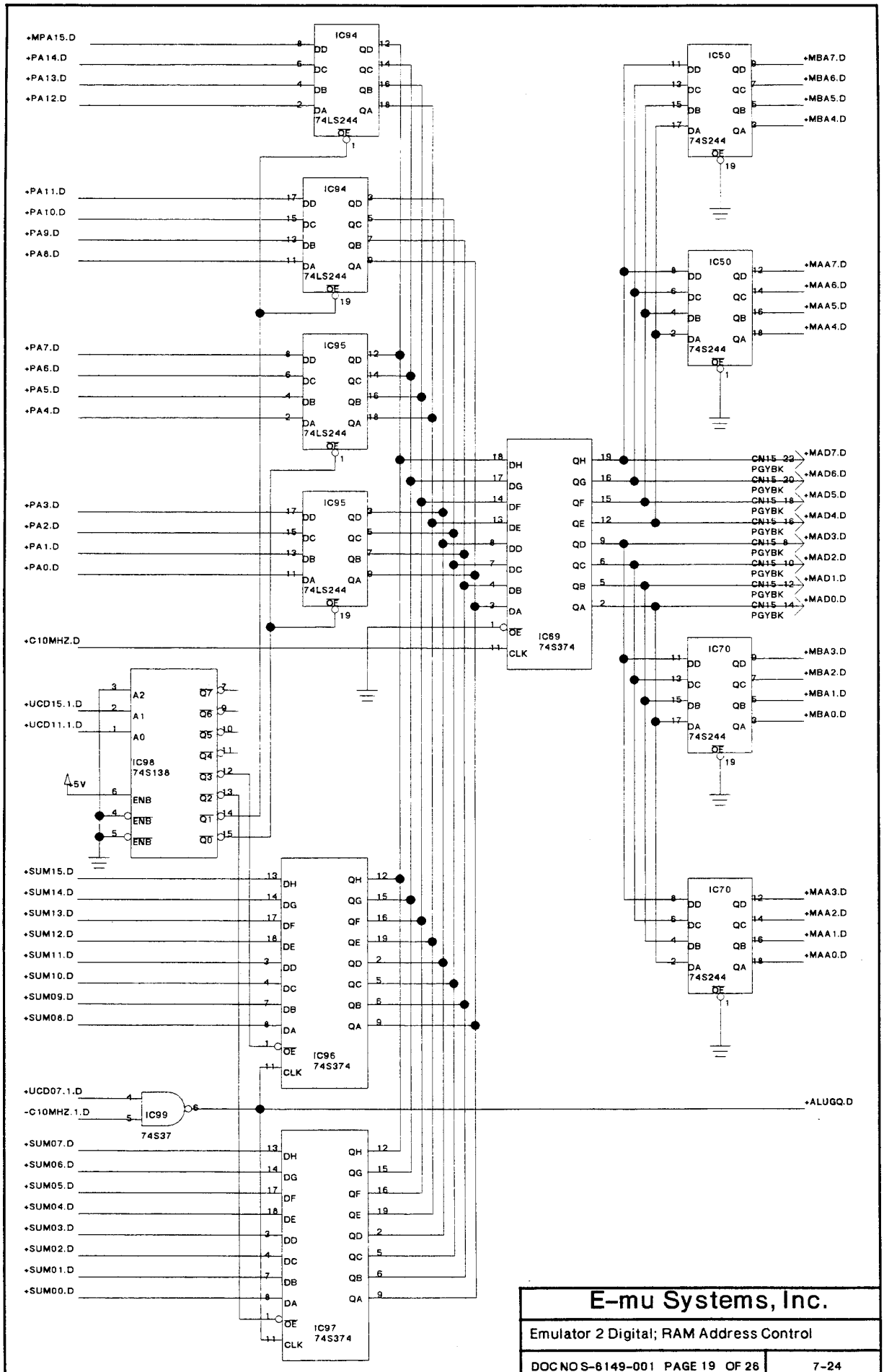
E-mu Systems, Inc.	
Emulator 2 Digital; Microcntrlr Pipeline	
DOC NO S-6149-001 PAGE 16 OF 26	7-21



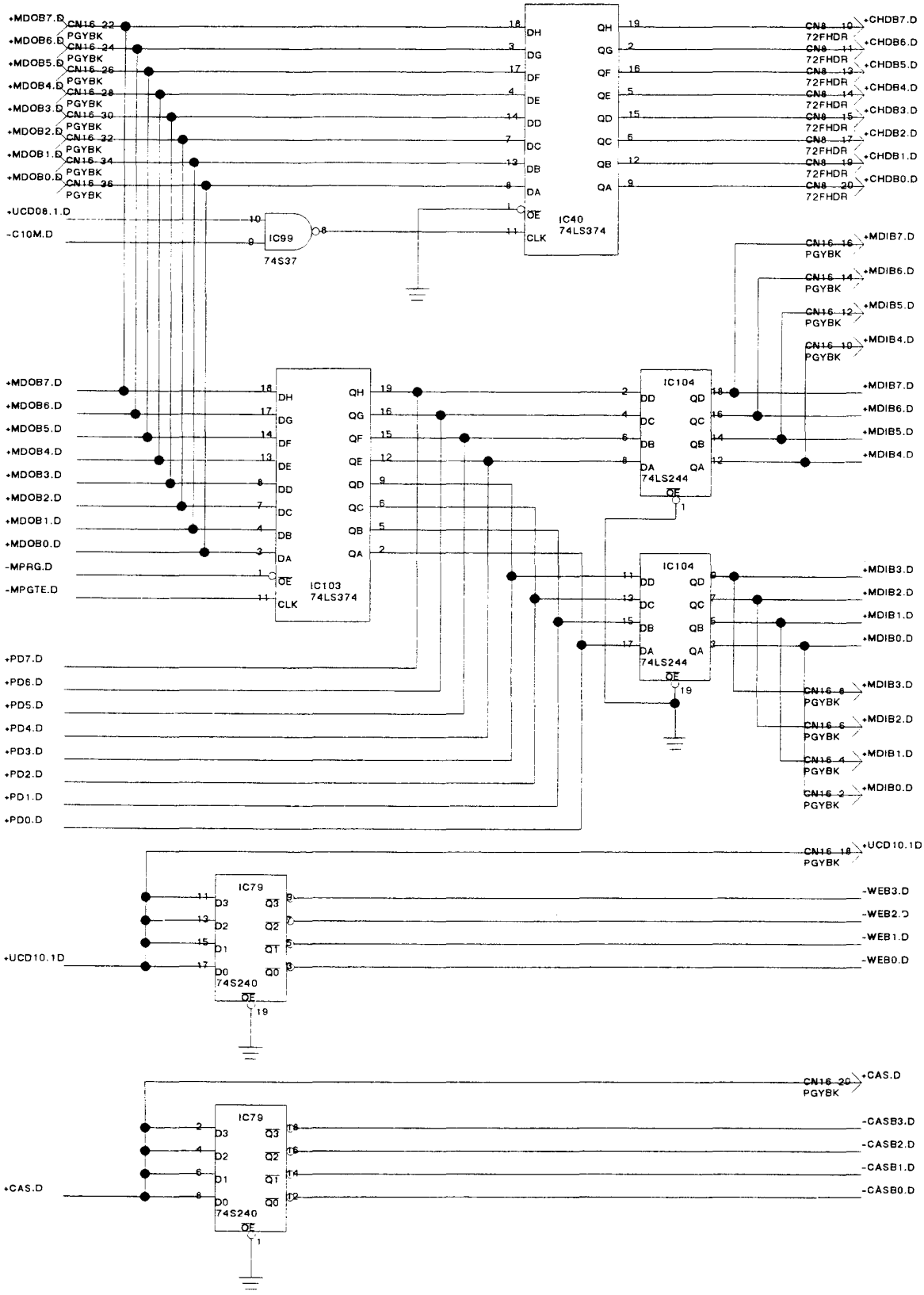
E-mu Systems, Inc.	
Emulator 2 Digital; Microcontroller ALU	
DOC NO S-6149-001 PAGE 17 OF 26	7-22



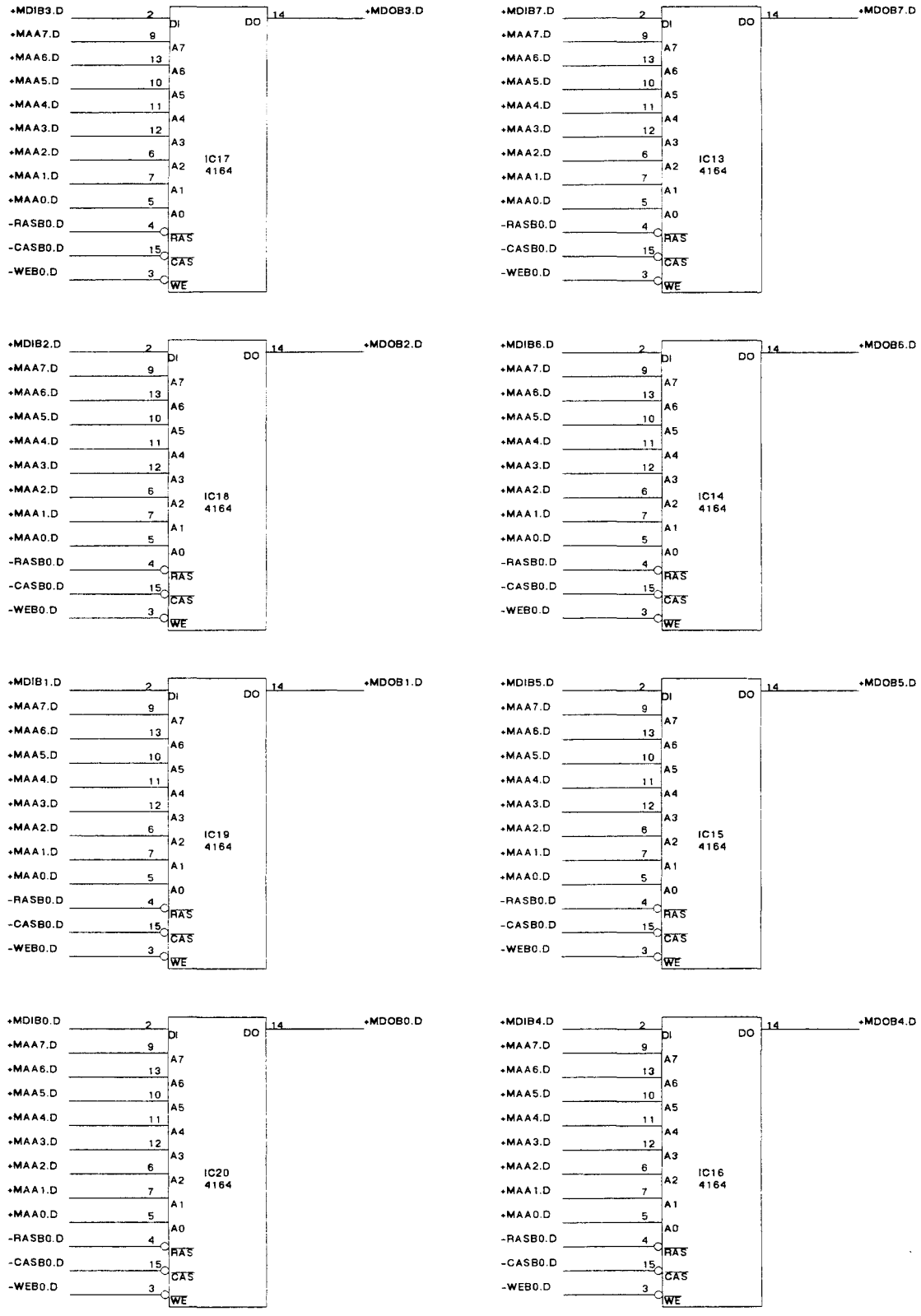
E-mu Systems, Inc.	
Emulator 2 Digital; RAM Timing	
DOC NO S-6149-001 PAGE 18 OF 26	7-23



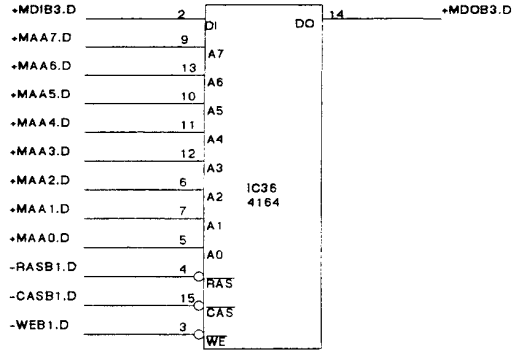
E-mu Systems, Inc.	
Emulator 2 Digital; RAM Address Control	
DOC NO S-6149-001 PAGE 19 OF 28	7-24

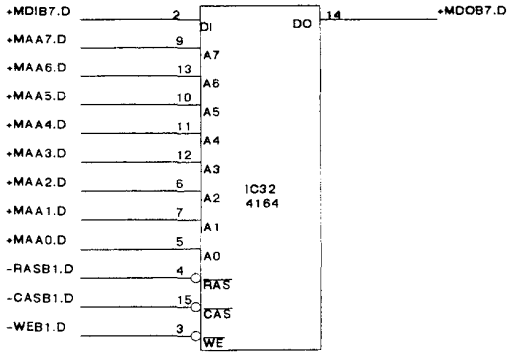


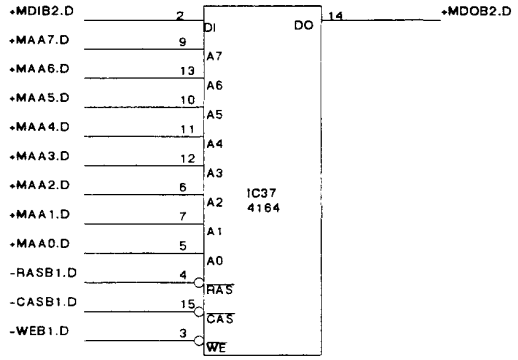
E-mu Systems, Inc.	
Emulator 2 Digital; RAM Buffering	
DOC NO S-6149-001 PAGE 20 OF 26	7-25

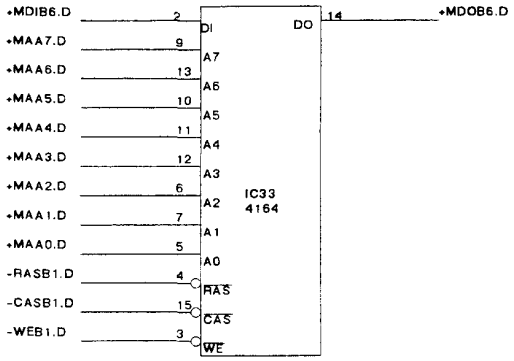


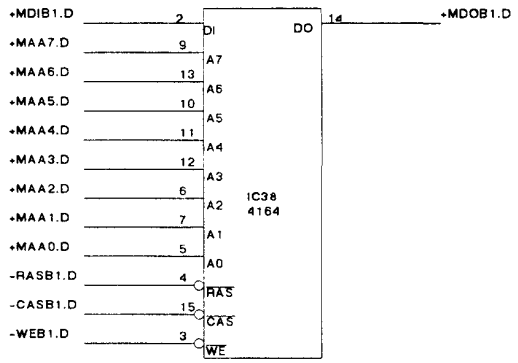
E-mu Systems, Inc.	
Emulator 2 Digital; Dynamic RAM	
DOC NO S-6149-001 PAGE 21 OF 26	7-26

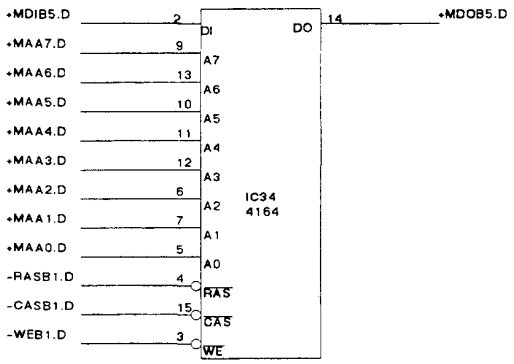

+MDIB3.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC36
4164
DO
+MDOB3.D

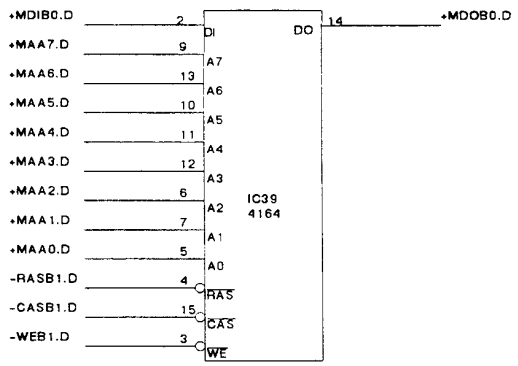

+MDIB7.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC32
4164
DO
+MDOB7.D

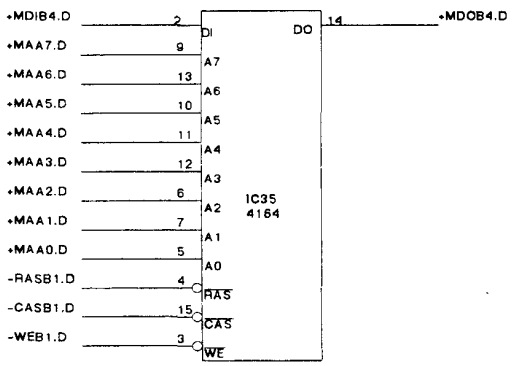

+MDIB2.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC37
4164
DO
+MDOB2.D

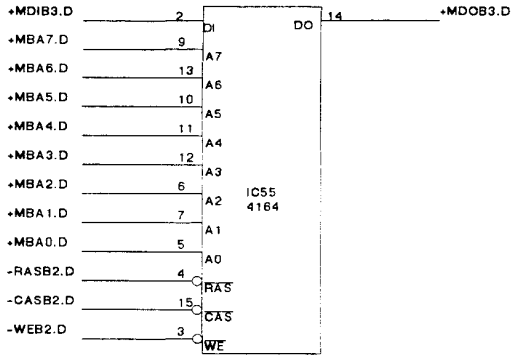

+MDIB6.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC33
4164
DO
+MDOB6.D

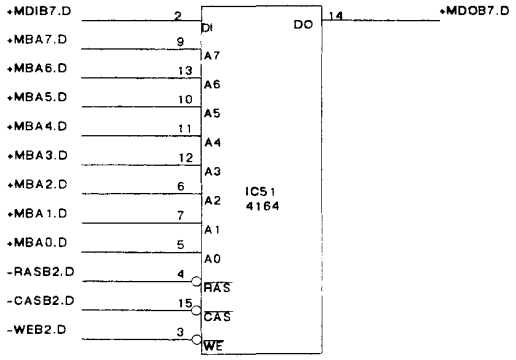

+MDIB1.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC38
4164
DO
+MDOB1.D

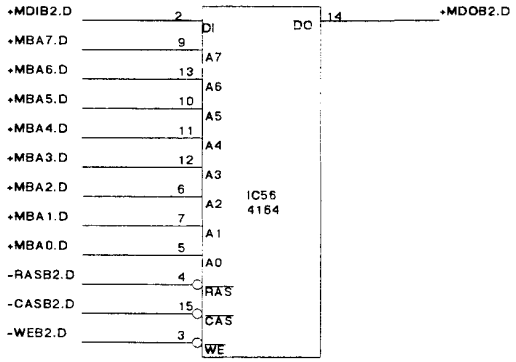

+MDIB5.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC34
4164
DO
+MDOB5.D

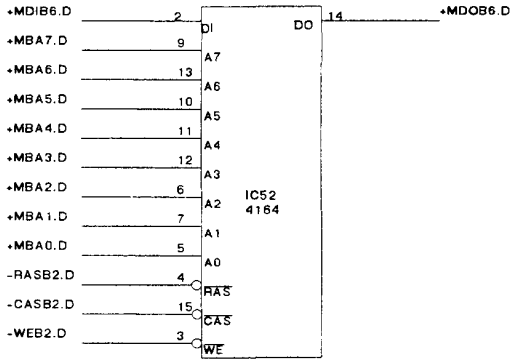

+MDIB0.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC39
4164
DO
+MDOB0.D

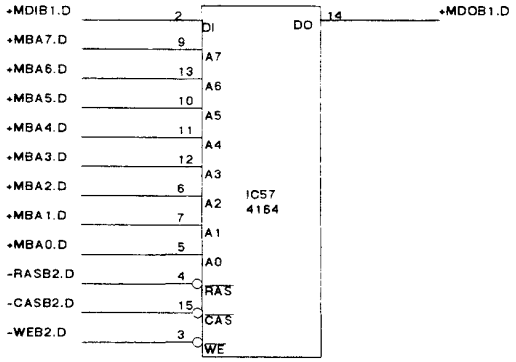

+MDIB4.D
+MAA7.D
+MAA6.D
+MAA5.D
+MAA4.D
+MAA3.D
+MAA2.D
+MAA1.D
+MAA0.D
-RASB1.D
-CASB1.D
-WEB1.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC35
4164
DO
+MDOB4.D

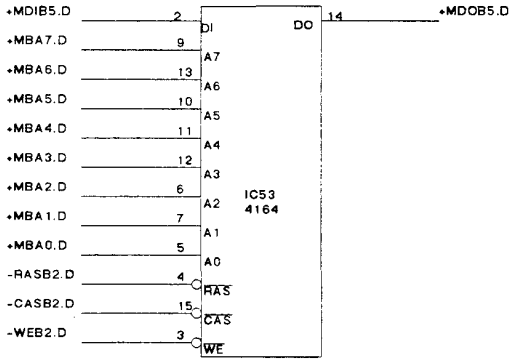

+MDIB3.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC55
4164
DO
+MDOB3.D

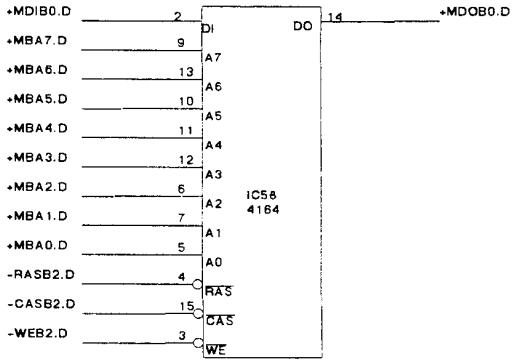

+MDIB7.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC51
4164
DO
+MDOB7.D

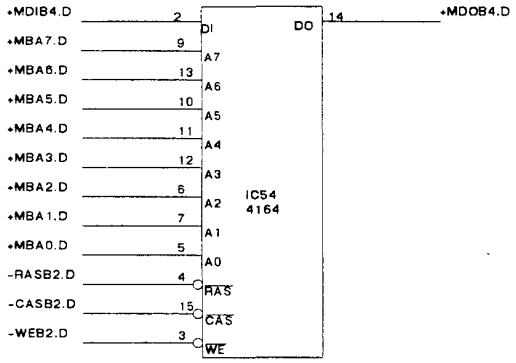

+MDIB2.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC56
4164
DO
+MDOB2.D

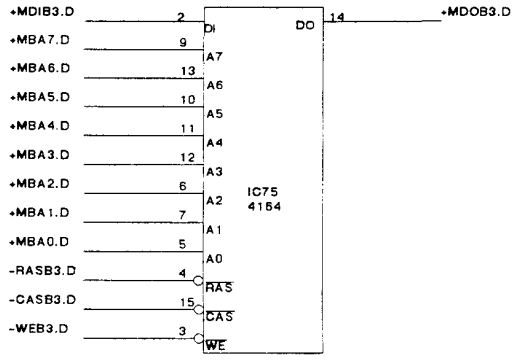

+MDIB6.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC52
4164
DO
+MDOB6.D

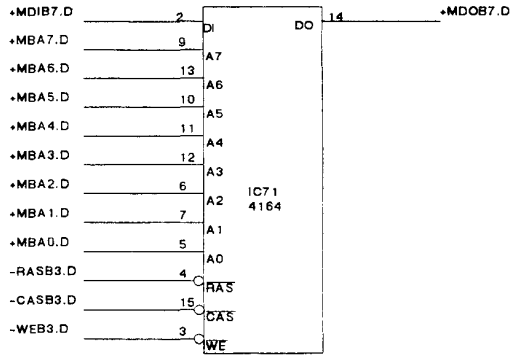

+MDIB1.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC57
4164
DO
+MDOB1.D

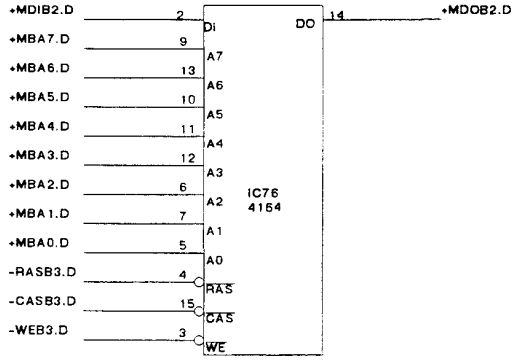

+MDIB5.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC53
4164
DO
+MDOB5.D

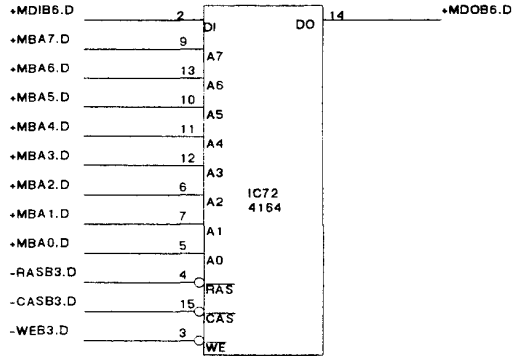

+MDIB0.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC58
4164
DO
+MDOB0.D

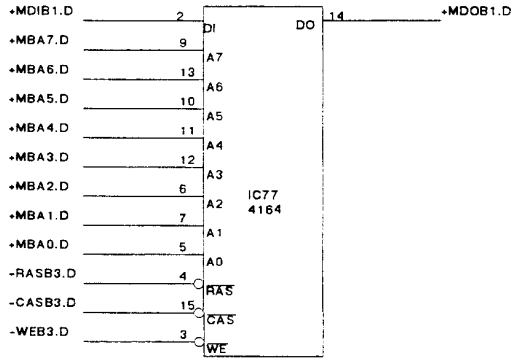

+MDIB4.D
+MBA7.D
+MBA6.D
+MBA5.D
+MBA4.D
+MBA3.D
+MBA2.D
+MBA1.D
+MBA0.D
-RASB2.D
-CASB2.D
-WEB2.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC54
4164
DO
+MDOB4.D

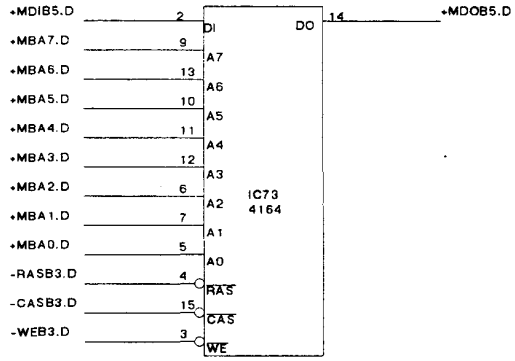


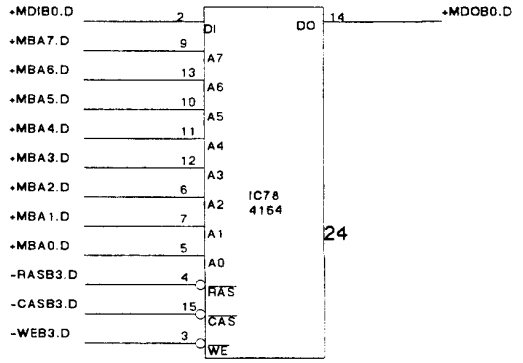


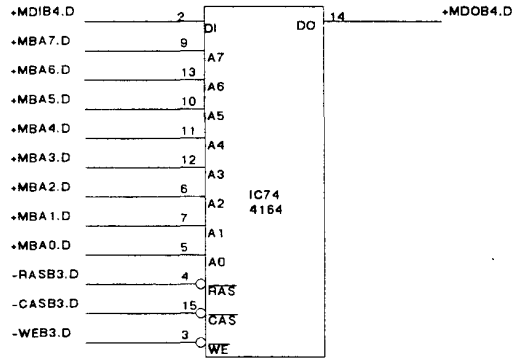












E-mu Systems, Inc.	
Emulator 2 Digital; Dynamic RAM	
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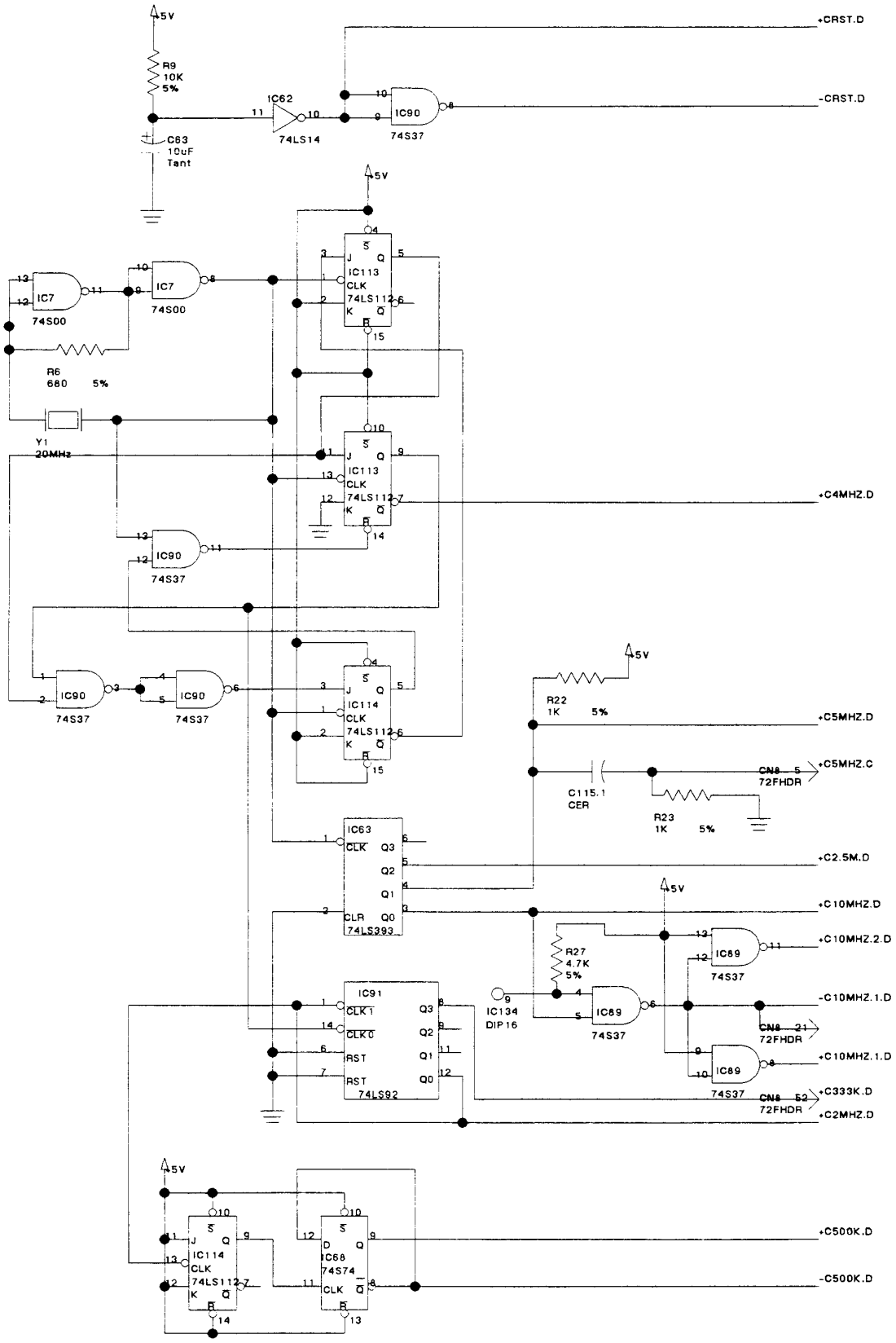
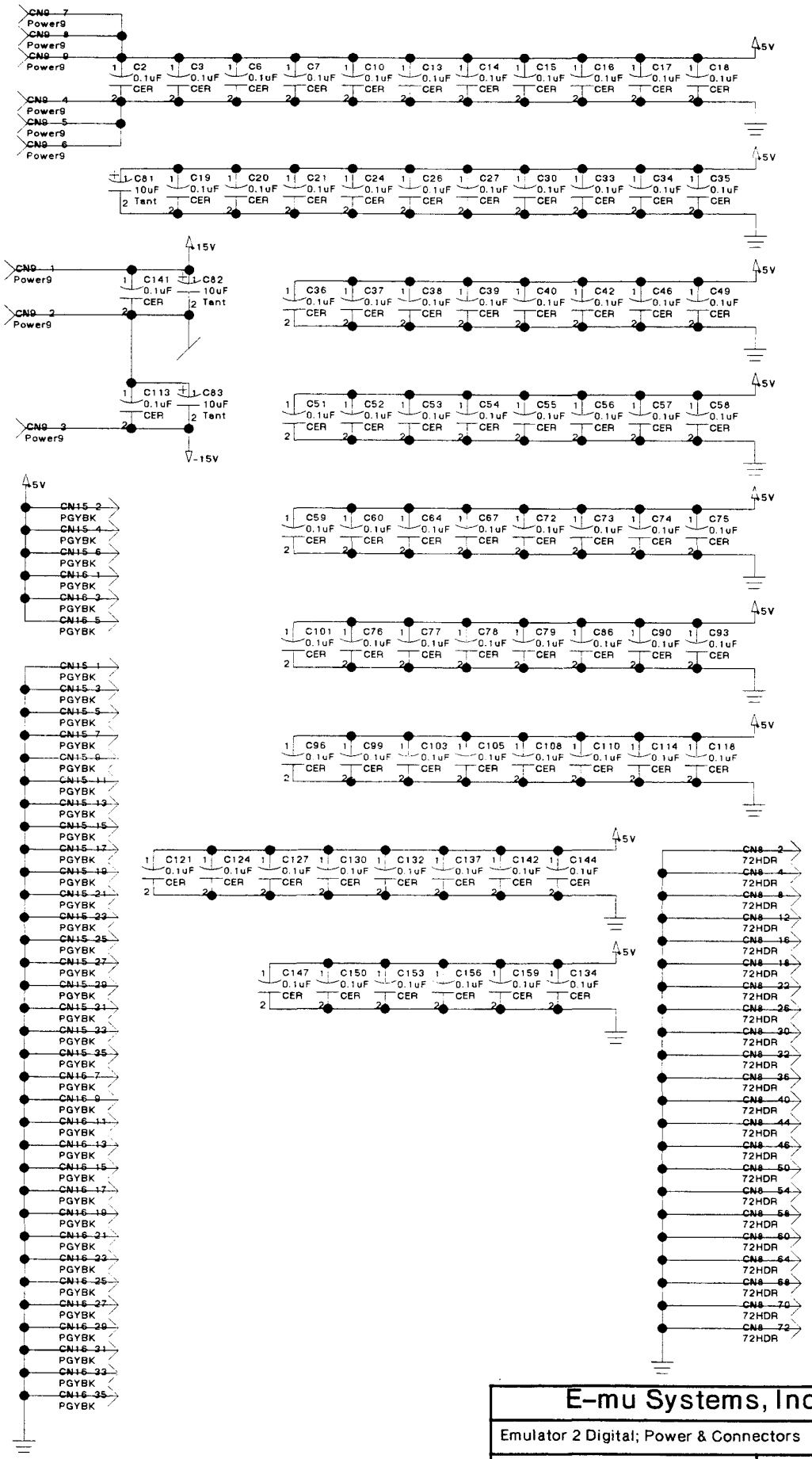


E-mu Systems, Inc.	
Emulator 2 Digital; Clocks & Reset	
DOC NO S-6149-001 PAGE 25 OF 26	7-30



E-mu Systems, Inc.	
Emulator 2 Digital; Power & Connectors	
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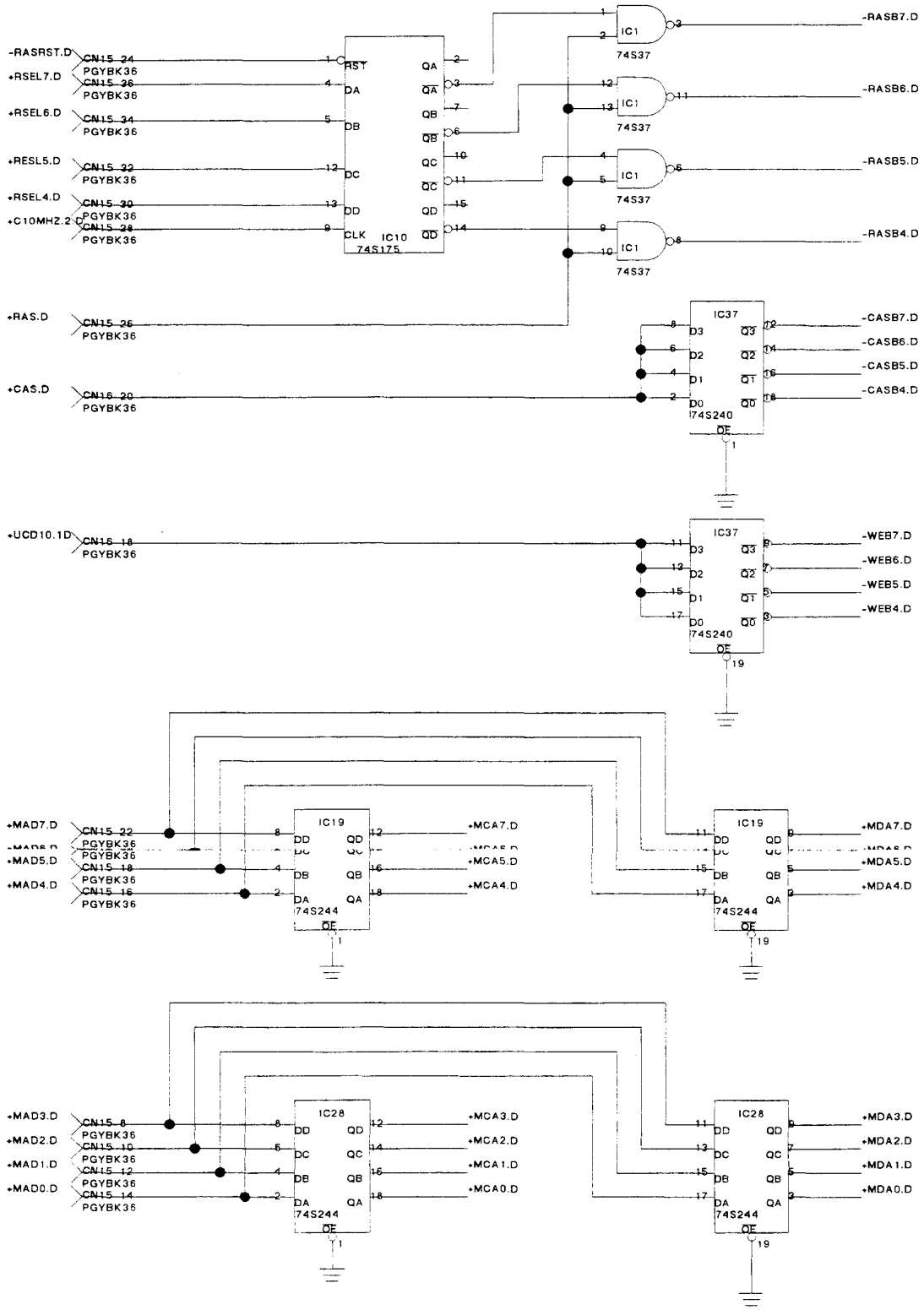

E-mu Systems, Inc.

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Emulator 2 Memory Option

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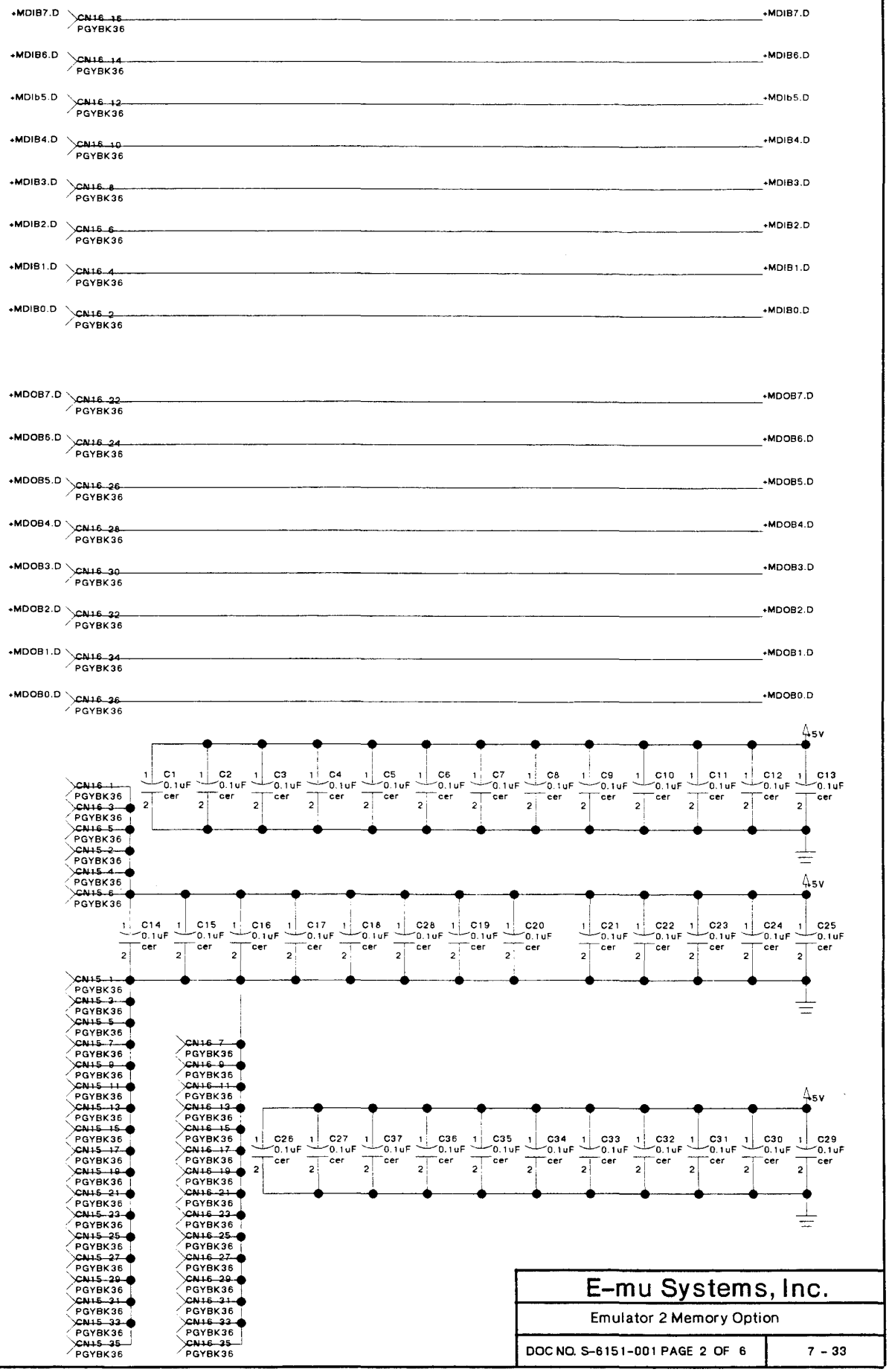
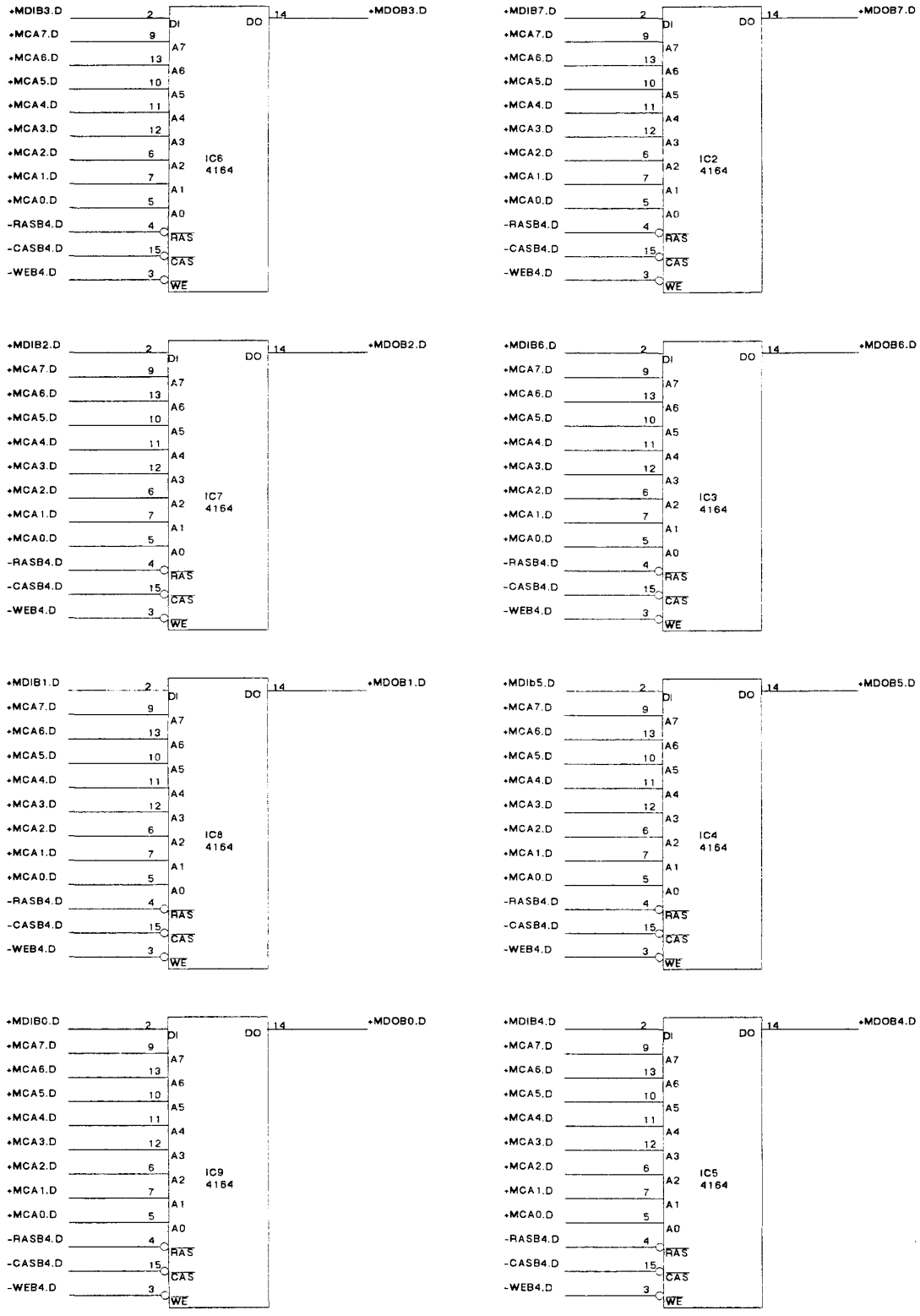
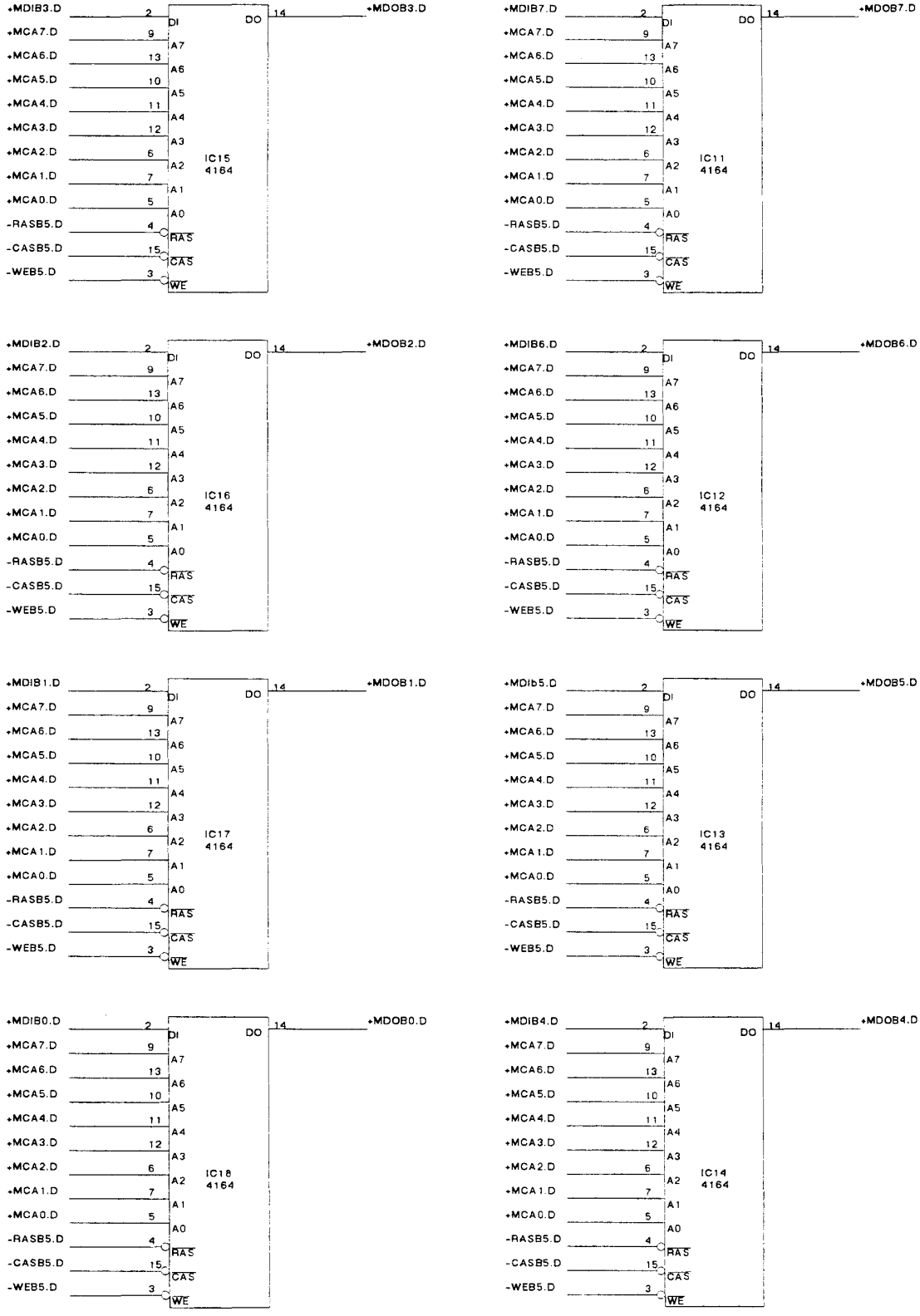
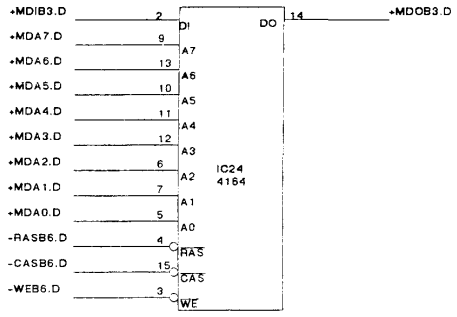
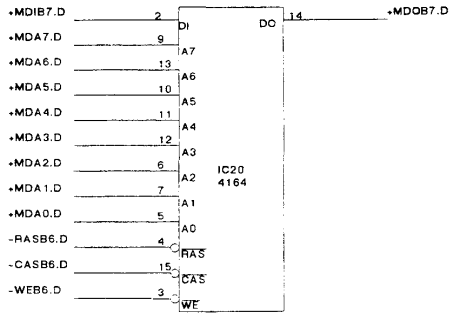


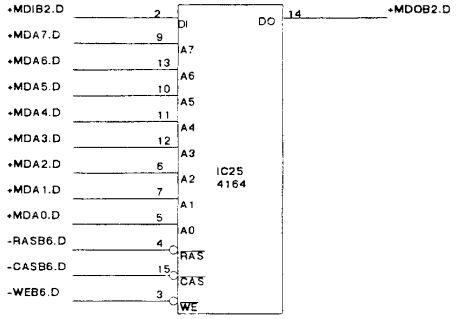
E-mu Systems, Inc.	
Emulator 2 Memory Option	
DOC NO. S-6151-001 PAGE 2 OF 6	7 - 33

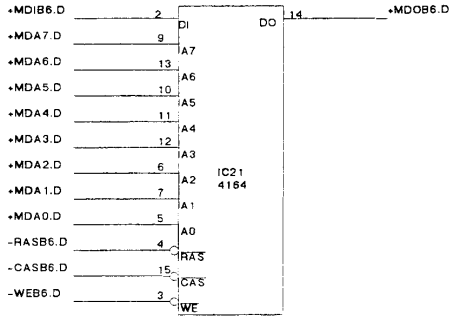

+MDIB3.D
+MCA7.D
+MCA6.D
+MCA5.D
+MCA4.D
+MCA3.D
+MCA2.D
+MCA1.D
+MCA0.D
-RASB4.D
-CASB4.D
-WEB4.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC6
4164
+MDOB3.D
+MDIB7.D
IC2
4164
+MDOB7.D
+MDIB2.D
IC7
4164
+MDOB2.D
+MDIB6.D
IC3
4164
+MDOB6.D
+MDIB1.D
IC8
4164
+MDOB1.D
+MDIb5.D
IC4
4164
+MDOB5.D
+MDIB0.D
IC9
4164
+MDOB0.D
+MDIB4.D
IC5
4164
+MDOB4.D

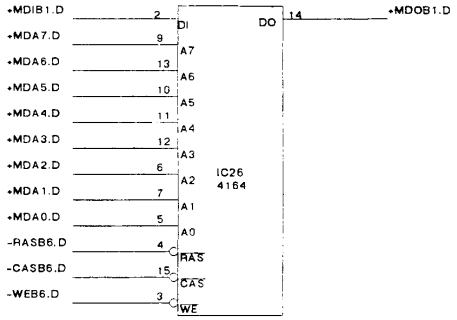

+MDIB3.D
+MCA7.D
+MCA6.D
+MCA5.D
+MCA4.D
+MCA3.D
+MCA2.D
+MCA1.D
+MCA0.D
-RASB5.D
-CASB5.D
-WEB5.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC15
4164
+MDOB3.D
+MDIB7.D
IC11
4164
+MDOB7.D
+MDIB2.D
IC16
4164
+MDOB2.D
+MDIB6.D
IC12
4164
+MDOB6.D
+MDIB1.D
IC17
4164
+MDOB1.D
+MDIb5.D
IC13
4164
+MDOB5.D
+MDIB0.D
IC18
4164
+MDOB0.D
+MDIB4.D
IC14
4164
+MDOB4.D

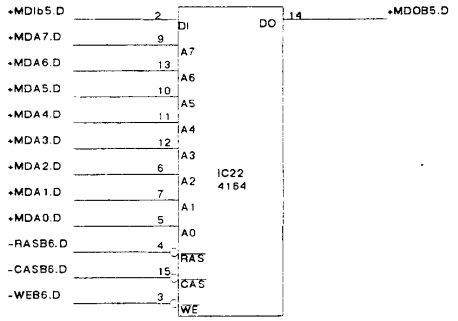

+MDIB3.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC24
4164
+MDOB3.D

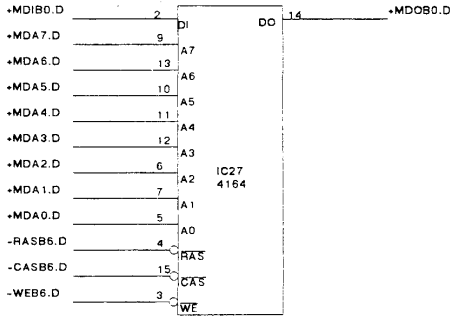

+MDIB7.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC20
4164
+MDOB7.D

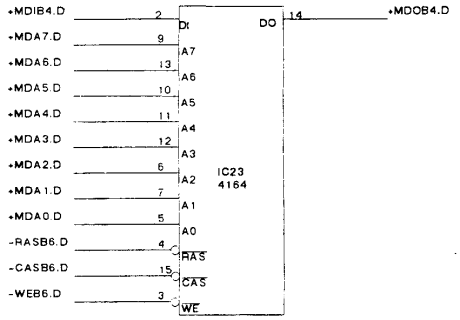

+MDIB2.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC25
4164
+MDOB2.D

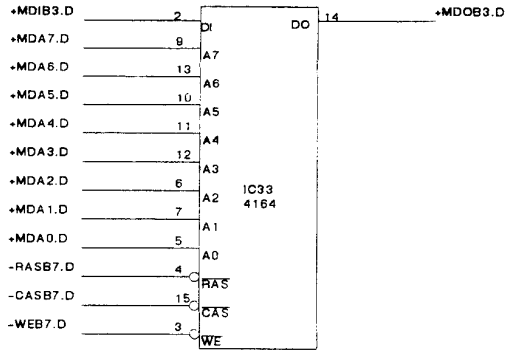

+MDIB6.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC21
4164
+MDOB6.D

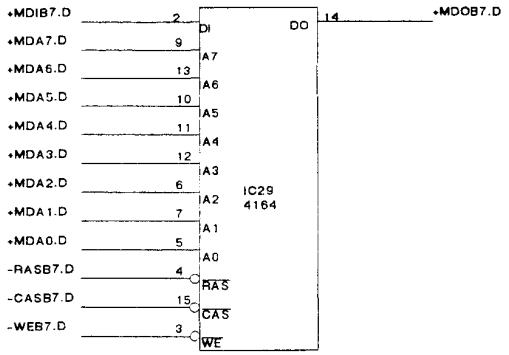

+MDIB1.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC26
4164
+MDOB1.D

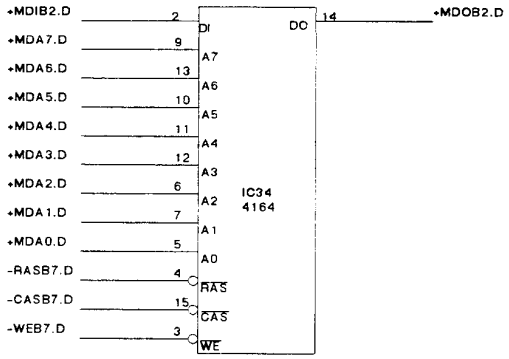

+MDIb5.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC22
4164
+MDOB5.D

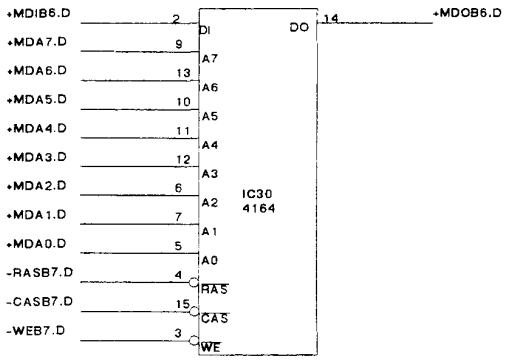

+MDIB0.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC27
4164
+MDOB0.D

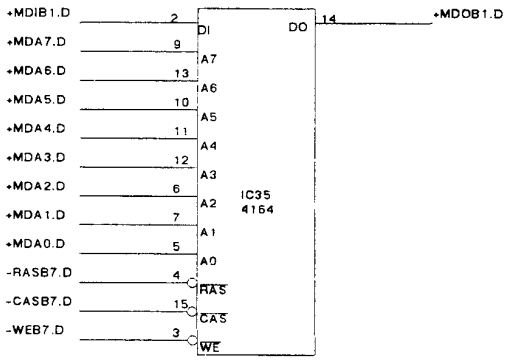

+MDIB4.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB6.D
-CASB6.D
-WEB6.D
DI
DO
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
IC23
4164
+MDOB4.D

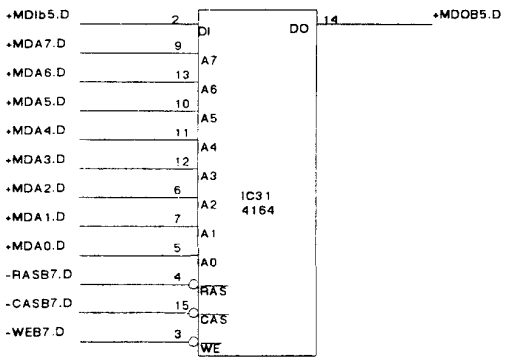

+MDIB3.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC33
4164
+MDOB3.D

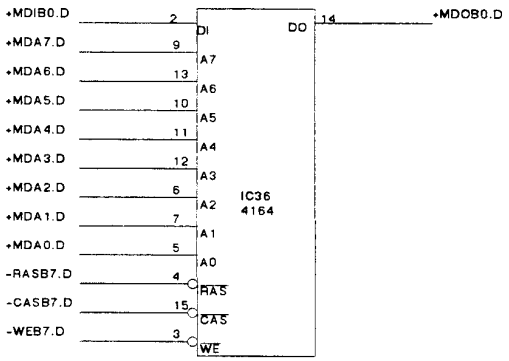

+MDIB7.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC29
4164
+MDOB7.D

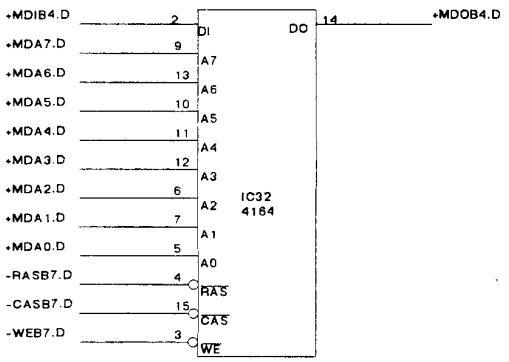

+MDIB2.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC34
4164
+MDOB2.D

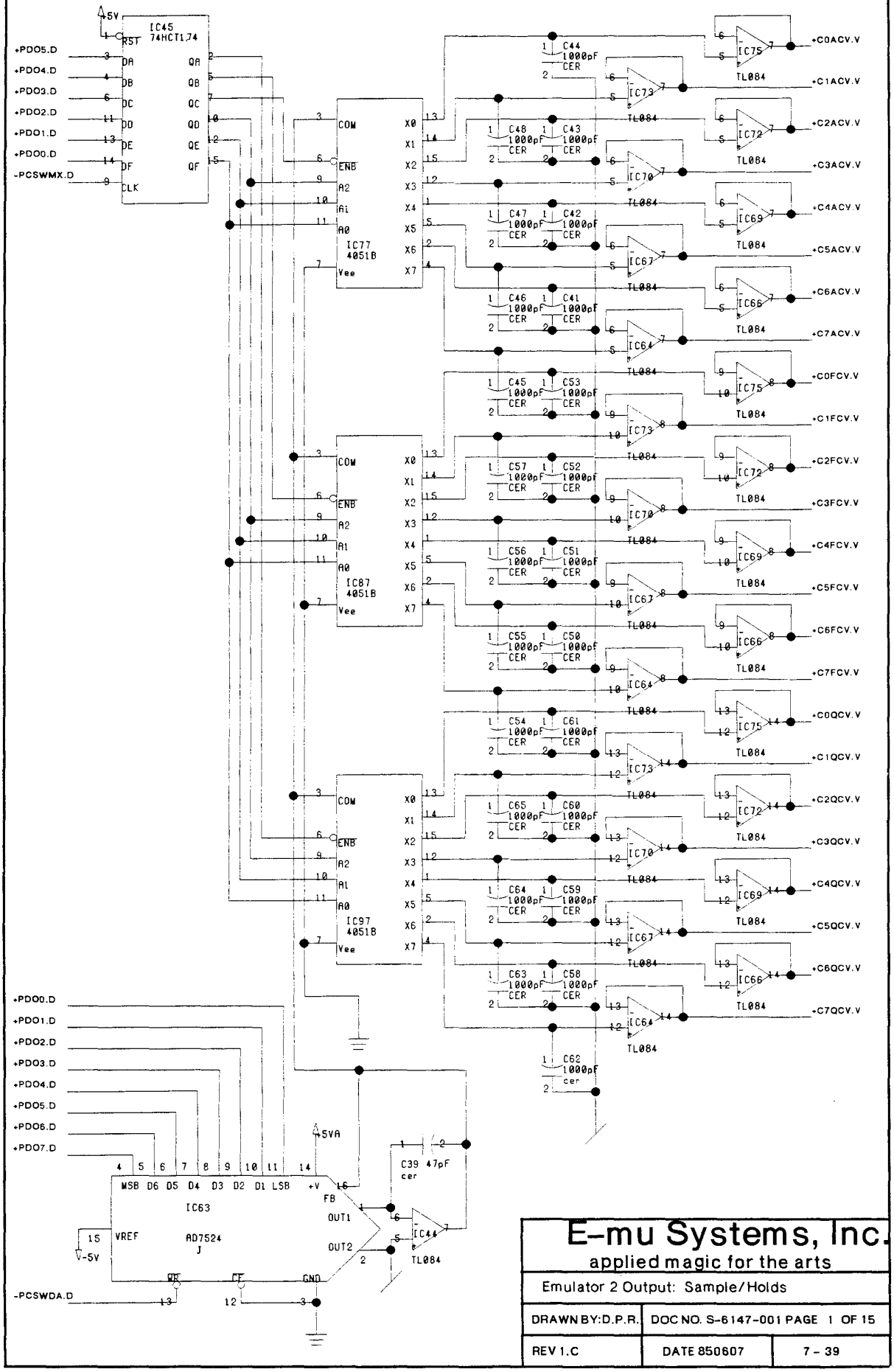

+MDIB6.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC30
4164
+MDOB6.D


+MDIB1.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC35
4164
+MDOB1.D


+MDIb5.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC31
4164
+MDOB5.D


+MDIB0.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC36
4164
+MDOB0.D


+MDIB4.D
+MDA7.D
+MDA6.D
+MDA5.D
+MDA4.D
+MDA3.D
+MDA2.D
+MDA1.D
+MDA0.D
-RASB7.D
-CASB7.D
-WEB7.D
DI
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DO
IC32
4164
+MDOB4.D



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Emulator 2 Output: Sample/Holds

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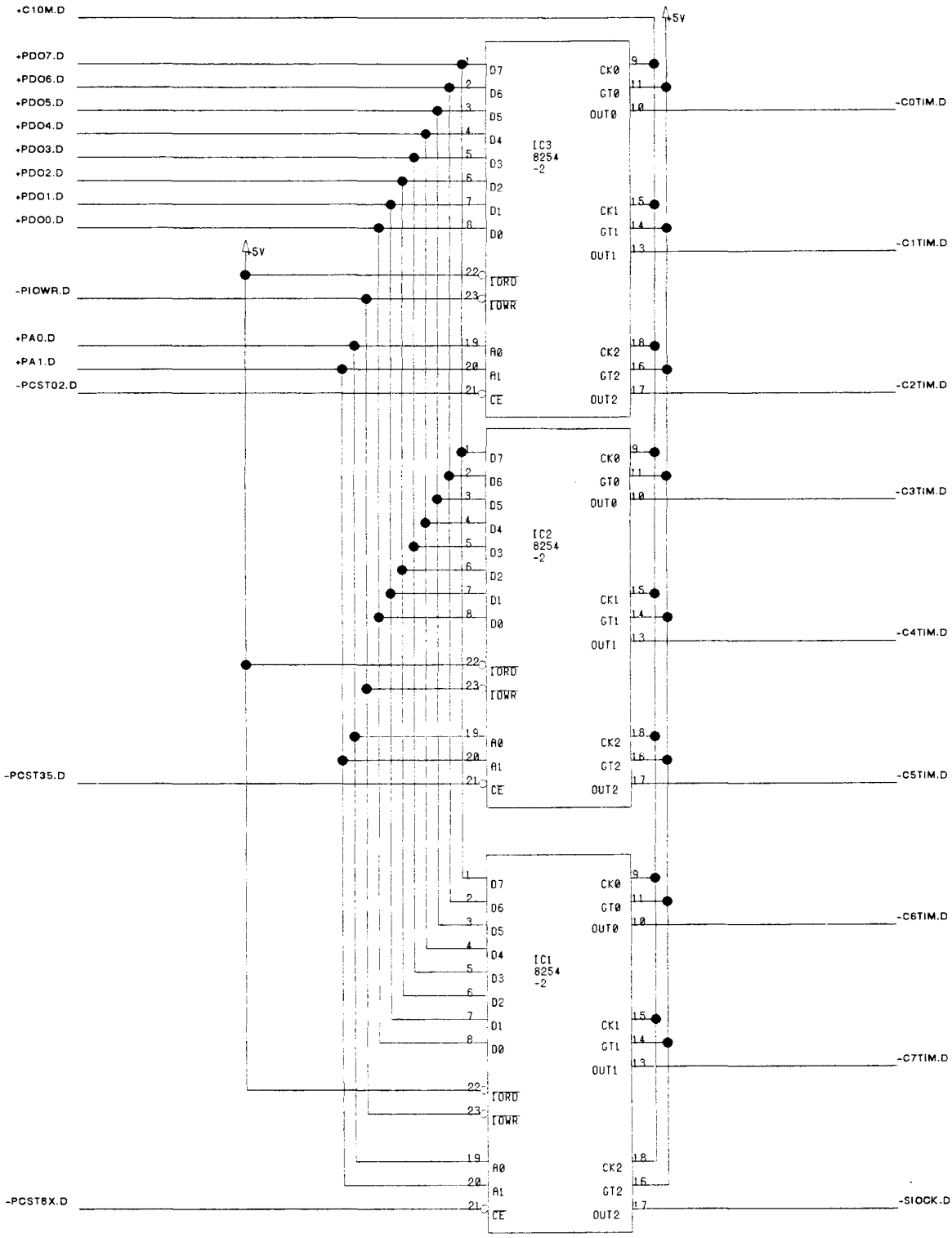

E-mu Systems, Inc.	
Emulator 2 Output: Timers	
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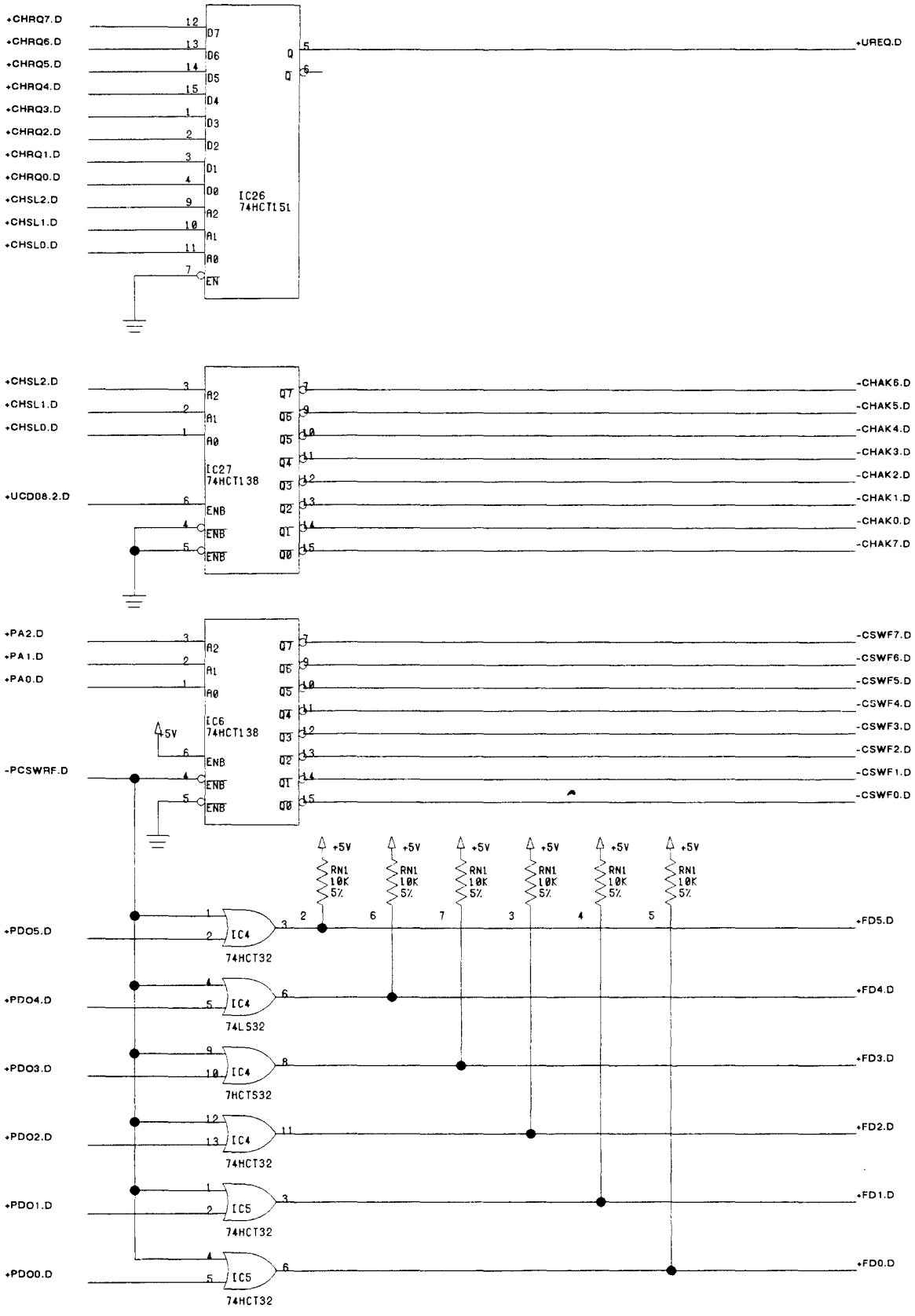

E-mu Systems, Inc.	
Emualtor 2 Output: RQ/AK, Filter Sel	
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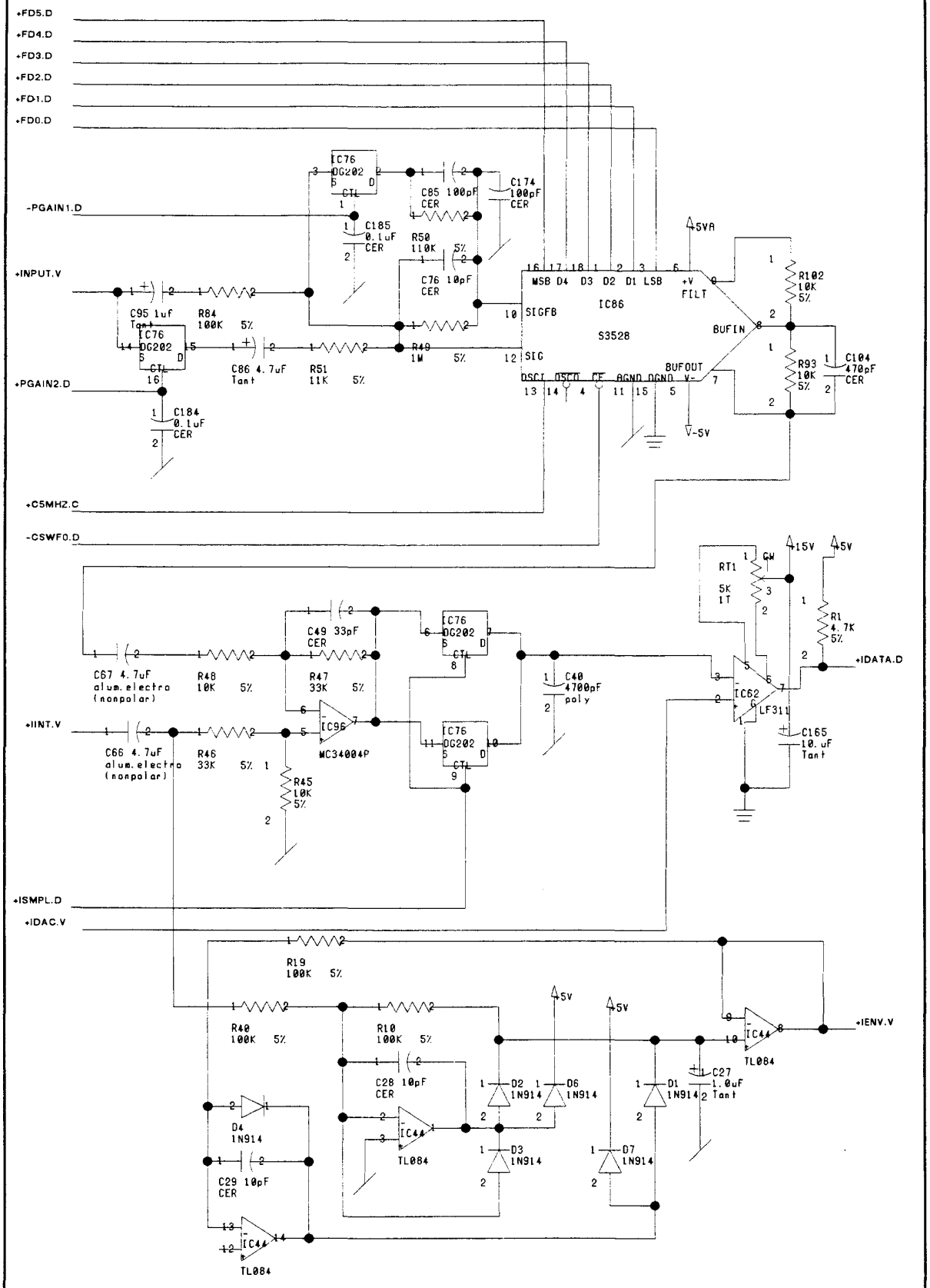

E-mu Systems, Inc.	
Emulator 2 Output: Input Analog	
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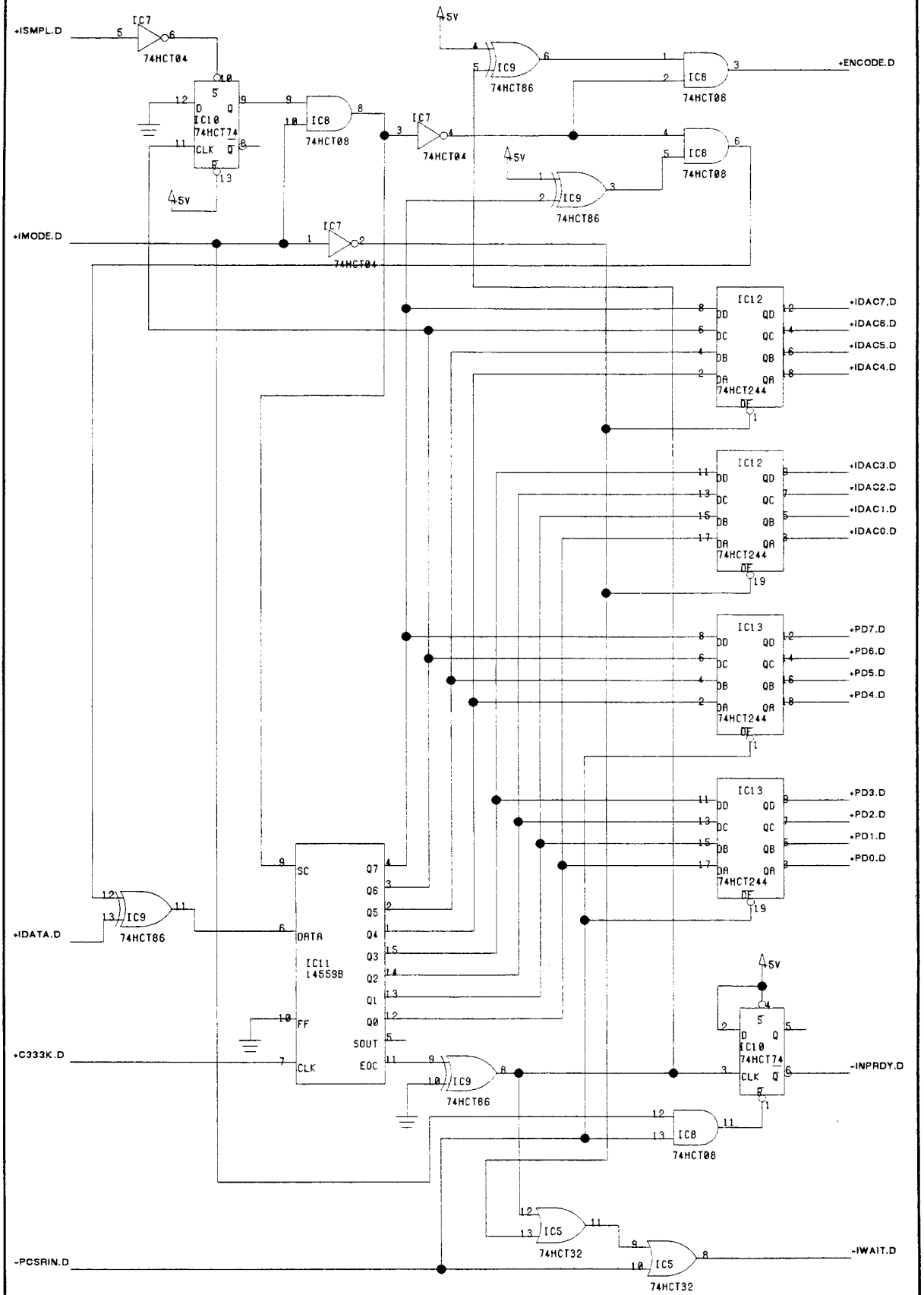

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Emulator 2 Output: SAR and logic	
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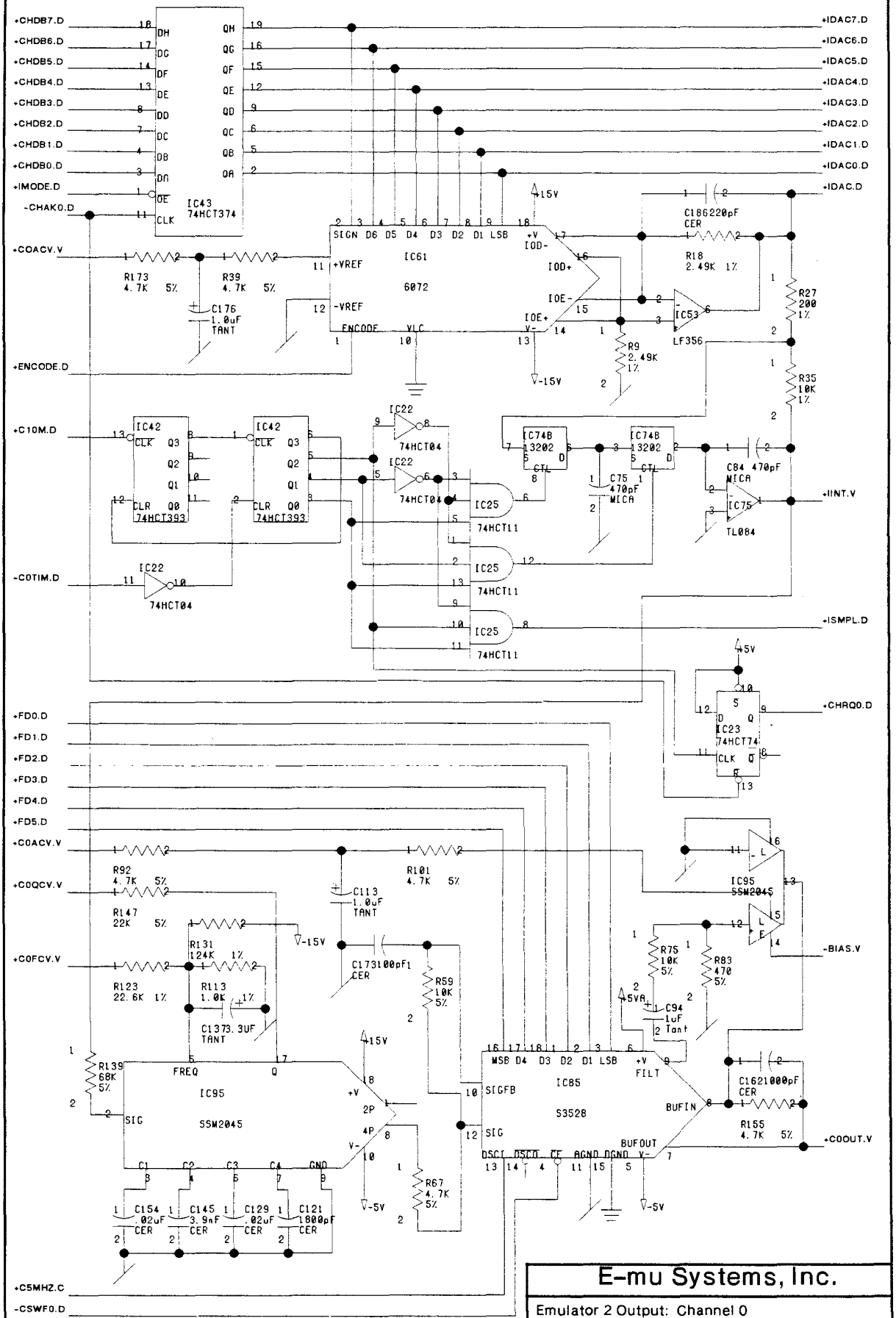
NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN



E-mu Systems, Inc.	
Emulator 2 Output: Channel 0	
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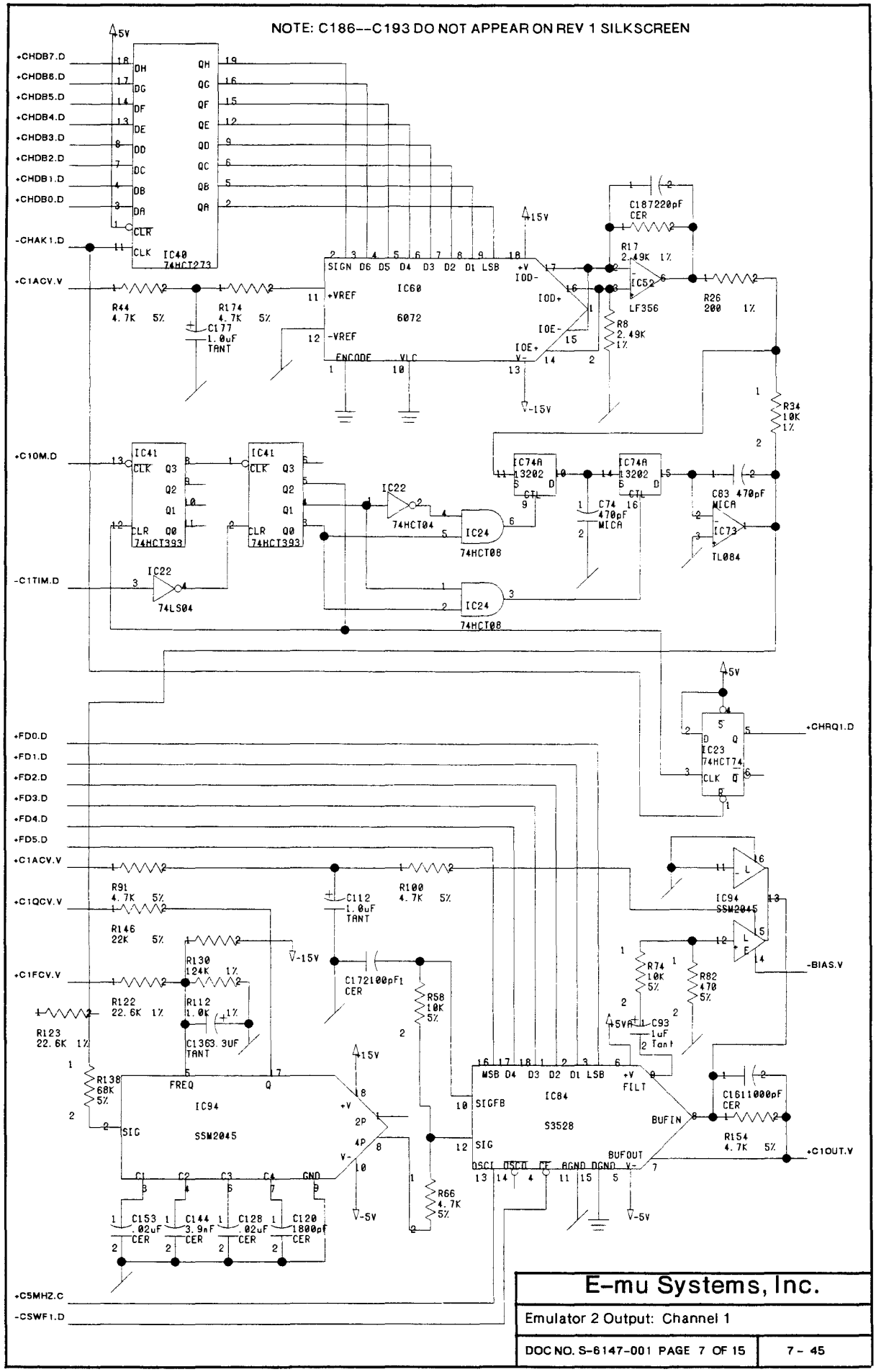
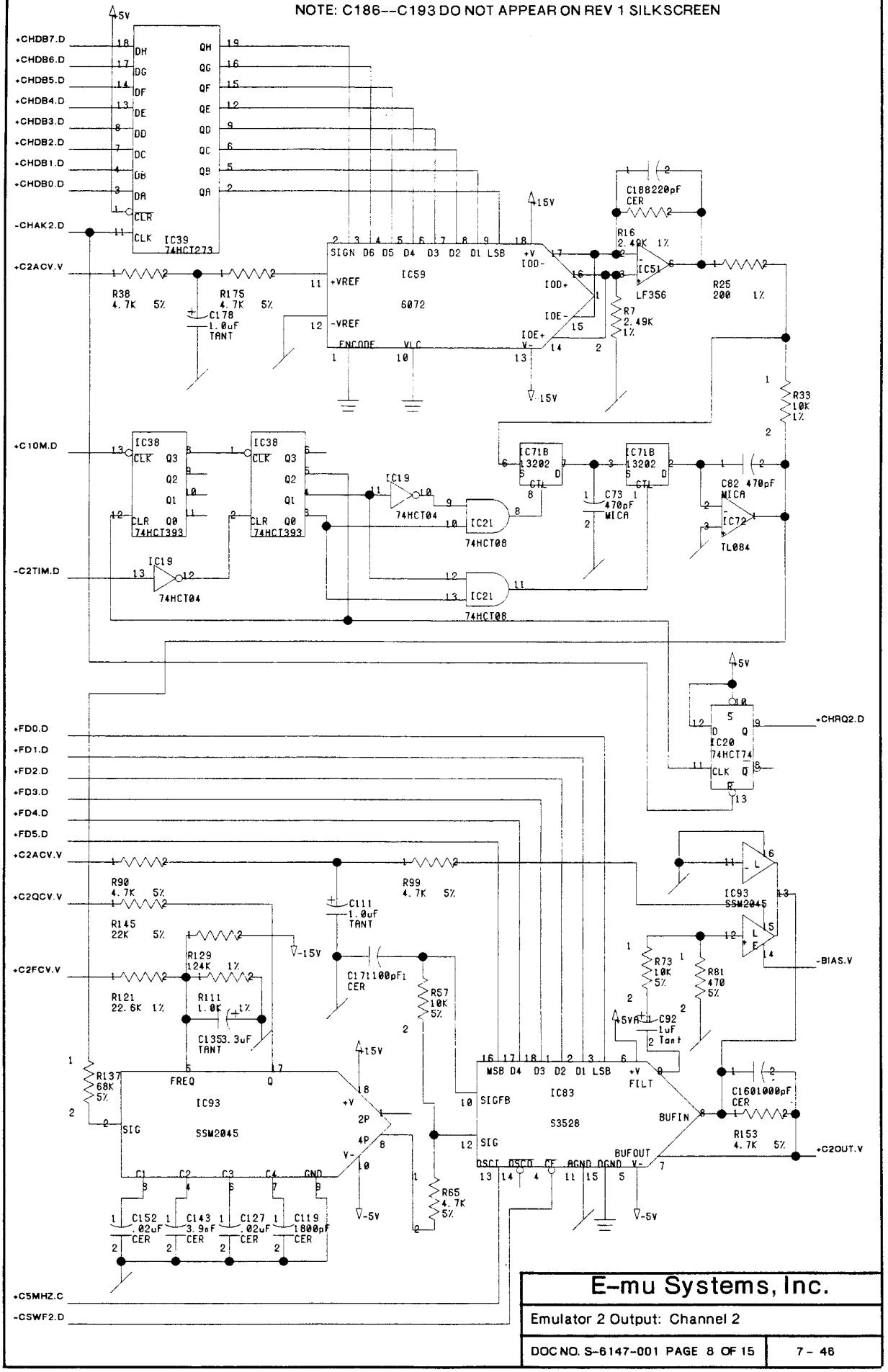


E-mu Systems, Inc.

Emulator 2 Output: Channel 1

NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN



E-mu Systems, Inc.	
Emulator 2 Output: Channel 2	
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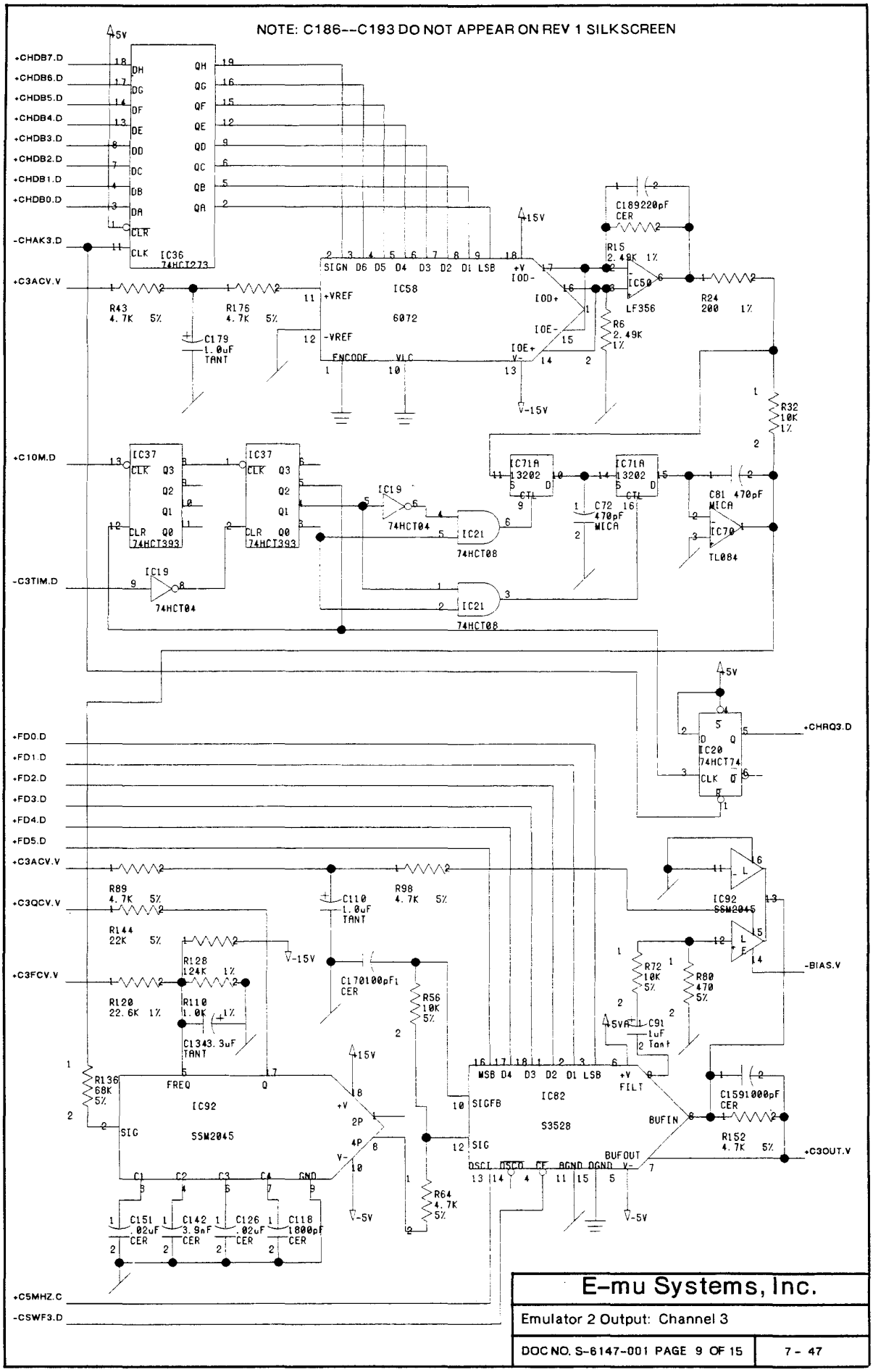
NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN
+CHDB7.D
+CHDB6.D
+CHDB5.D
+CHDB4.D
+CHDB3.D
+CHDB2.D
+CHDB1.D
+CHDB0.D
-CHAK3.D
+C3ACV.V
+C10M.D
-C3TIM.D
+FD0.D
+FD1.D
+FD2.D
+FD3.D
+FD4.D
+FD5.D
+C3QCV.V
+C3FCV.V
+C5MHZ.C
-CSWF3.D
+CHRQ3.D
-BIAS.V
+C3OUT.V
IC36 74HCT273
IC58 6072
IC50 LF356
IC37 74HCT393
IC19 74HCT04
IC21 74HCT08
IC71A 13202
IC70 TL084
IC20 74HCT74
IC92 SSM2045
IC82 S3528
R43 4.7K 5%
R176 4.7K 5%
R6 2.49K 1%
R24 200 1%
R32 10K 1%
R89 4.7K 5%
R98 4.7K 5%
R144 22K 5%
R128 124K 1%
R120 22.6K 1%
R110 1.0K 1%
R136 68K 5%
R56 10K 5%
R64 4.7K 5%
R72 10K 5%
R80 470 5%
R152 4.7K 5%
C179 1.0uF TANT
C110 1.0uF TANT
C134 3.3uF TANT
C91 1uF Tant
C72 470pF MICA
C81 470pF MICA
C151 .02uF CER
C142 3.9nF CER
C126 .02uF CER
C118 1800pF CER
C189220pF CER
C1591000pF CER
+5V
-5V
+15V
-15V
E-mu Systems, Inc.
Emulator 2 Output: Channel 3
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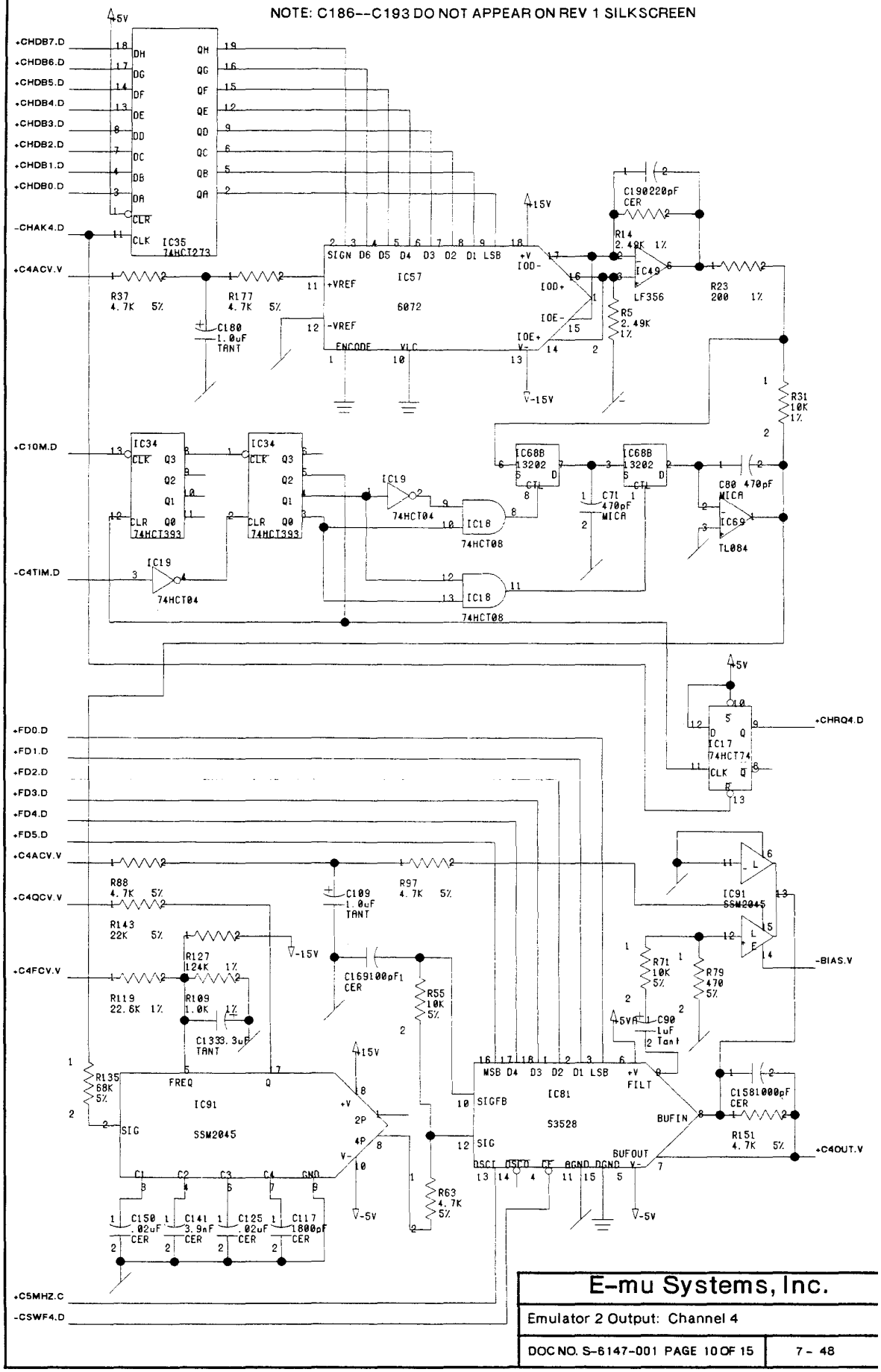
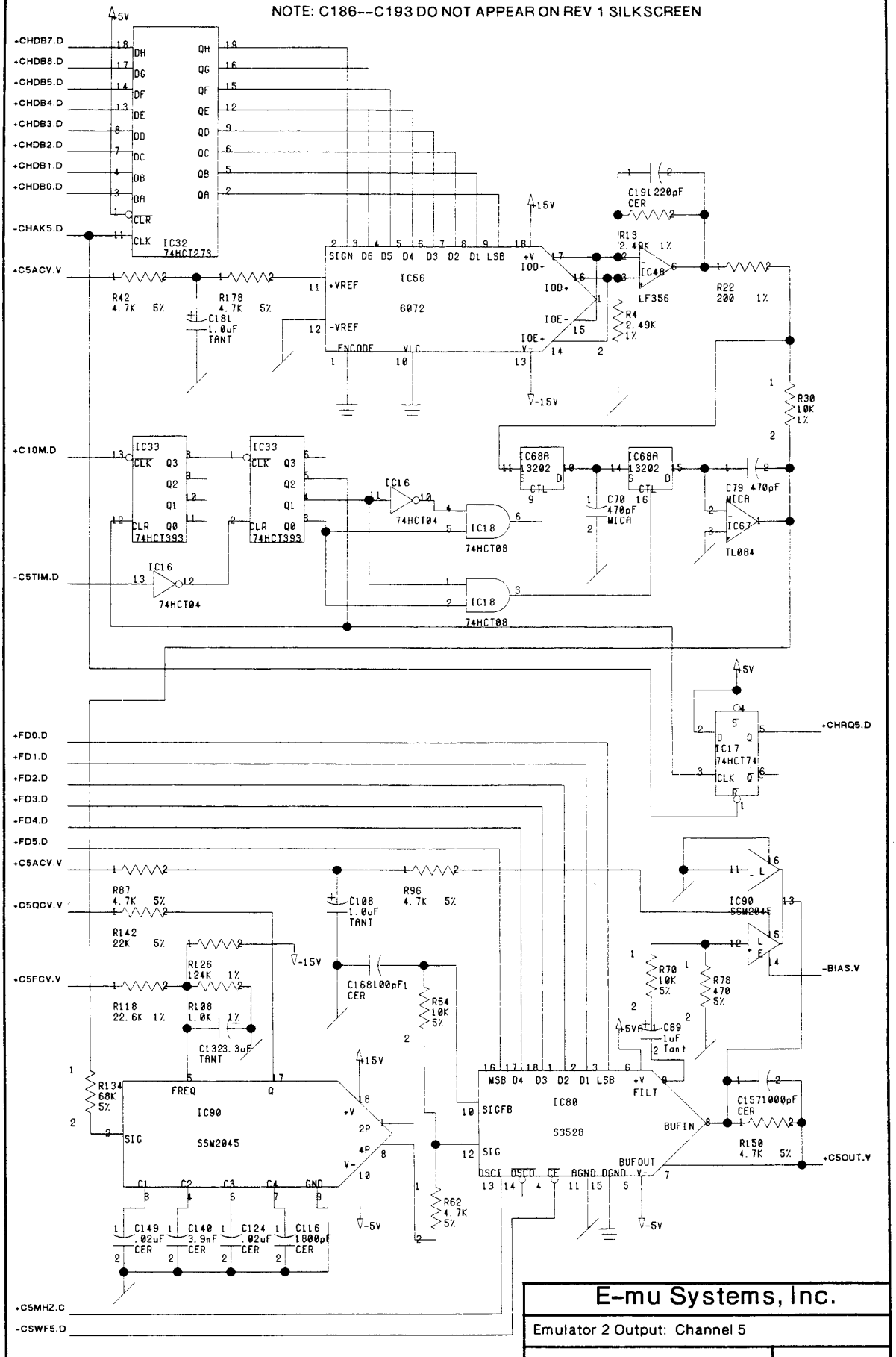

NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN
+CHDB7.D
+CHDB6.D
+CHDB5.D
+CHDB4.D
+CHDB3.D
+CHDB2.D
+CHDB1.D
+CHDB0.D
-CHAK4.D
+C4ACV.V
+C10M.D
-C4TIM.D
+FD0.D
+FD1.D
+FD2.D
+FD3.D
+FD4.D
+FD5.D
+C4ACV.V
+C4QCV.V
+C4FCV.V
+C5MHZ.C
-CSWF4.D
+CHRQ4.D
-BIAS.V
+C4OUT.V
IC35 74HCT273
IC57 6072
IC34 74HCT393
IC19 74HCT04
IC18 74HCT08
IC68B 13202
IC49 LF356
IC69 TL084
IC17 74HCT74
IC91 SSM2045
IC81 S3528
R37 4.7K 5%
R177 4.7K 5%
R14 2.49K 1%
R23 200 1%
R5 2.49K 1%
R31 10K 1%
R88 4.7K 5%
R97 4.7K 5%
R143 22K 5%
R127 124K 1%
R119 22.6K 1%
R109 1.0K 1%
R135 68K 5%
R55 10K 5%
R63 4.7K 5%
R71 10K 5%
R79 470 5%
R151 4.7K 5%
C180 1.0uF TANT
C109 1.0uF TANT
C133 3.3uF TANT
C90 1uF Tant
C190220pF CER
C169100pF CER
C158 1000pF CER
C150 .02uF CER
C141 3.9nF CER
C125 .02uF CER
C117 1800pF CER
C71 470pF MICA
C80 470pF MICA
+5V
+15V
-15V
-5V
+5VA

NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN



E-mu Systems, Inc.	
Emulator 2 Output: Channel 5	
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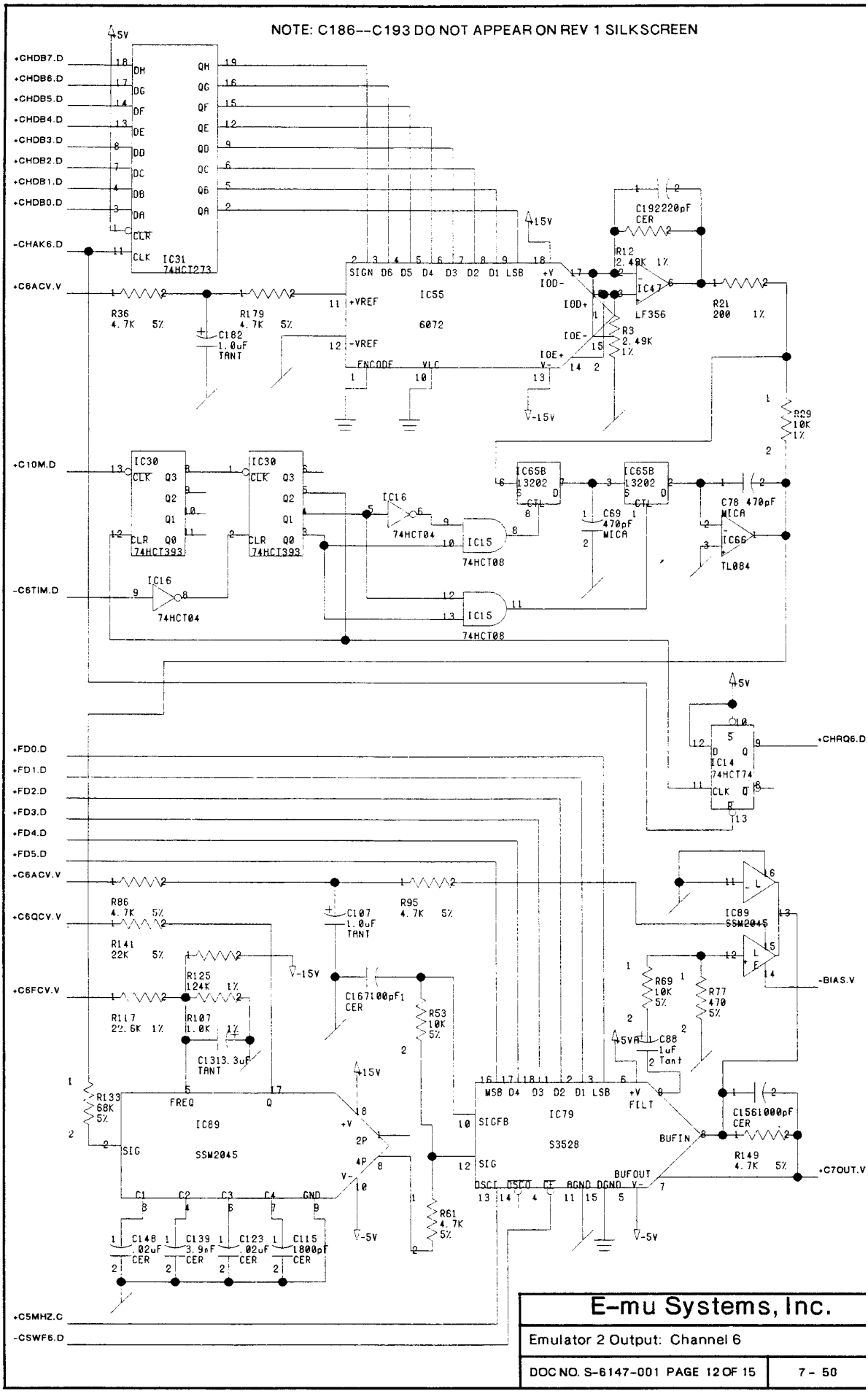
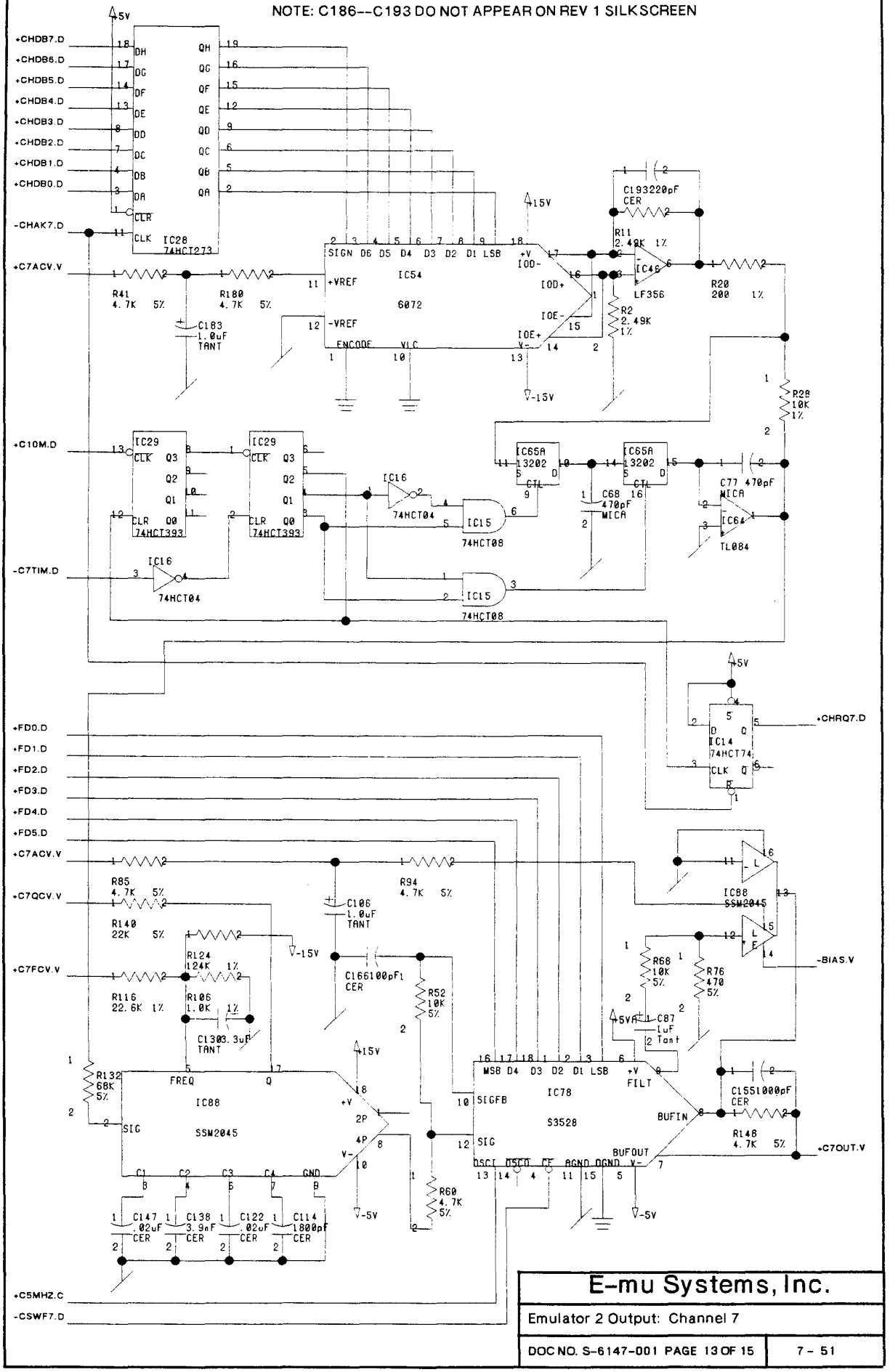


E-mu Systems, Inc.

Emulator 2 Output: Channel 6

NOTE: C186--C193 DO NOT APPEAR ON REV 1 SILKSCREEN



E-mu Systems, Inc.	
Emulator 2 Output: Channel 7	
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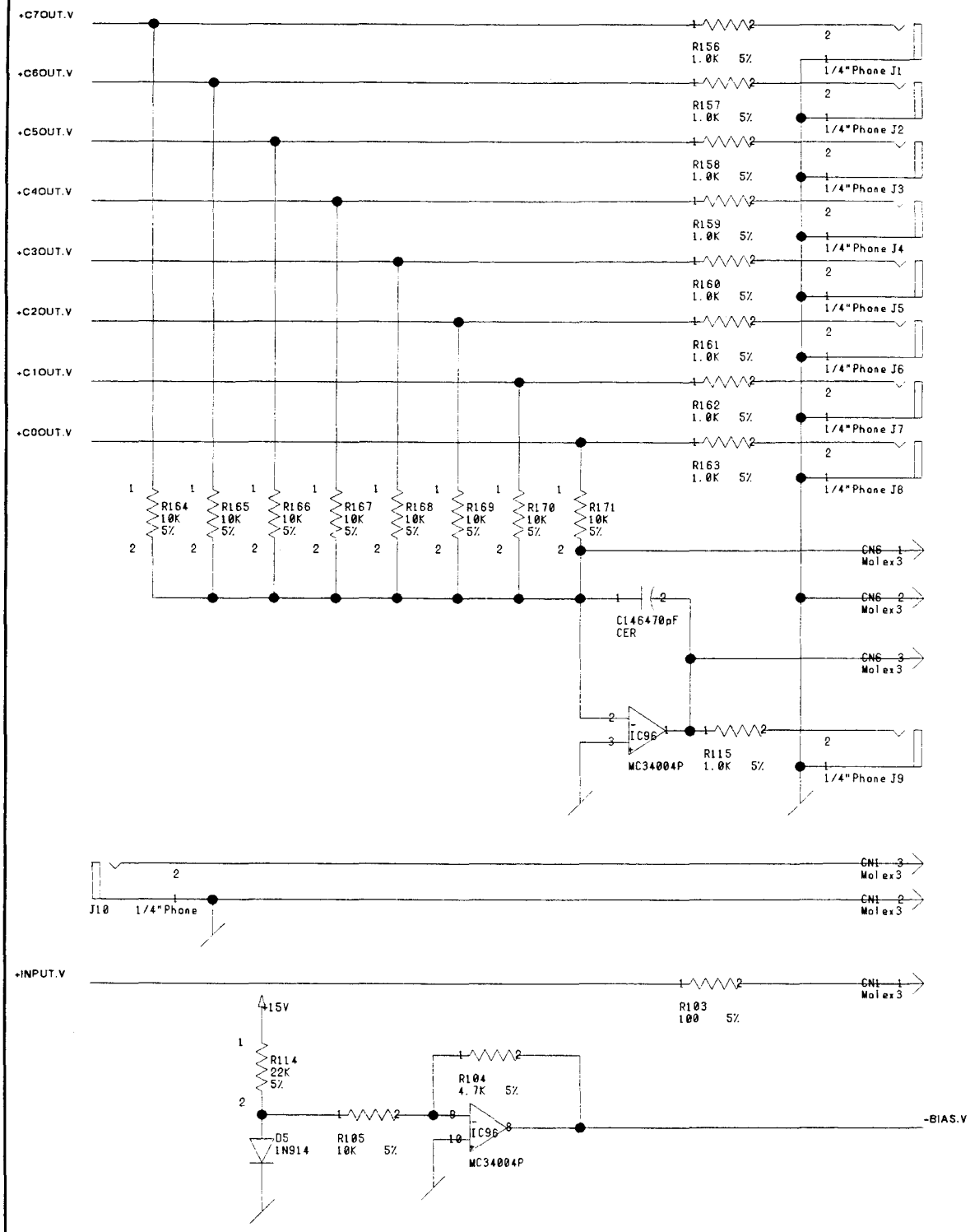

E-mu Systems, Inc.	
Emulator 2 Output: Mixer, Common	
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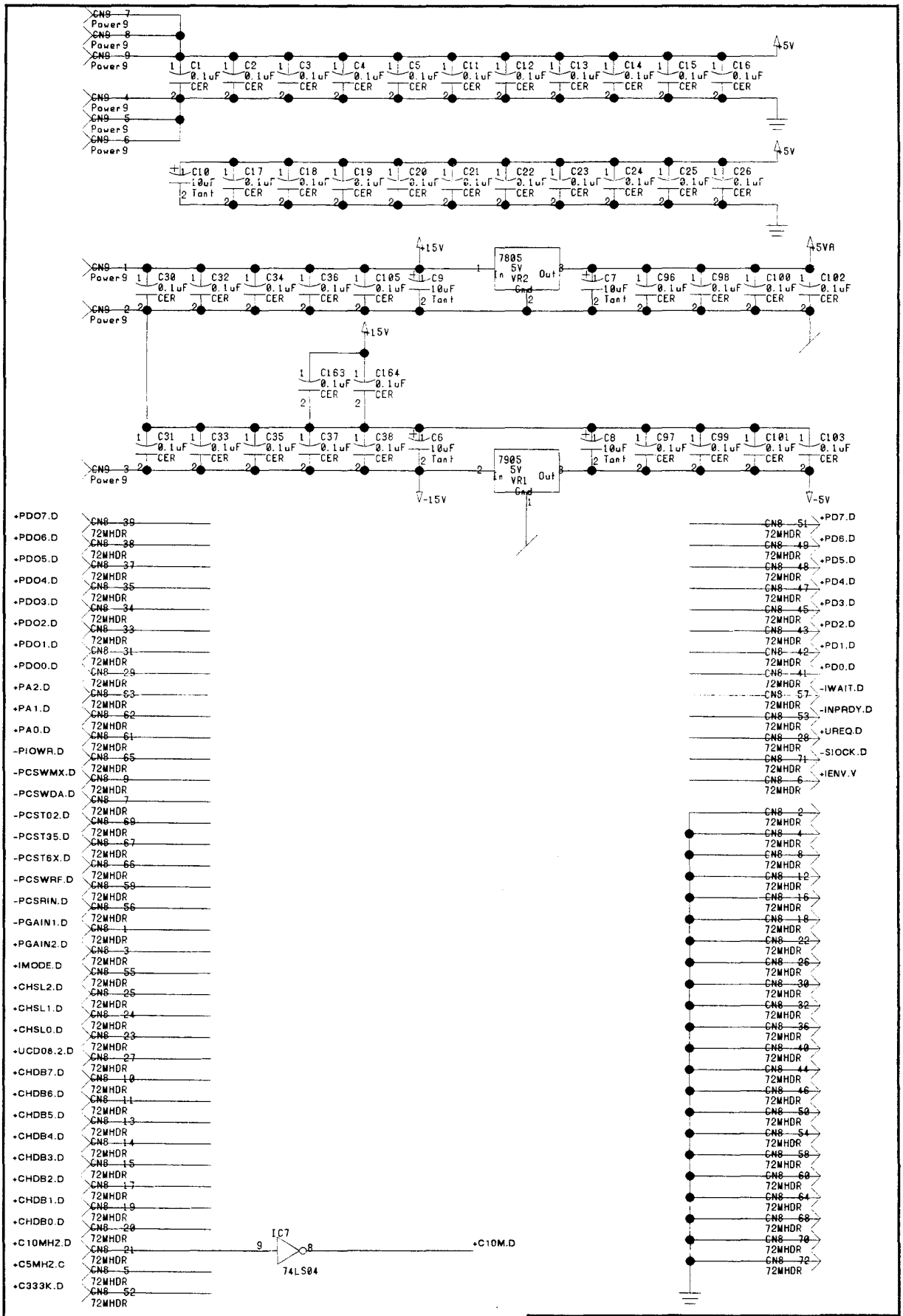

E-mu Systems, Inc.	
Emulator 2 Output: Connectors & Power	
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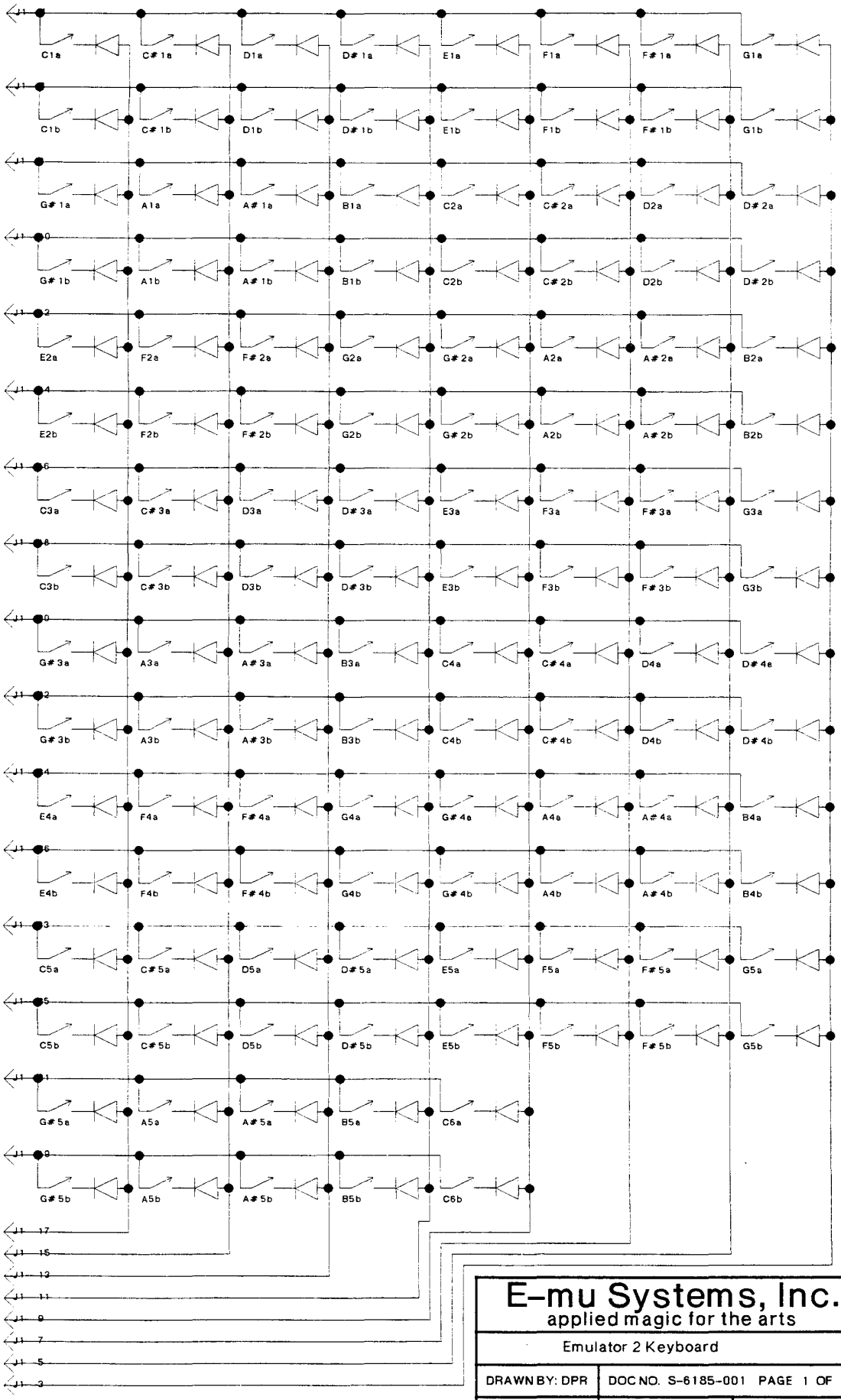

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Emulator 2 Keyboard

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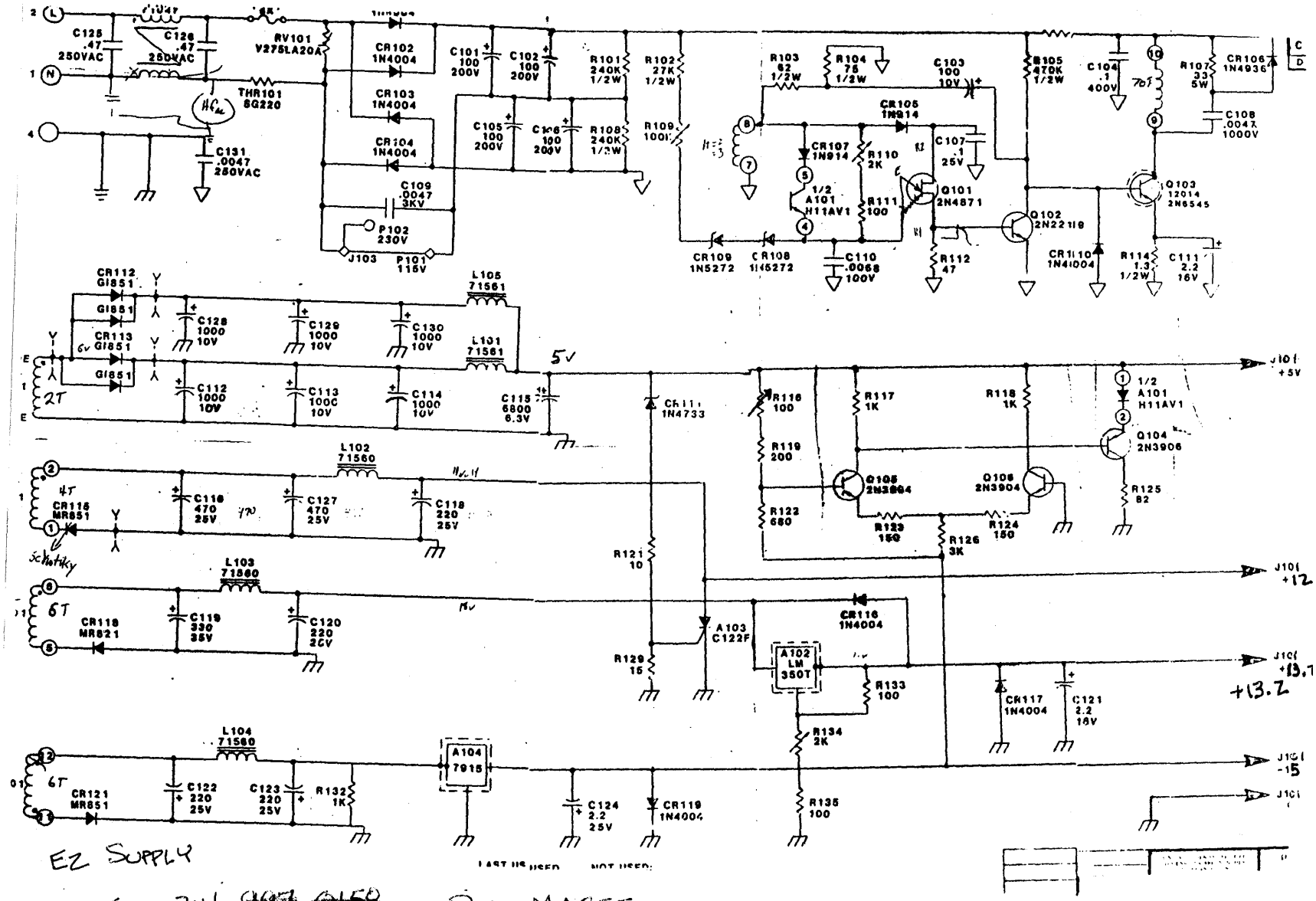
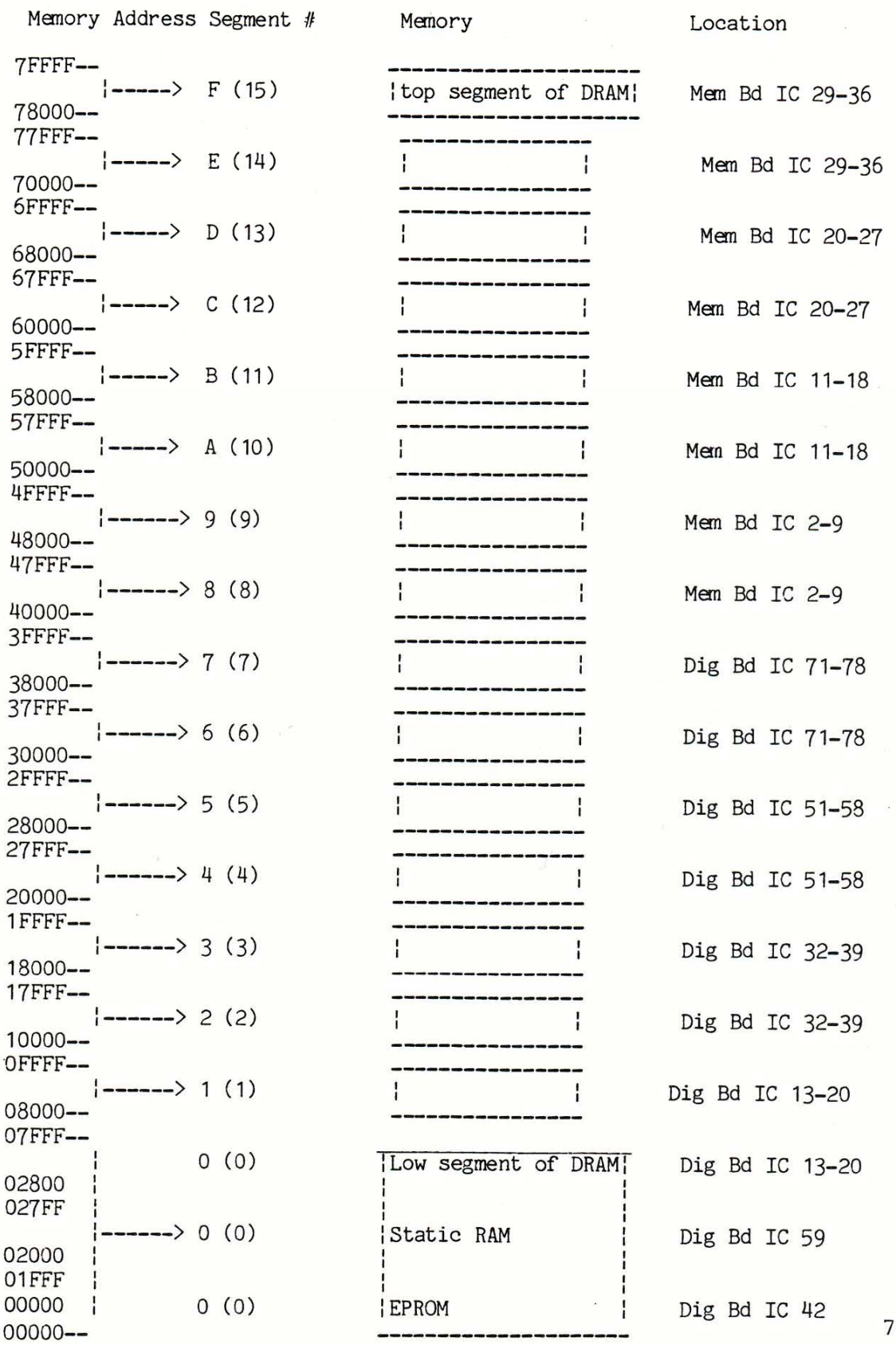

C125 .47 250VAC
C126 .47 250VAC
RV101 V275LA20A
THR101 SG220
C131 .0047 250VAC
CR102 1N4004
CR103 1N4004
CR104 1N4004
C109 .0047 3KV
P102 230V
J103
P101 115V
C101 100 200V
C102 100 200V
C105 100 200V
C106 100 200V
R101 240K 1/2W
R108 240K 1/2W
R102 27K 1/2W
R109 100K
R103 82 1/2W
R104 75 1/2W
C103 100 10V
CR105 1N914
CR107 1N914
R110 2K
C107 .1 25V
1/2 A101 H11AV1
R111 100
Q101 2N4871
CR109 1N5272
CR108 1N5272
C110 .0068 100V
R112 47
R105 470K 1/2W
C104 .1 400V
R107 33 5W
CR106 1N4936
C108 .0047 1000V
Q103 12014 2N6545
Q102 2N2218
CR1110 1N41004
R114 1.3 1/2W
C111 2.2 16V
CR112 GI851
CR113 GI851
L105 71561
L101 71561
C128 1000 10V
C129 1000 10V
C130 1000 10V
C112 1000 10V
C113 1000 10V
C114 1000 10V
C115 6800 6.3V
2T
5V
CR111 1N4733
R116 100
R117 1K
R118 1K
R119 200
R122 680
Q105 2N3904
Q106 2N3904
R123 150
R124 150
R126 3K
1/2 A101 H11AV1
Q104 2N3906
R125 82
+5V
L102 71560
4T
CR115 MR851
C116 470 25V
C117 470 25V
C118 220 25V
Schottky
L103 71560
6T
CR118 MR821
C119 330 35V
C120 220 25V
R121 10
R129 15
A103 C122F
CR116 1N4004
A102 LM 350T
R133 100
R134 2K
CR117 1N4004
C121 2.2 16V
+12
+13.7
+13.2
L104 71560
6T
CR121 MR851
C122 220 25V
C123 220 25V
R132 1K
A104 7915
C124 2.2 25V
CR119 1N4004
R135 100
-15
EZ SUPPLY
LAST IS USED
NOT USED:

EMULATOR 2 MEMORY ORGANIZATION



NET LIST FOR SCHEMATIC SET FOR E2 DIGITAL PCB

SIGNAL NAME	SRCE P#	DEST P#s	NOTES
+ALUGQ.D	21	18	ALU latch clock
+BACKMD.D	13	13	Latch bkwd mode flag
+C10MHZ.D	25	18	Basic 10MHz clock
-C10MHZ.1.D	25	13,16,17,19	Inverted Buff'd clock
-C10M.D	18	20	Yet another clock
+C10MHZ.1.D	25	12,13,16	Buffered clock
+C10MHZ.2.D	25	13,16,18,19	Buffered clock
+C2.5M.D	25	10	clock
+C2MHZ.D	25	9	clock
+C333K.D	25	Output Board	clock
+C4MHZ.D	25	1,5	clock
+C500K.D	25	11,3	clock
+C5MHZ.C	25	Output Board	clock
+C5MHZ.D	25	11	clock
+CAS.D	18	20	CAS unbuffered
-CASB0-CASB3.D	20	21,22,23,24	CAS to Memory IC's
+CHDB0-CHDB7.D	20	Output Board	Channel Data Bus
+CHSL0-+CHSL3	12	13,14,16	Channel Select Bus
+CRST.D	25	11	Power On Reset
-CRST.D	25	1,5,6,8,9,10,12,13	Power On Reset
+CTCIEO.D	8	9	Int enable CTC-PIO
+CTS.V	RS232	11	Clear to Send
-DDIR.D	9	Disk	Disk Direction
+DECCTL.D	13	17	Decrement Control
+DECFLG.D	13	13	Decrement Flag
-DIDX.D	Disk	10	Disk Index
+DMAIEO.D	8	8	Int enable DMA-CTC
-DMTRON.D	9	Disk	Disk Motor On
-DRDTA.D	Disk	10	Disk Receive Data
-DRDY.D	Disk	10	Disk Ready
-DSEL0.D	9	Disk	Disk Drive Select 0
-DSEL1.D	9	Disk	Disk Drive Select 1
-DSIDE.D	10	Disk	Disk Side Select
+DSR.V	RS232	11	Data Set Ready
-DSTEP.D	9	Disk	Disk Step Command
-DTK00.D	Disk	9	Disk Track 00 detect
+DTR.V	11	RS232	Data Terminal Ready
-DWDTA.D	10	Disk	Disk Write Data
-DWP.D	Disk	9	Disk Write Protect
-DWTGT.D	10	Disk	Disk Write Gate
+IENV.V	Out Bd	3	Input Envelope Voltage
+IMODE.D	9	Output Board	Input Mode
-INPRDY.D	Out Bd	8	Input Ready
-IWAIT.D	Out Bd	5	Input Wait
+LOOPMD.D	13	13	Loop Control Flag
+LWHEEL.V	FP	3	Left Wheel Voltage
+MAA0-MAA7.D	19	21,22	Memory IC Address Ins
+MBA0-MBA7.D	19	23,24	Memory IC address Ins
+MAD0-MAD7.D	19	Option Board	Memory IC addr unbuf.
+MDIB0-MDIB7.D	20	21,22,23,24,OpB	Memory IC input data
+MDOB0-MDOB7.D	21	20	Memory IC output data

SIGNAL NAME	SRCE P#	DEST P#	NOTES
+MIDI.V	MIDI	11	MIDI current loop
-MIDI.V	MIDI	11	MIDI current loop
+MIDO.V	11	MIDI	MIDI output
+MMOVE.D	9	8	Memory Move Burst Enable
-MMRDY.D	8	8	Memory Move Burst Pulse
+MPA15-MPA18.D	6	18,19	Seg-decoded Proc Mem Add
-MPGTE.D	13	20	Processor Mem Gate Enb
-MPRD.1.D	16	13	Processor read sync'd
-MPREQ.D	5	16	Proc main RAM req - gtd
-MPRG.D	5	20	Processor memory rd gate
-MPRQ.D	7	5	Processor main RAM req
-MPRQ.1.D	16	13	Proc main RAM req sync'd
-MPWEN.D	16	14	Reg File Write by Proc
+MPWFG.D	16	16	Proc Reg file Write Flag
-MRD.D	5	7	Main Processor Read
-MWR.D	5	7	Main Processor Write
+PA0-PA1.D	5	6,7,8,9,10,19	Processor Address Bus
+PA2-PA15.D	5	6,7,8,19	Processor Address Bus
-PBAK.D	5	6,8	Processor Bus Ack
-PBRQ.D	8	5	Processor Bus Request
+PCLK.D	5	8,9,10	Processor Clock
-PCSCTC.D	6	8	Main CTC Chip Select
-PCSDMA.D	6	8	Main DMA Chip Select
-PCSPIO.D	6	9	Main PIO Chip Select
-PCSRAD.D	6	Output Board	Main A/D Chip Select
-PCSSER.D	6	11	Main Serial Chip Select
-PCSSIO.D	6	10	Main SIO Chip Select
-PCST02.D	6	Output Board	Main Timer0-2 Chip Sel
-PCST35.D	6	Output Board	Main Timer3-5 Chip Sel
-PCST6X.D	6	Output Board	Main Timer6-extra C S
-PCSWDA.D	6	Output Board	Main D/A Write Select
-PCSWMR.D	6	6	Main SegReg Write Sel
-PCSWMX.D	6	Output Board	Main D/A Mux Write Sel
-PCSWRF.D	6	Output Board	Main Recon filt Wr Sel
-PCWS0-3.D	6	14	Main RegFile Wr Sels
+PD0-PD7.D	5	6,7,8,9,10,11,20	Processor Data Bus
+PDO0-PDO7.D	6	6,14,Output Bd	Buffered Proc Data Bus
-PGAIN1.D	4	Output Bd	Input Gain Select 1
+PGAIN2.D	4	Output Bd	Input Gain Select 2
-PINT.D	8,9,10	5	Main Proc Interrupt
+PIOB0-PIOB5.D	4	3	Kdb Scan Bus Encoded
-PIORD.D	5	6	Main Proc I/O Read
-PIORQ.D	5	8,9,10	Main Proc I/O Req
-PIOWR.D	5	6	Main Proc I/O Write
-PM1.D	5	7,8,9,10	Main Proc M1 Cycle
-PMRQ.D	5	7,8	Main Proc Mem Req
+PPG0.D	6	7	Processor Page 0 Select
-PRD.D	5	8,9,10,11,16	Main Proc Read Request
+PRECAR.D	13	13	Previous Carry Flag
-PRXC.D	11	10,1	SMPTE Receive Clock
+PRXD.D	11	10	SMPTE Receive Data
-PWAIT.D	5	5,8	Main Processor Wait
-PWR.D	5	8	Main Proc Write Req
+RAS.D	18	Option Bd.	+RAS Unbuffered

SIGNAL NAME	SRCE P#	DEST P#S	NOTES
-RASB0-RASB3.D	18	21,22,23,24	-RAS Buffered
-RASRST.D	18	Option Bd.	RAS Latch Reset (rfsh)
+RFA0-RFA5.D	14	15	Register File Addr Bus
+RFD00-RFD19.D	15	14,16,17	Register File Data
+RFD20-RFD23.D	15	13,14,17	Register File Data
+RFD00-19.1.D	16	17	Latched RF Data
+RFD20.1.D	13	17	Latched RF Data
+RFD22.1.D	13	17	Latched RF Data
-RFWR.D	16	15	Register File Write
-RSEL4-RSEL7.D	18	Option Bd	RAS Selects
+RTS.D	11	RS232	Request to Send
+RWHEEL.V	FP	3	Right Wheel Voltage
-RXD.V	RS232	11	RS232 Receive Data
+S24FPS.D	10	11	SMPTE 24 Frames/sec
+SA0-SA15.D	1	2,4	Scanner Address Bus
-SBUS0-SBUS41.D	3	Keybd/Panel,4	Scanner Kbd/PB busses
+SCI.D	3	1	Scanner Convert Int
+SCLK.D	1	4	Scanner Processor Clock
-SCON0-SCON7.D	Kbd/Pnl	3,4	Scanner Contact Inputs
-SCSMET.D	1	2	Scanner Metronome Sel
-SCSRC.D	1	3	Scanner Read A/D Conv
-SCSRPB.D	1	3	Scanner Read PB Cons
-SCSWC.D	1	3	Scanner Write A/D Conv
+SCSWD.D	1	Front Panel	Chip Select Write Disp
-SCSWL0-2.D	1	Front Panel	Chip Select Write Lamps
+SD0-SD7.D	1	2,3,4	Scanner Data Bus
+SDB0-SDB7.D	2	Front Panel	Scanner Buffered Data
+SDIR.D	4	9	Scanner Data Input Rdy
-SDIS.D	9	4	Scanner Data Input Stb
+SDO0-SDO7.D	4	9	Scanner-Proc Data Bus
+SDOR.D	9	4	Scanner Data Output Rdy
-SDOS.D	4	9	Scanner Data Output Stb
-SERINT.D	11	8	Serial Port Interrupt
+SIEO.D	1	4	Scanner Int Enable
-SINT.D	4	1	Scanner Interrupt
-SIOCK.D	Out Bd	10	SMPTE Transmit Clock
+SIOIEO.D	10	8	Int Enable SIO-CTC
-SIORDY.D	10	8	SIO Data Ready
-SIORQ.D	1	4	Scanner I/O request
+SLDRA-SLDRD.V	FP	3	Slider A-D Voltages
-SM1.D	1	4	Scanner M1 Cycle
+SMPI.V	SMPTE	11	SMPTE Input
+SMPO.V	10	SMPTE	SMPTE Output
-SMRD.D	1	2	Scanner Mem Read Req
+SMRQ.D	1	2	Scanner Memory Request
-SPROM.D	7	7	Main PROM select
-SRD.D	1	4	Scanner Read Request
-SSRAM.D	7	7	Main Static RAM request
+STATE0.D	12	13	Microcontroller State 0
+STATE3.D	12	16	Microcontroller State 3
+SUM0-SUM15.D	17	19	ALU Sum Output
+SUM16-SUM18.D	17	18	ALU Sum Output
-SWR.D	1	2	Scanner Write Request
-TXD.V	11	RS232	RS232 Transmit Data

SIGNAL NAME	SRCE P#	DEST P#S	NOTES
+UCD04.D	13	16	Microcode 4 Unbuffered
+UCD00.1.D	13	14	Microcode RF address 0
+UCD01.1.D	13	14	Microcode RF address 1
+UCD02.1.D	13	16	Microcode RF write
+UCD03.1.D	13	17	Microcode carry input
+UCD04.1A.D	13	17	Microcode inc/dec
+UCD04.1B.D	16	17	Microcode inc/dec
+UCD05.1.D	13	17	Microcode sum latch enb
+UCD06.1.D	13	17	Microcode sum out enb
+UCD07.1.D	13	19	Microcode MemAdd Ltch en
+UCD08.1.D	13	16,19	Microcode Chan Data Ltch
+UCD08.2.D	16	Output Bd	Microcode Chan Acknowl
+UCD09.1.D	13	5,13	Microcode Proc Data Rdy
+UCD10.1.D	13	20	Microcode Main Mem Write
+UCD11.1.D	13	19	Microcode Addr Mux Sel
+UCD12.1.D	13	18	Microcode RAS/CAS cntl
-UCD13.1.D	13	18	Microcode CAS control
+UCD14.1.D	13	18	Microcode Refresh cntl
+UCD15.1.D	13	18	Microcode Proc/Rf cntl
-UCD15.1.D	13	18,19	Microcode Proc/Rf cntl
+UCNT0-UCNT2.D	12	13	Microcode State Bus
-UCNT2.D	12	16	Microcode State Bus MS
+UREQ.D	Out Bd	13	Channel Request unsync
+UREQ.1.D	13	13	Channel Request sync'd
-WEB0-WEB3.D	20	21,22,23,24	Memory IC Write

NET LIST FOR SCHEMATIC SET FOR E2OUTPUT BOARD - Revision of 3/27/84

SIGNAL NAME	SRCE P#	DEST P#'s	Notes
-BIAS.V	14	6-13	Diode Bias Voltage
+C0ACV.V	1	6	Amplitude control Volt
+C1ACV.V	1	7	Amplitude control Volt
+C2ACV.V	1	8	Amplitude control Volt
+C3ACV.V	1	9	Amplitude control Volt
+C4ACV.V	1	10	Amplitude control Volt
+C5ACV.V	1	11	Amplitude control Volt
+C6ACV.V	1	12	Amplitude control Volt
+C7ACV.V	1	13	Amplitude control Volt
+C0FCV.V	1	↓	Filter CV control volt
+C1FCV.V	1	7	Filter CV control volt
+C2FCV.V	1	8	Filter CV control volt
+C3FCV.V	1	9	Filter CV control volt
+C4FCV.V	1	10	Filter CV control volt
+C5FCV.V	1	11	Filter CV control volt
+C6FCV.V	1	12	Filter CV control volt
+C7FCV.V	1	13	Filter CV control volt
+C0QCV.V	1	6	Filter Q control volt
+C1QCV.V	1	7	Filter Q control volt
+C2QCV.V	1	8	Filter Q control volt
+C3QCV.V	1	9	Filter Q control volt
+C4QCV.V	1	10	Filter Q control volt
+C5QCV.V	1	11	Filter Q control volt
+C6QCV.V	1	12	Filter Q control volt
+C7QCV.V	1	13	Filter Q control volt
+C0OUT.V	6	14	Channel Output
+C1OUT.V	7	14	Channel Output
+C2OUT.V	8	14	Channel Output
+C3OUT.V	9	14	Channel Output
+C4OUT.V	10	14	Channel Output
+C5OUT.V	11	14	Channel Output
+C6OUT.V	12	14	Channel Output
+C7OUT.V	13	14	Channel Output
-C0TIM.D	2	6	Channel Timer
-C1TIM.D	2	7	Channel Timer
-C2TIM.D	2	8	Channel Timer
-C3TIM.D	2	9	Channel Timer
-C4TIM.D	2	10	Channel Timer
-C5TIM.D	2	11	Channel Timer
-C6TIM.D	2	12	Channel Timer
-C7TIM.D	2	13	Channel Timer
+C10M.D	15	2,6-13	clock
+C10MHZ.D	Dig Bd	15	clock
+C333K.D	Dig Bd	15,5	clock
+C5MHZ.C	Dig Bd	4,6-13,15	clock
-CHAK0.D	3	6	Channel Acknowledge
-CHAK1.D	3	7	Channel Acknowledge
-CHAK2.D	3	8	Channel Acknowledge
-CHAK3.D	3	9	Channel Acknowledge
-CHAK4.D	3	10	Channel Acknowledge
-CHAK5.D	3	11	Channel Acknowledge
-CHAK6.D	3	12	Channel Acknowledge

SIGNAL NAME	SRCE P#	DEST P#S	Notes
-CHAK7.D	3	13	Channel Acknowledge
+CHDB0-CHDB7.D	dDig Bd	6-13,15	Channel Data Bus
+CHRQ0.D	6	3	Channel Request
+CHRQ1.D	7	3	Channel Request
+CHRQ2.D	8	3	Channel Request
+CHRQ3.D	9	3	Channel Request
+CHRQ4.D	10	3	Channel Request
+CHRQ5.D	11	3	Channel Request
+CHRQ6.D	12	3	Channel Request
+CHRQ7.D	13	3	Channel Request
+CHSL0-CHSL2.D	Dig Bd	3,15	Channel Select Encoded
-CSWF0.D	3	4,6	Select Input & Ch0 Filt
-CSWF1.D	3	7	Select Channel Filter
-CSWF2.D	3	8	Select Channel Filter
-CSWF3.D	3	9	Select Channel Filter
-CSWF4.D	3	10	Select Channel Filter
-CSWF5.D	3	11	Select Channel Filter
-CSWF6.D	3	12	Select Channel Filter
-CSWF7.D	3	13	Select Channel Filter
+ENCODE.D	5	6	Input DAC Encode Mode
+FD0-FD5.D	3	4,6-13	Filter Data Bus
+IDAC.V	6	4	Channel 0 DAC voltage
+IDAC0-IDAC7.V	5	6	Channel 0 DAC data bus
+IDATA.D	4	5	Comparator Data Out
+IENV.V	4,15	Digital Bd	Input Envelope
+IINT.V	6	4	Channel 0 Integrator
+IMODE.D	Dig Bd	5,6,15	Input Mode Select
-INPRDY.D	5,15	Digital Bd	Input Ready
+INPUT.V	FP	4,14	Atten'd input signal
+ISMPL.D	5,6	4	Sample/Hold Command
-IWAIT.D	5,15	Digital Bd	Input Wait for data
+PA0-PA2.D	Dig Bd	2,3,15	Processor Address Bus
-PCSRIN.D	Dig Bd	5,15	Proc Chip Sel Read In
-PCST02.D	Dig Bd	2,15	Proc CS Timer Ch0-Ch2
-PCST35.D	Dig Bd	2,15	Proc CS Timer Ch3-Ch5
-PCST6X.D	Dig Bd	2,15	Proc CS Timer Ch6,7,SIO
-PCSWDA.D	Dig Bd	1,15	Proc CS Write DAC
-PCSWMX.D	Dig Bd	1,15	Proc CS Write Mux Sel
-PCSWRF.D	Dig Bd	3,15	Proc CS Write Recon Flt
+PD0-PD7.D	5,15	Digital Bd	Processor Data Bus
+PD00-PD07.D	Dig Bd	1,2,3,15	Processor Buf'd Data
-PGAIN1.D	Dig Bd	4,15	Input Gain Select 1
+PGAIN2.D	Dig Bd	4,15	Input Gain Select 2
-PIOWR.D	Dig Bd	2,15	Processor I/O Write
-SIOCK.D	2,15	Digital Bd	SMPTE Clock
+UCD08.2.D	Dig Bd	3,15	Channel Acknowledge
+UREQ.D	3,15	Digital Bd	Encoded Channel Req

E-mu Systems, Inc.

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ENGINEERING CHANGE ORDER

E.C.O. No: 093

Date: 9-10-84 E.C.O. By: B.H.M. Approval: [signature] Chief Engineer: [signature]

Confidential: _____ Customer Release: X

Affects Product: Emulator 2 Affects Assembly: AE311, AE312

Serial Nos. Modified in Production: N/A

Notation to Modify Units in Repair: See reverse.

Approximate Starting Serial No. for New Documents: 26
(visual check or call factory to verify)

P.C.B. Serial No. 26

Purpose of Change: To enable implementation of new MIDI software update.

PRIORITY OF CHANGE:

For Future Units: X Modify Units in Production: X

Modify all Units Available for Repair: X Modify All Field Units: X

PARTS AFFECTED:

Reference Designator		Description		Part Number	
Old	New	Old	New	Old	New
R10	same	4.7k,1/4w,5%	270,1/4w,5%	RR307	RR347*
R41	same	220,1/4w,5%	150,1/4w,5%	RR339	RR102
R42	"	"	"	"	"
R43	"	"	"	"	"
IC107	same	SCN2651	less pin #15	II335	same

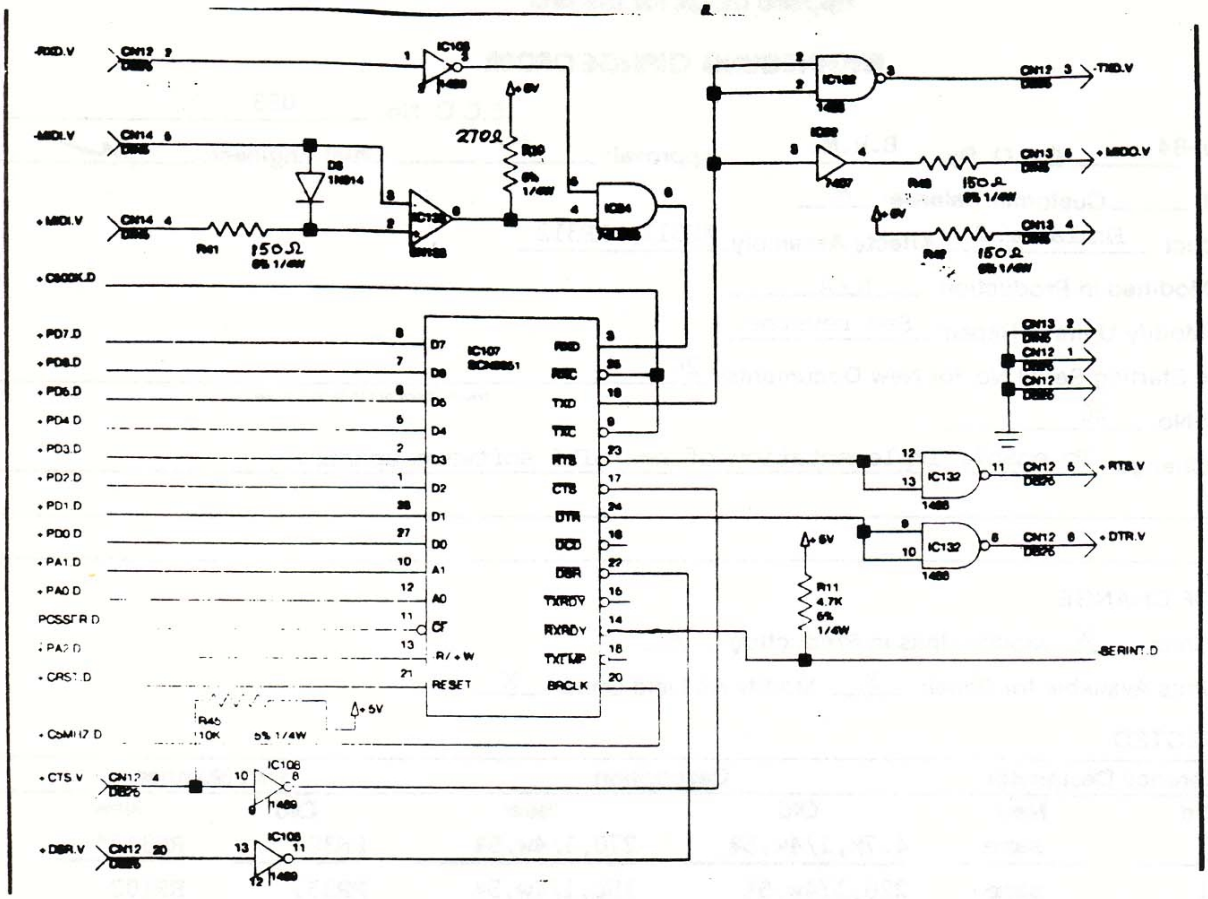
* ATTN: PURCHASING: NEW PART.

FULL DESCRIPTION OF CHANGES ON REVERSE SIDE & ATTACHED DOCUMENTS

FOR E-MU SYSTEMS, INC. USE ONLY:

Documents Affected	Page No.	Deliver to Production	Deliver to Purchasing	Obsolete Copies Filed	Preformed By	Date
X Schematic	11					
_____ Software						
X Parts List	all	X	X	X	B.H.M.	9/11/84
X Assy. Diag.	ALL	X		X	B.H.M.	9/11/84
_____ P.C.B Masters						
_____ P.C.B. Films						
_____ Dimensional Diag						
_____ Package Master Art						
_____ Package Films						
_____ Other. _____						
_____ Other: _____						

E.C.O. Completed and Filed By: Brian Monahan Date: _____

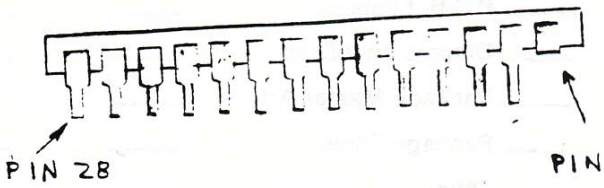


Mechanical Diagram: Old

N/A

New

SCN 2651 (SIDE VIEW)



REMOVE OR BEND PIN 15 90 DEGREES UNDER PART. PIN 15 NOT TO BE CONNECTED.

Engineering Change Order ECO # 109

ECO by: BHM Approved by: M CK by: M Date 1-30-85

Product affected 6018/6028 Approx. starting S/N _____

This ECO is for in house use only _____

This ECO is to be included in product service manual X

The purpose for this ECO is: to enable the sequencer click. track sync. to function properly.

This ECO is to be implemented on all:

Units in process X Field Units _____

Finished Goods X Units available for repair X

Future units X Units that problem exists X

Parts affected:

E-mu P/N	Description	BOM	Old rev	New rev	Attached
AE311	E^2 Digital Backboard PWA	X	Ø.C	Ø.D	X

Documents affected:

A-6149-Ø11 E^2 Digital Backboard assy diagram

S-6149-ØØ1 E^2 Digital schematic (pgs 8+9)

PCB affected	Old rev	New rev	Schematic revs	Starting S/N
				675

ECO completed and filed by: _____ Date _____

Emulator 2 digital board kluges to rev 0.D boards
*Refer to document # A-6149-011 *
Vers. 850130

#	Date	Who	Describe
1	4/30	dr	On component side, add bare wire horizontal jumper between to vias directly to right of pin 16 of IC112. (See detail "M") Check by verifying continuity between IC112 pin 11 and IC 67 pin 9.
2	4/30	dr	On solder side, cut trace from IC 92 pin 5 to via. Add bare wire jumper from this via to IC 92 pin 6. (See detail "B") Check by verifying continuity betweem IC92 pin 6 and IC 92 pin 12, and lack of continuity between IC 92 pin 5 and IC 92 pin 6.
3	4/30	dr	On solder side, cut thick trace from IC 132 pin 7 to IC 132 pins 4 and 5. Pins 4 and 5 remain connected. (See detail "C") On component side, cut trace from pin 4 of IC 108 to resistor R23. (See detail "N"). On solder side, add insulated jumper from IC 46 pin 34 to IC 132 pin 5. On solder side, add insulated jumper from IC 132 pin 6 to CN12 pin 12. This is the next to furthest pin on the longer row of the DB25 RS232 connector. On solder side, add insulated jumper from IC 46 pin 31 to IC 108 pin 6. On solder side, add insulated jumper from IC108 pin 4 to CN12 pin 13, which is the furthest pin on the longer row of the DB25 RS232 connector. (See ass'y diagram, P. 2) Check by verifying continuity between CN12 pin 12, IC132 pin 6. Verify continuity between IC132 pin 4, IC132 pin 5, and IC 46 pin 34. Verify continuity between CN12 pin 13 and IC 108 pin 4. Verify continuity between IC108 pin 6 and IC 46 pin 31. Verify lack of continuity between IC 108 pin 4 and IC108 pin 7. Verify lack of continuity between IC132 pin 4 and IC132 pin 7.
4	4/30	dr	On solder side, add 10K resistor R45 between IC108 pin 10 and IC108 pin 14. (See detail "D"). Check by visual.
5	4/30	dr	On solder side, add 47K resistor R44 between J6 ground shield pin (top center) and J6 lower pin. Check by visual. (See detail "E").
6	4/30	dr	Check on component side for short or open on trace near IC 24 pin 40. Repair if necessary. (See detail "O"). Check by verifying continuity between IC24 pin 17 and IC 46 pin 16. Verify lack of continuity between IC 24 pin 17 and IC 24 pin 40.

7	4/30	dr	On solder side, add bare jumper from IC87 pin 14 to IC87 pins 13,12,11,10. (See detail "F"). Check by verifying continuity between IC87 pins 10-14.
8	4/30	dr	Verify C63 is 10 uF with + end nearest IC62.
9	5/10	dr	On Prototype boards ONLY (not necessary on production rev 0 boards) drill hole for mounting spacer near CN9. Hole should be .140 dia and should be located directly above pin 4 of CN9 by .200 inches. The hole should be VERY carefully drilled from the bottom side to avoid damaging bottom side traces. After drilling, use an xacto knife and a magnafying lens to examine and insure that the two inner layers are not shorted. The board will be mounted using an insulating shoulder washer to insure that the screw does not touch the inner layers.
10	5/10	dr	Add insulating pad on solder side around mounting hole near CN9 and C81. Crazy glue HW115 pad to board. Use Permabond 750, EMU P/N BS329.
11	5/26	dr	On component side, cut trace from upper pin of R41 to "pin 4" of CN14. On component side, cut trace from "pin 5" of CN14 to via near "pin 4" of CN14. (See detail "P"). On component side, cut trace from "pin 4" of CN13 to lower pin of R42. On component side, cut trace from "pin 5" of CN13 to lower pin of R43. (See detail "Q"). On solder side, add the following four jumpers: Bare jumper from "pin 4" of CN14 to via right next to it. Insulated jumper from "pin 5" of CN14 to upper pin of R41. (See detail "H") Insulated jumper from "pin 4" of CN13 to lower pin of R43. Insulated jumper from "pin 5" of CN13 to lower pin of R42. (See detail "I") Check by verifying continuity between the following pairs of points: CN14 "pin 5" to upper end of R41. CN14 "pin 4" to IC133 pin 3. CN13 "pin 5" to lower end of R42. CN13 "pin 4" to lower end of R43. And verify lack of continuity between: CN14 "pin 4" and CN14 "pin 5". CN13 "pin 4" and CN14 "pin 5".

12	5/29	dr	On solder side, cut trace from via nearest IC66 pin 33 (via is lowest of group of 6 vias) to via nearest IC66 pin 37 (which is one of two next to highest in same group of 6 vias). Leave trace intact which continues onward from the second via mentioned upwards. On solder side, add insulated jumper from the first via mentioned to pin 8 of IC68. (See detail "J") Check by verifying continuity between pin 10 of IC27 and pin 8 of IC68, continuity between pin 9 of IC107 and pin 9 of IC68, and lack of continuity between pin 8 and pin 9 of IC68.
13	6/4	dr	On solder side, add bare jumper between pin 8 of IC 133 and the pin of C142 directly above. (See detail "K") Check by verifying continuity between IC133 pin 8 and IC108 pin 14.
14	6/26	ws	On component side, cut etch at IC43-13. On component side, cut etch as it emerges from between IC43-1 and IC43-2, isolating a via we will refer to as "A". (See detail "R"). On solderside, connect "A" via to the via nearest IC43-13. On solder side, connect IC43-13 to IC43-14. (See detail "L").
15	7/12	dr	Add 0.1uF capacitor CC314 across diode D4. (Component Side). (See detail "A").
16	7/30	dr	On solder side, jumper between IC107-4 and IC107-16. (See detail "S").
17	8/10	dr	Cut trace from IC68-5 to IC115-13 on the solder side near IC68. Install a 330 ohm, 5% resistor in the feedthru at the end of the severed trace (see detail "W"). Wire from the other end of the resistor to IC68-5. Secure the resistor and the wire using RTV adhesive (see detail "W"). On the component side of board, install a 100 pf ceramic capacitor from the same feedthru as the resistor on the opposite side. Solder directly to the resistor (see detail "T").
18	8/10	dr	Component side- cut trace at IC69-11, isolating a feedthru. Cut trace as it emerges from between IC69 pins 9 and 10, isolating a second feedthru. (See detail "V"). On the solder side, wire between the two feedthrus we just isolated. Now wire between IC69-11 and IC30-5. (See detail "U").

19	9/7	dr	On IC107 remove the 2651 from the socket. Bend pin 15 of the 2651 underneath. Reinstall the 2651, with the bent pin now not making contact.
20	1/30/85	dr	On the solderside of the board, cut trace at IC106-11. Solder an insulated wire between IC106-11 and IC106-8. Solder one end of a 100k resistor (P/N RR318) to the top end of R39. Solder the unbanded end of a 1N914 diode (P/N DD301) to the other end of the 100k resistor, (see detail "Y"). Cut the trace at IC24-33. Wire between the banded end of the diode and IC24-33. The resistor and the diode should point towards IC 24 in a line, and after soldering, should be secured with an RTV adhesive to the PCB. Use care to avoid shorting to any adjacent pins or traces.

*****END OF LIST OF KLUGES*****

E-mu Systems, Inc.
Engineering Change Order

ECO # 114

ECO by: T.P. **Checked by:** B.H.M. **Appr. by:** D.P.R. **Date:** 850502

Product affected: Emulator 2 **Model #:** 6018 / 6028

Approx. starting S/N: 346 / 823 (respectively)

This ECO is for: [X] In house use [X] Service Manual

The purpose for this ECO is: To elimenate gross deviations in channel to channel resonances (Q) on the Emulator 2.

On the Output PWA, change the value of capacitors C114 -- C121 from 2,200 pF +/- 20% to 1,800 pF +/- 10%.

OLD PART NUMBER	NEW PART NUMBER
CC327	CC330

This ECO is to be implemented on all:

- [ ] Finished goods
- [ ] Units in process
- [X] Future units
- [ ] field units
- [ ] Units available for repair
- [X] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE3	E2 Output wave solder assy.	[X]	B	[X]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]

Documents affected	Document #	New rev #
Emulator 2 Output PWA wave assy. diagram	A-6148-011	B

PCB affected	E-mu P/N	New rev #	Starting S/N

E-mu Systems, Inc.
Engineering Change Order

ECO # 114

ECO by: T.P. Checked by: B.H.M. Appr. by: D.P.R. Date: 850502

Product affected: Emulator 2 Model #: 6018 / 6028

Approx. starting S/N: 346 / 823 (respectively)

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CC327	CC330

This ECO is to be implemented on all:

- [ ] Finished goods
- [ ] field units
- [ ] Units in process
- [ ] Units available for repair
- [x] Future units
- [x] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE310	E2 Output wave solder assy.	[X]	B	[X]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]

Documents affected	Document #	New rev #
Emulator 2 Output PWA wave assy. diagram	A-6148-011	B
Emulator 2 Output Schematics pgs. 1,6-13	S-6147-001	C

PCB affected	E-mu P/N	New rev #	Starting S/N

E-mu Systems, Inc.
Engineering Change Order

ECO #117

ECO by: D.L.M. Checked by: [illegible] Appr. by: [illegible] Date: 850523

Product affected: Emulator 2 Model #: 6018/6028

Approx. starting S/N: 379 / 948

This ECO is for: [X] In house use [X] Service Manual

The purpose for this ECO is: to improve SMPTE input sensitivity and reliability.

Fix: connect a 0.01 uF capacitor from pin 11 of IC131 to ground. Verify C138 is a 0.01 uF 10% as specified on the B.O.M., replace if necessary.

This ECO is to be implemented on all:

- [ ] Finished goods
- [ ] Units in process
- [X] Future units
- [ ] field units
- [ ] Units available for repair
- [X] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE311	Emulator 2 PCB Digital Backload	X		X

Documents affected	Document #	New rev #
Emulator 2 Digital Backload Rev 2 Assy Drwg	A-6189-016	Rev B
Emulator 2 Digital Board Schemtics	A-6149-001	Rev 1.B

PCB affected	E-mu P/N	New rev #	Starting S/N

E-mu Systems, Inc.
Engineering Change Order

ECO #121

ECO by: W.S. Checked by: B.H.M. Appr. by: [signature] Date: 850607

Product affected: Emulator 2 Model #: 6018 / 6028

Approx. starting S/N: 400 / 955

This ECO is for: [x] In house use [x] Service Manual

The purpose for this ECO is: to eliminate reset problems do to powersupply failures.

FIX: On the powersupply (ZV301), remove and discard R103. Remove R104 and install RR350 at R103 location. Discard R104.

* RR350 is a 1/2W 75 ohm resistor.

This ECO is to be implemented on all:

- [ ] Finished goods
- [x] Units in process
- [x] Future units
- [ ] field units
- [ ] Units available for repair
- [x] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE325	Assy Emul2 Power Supply	[ ]	D	[x]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]

Documents affected	Document #	New rev #
Emul2 Powersupply Assy Instructions	A-6185-015	D

PCB affected	E-mu P/N	New rev #	Starting S/N

Emulator 2 Power Supply Assembly Rev D Doc # A-6185-015
850614

1. Cut the jumper wire on the voltage selector switch. With the switch in the 115 mode, mount it to the power supply bracket with the 115 opposite the AC connector and fuse cutouts.
2. Insert the fuse into the fuse housing and atttach the cover. Install the fuse housing, the ON/OFF switch, and the AC receptacle of the AC harness (P/N AE329) into their appropriate cutouts.
3. Plug the AMP pin on the GRN wire of the AC harness into hole #22 of the AMP connector (P/N JP307). Crimp AMP pins onto the WHT and BLK wires of the AC harness. Plug the pin on the BLK wire into hole #6 Plug the pin on the WHT wire into hole #8. Connect the BLK wire from the AC receptacle to one side of the fuse housing. Connect one end of the BLK wire with connectors on both ends to the opposite side of the fuse housing. Connect the other end of the same wire to one side of the ON/OFF switch. Install the four polarizing pins into the holes numbered 1, 3, 5, and 7 on the AMP connector.
5. Cut the BLU wire from location J103 on the power supply flush to the PCB. The wire should remain connected to location P101. Cut a piece of 22G BLU wire 4" long. Strip both ends 1/8". To one end, connect a female Molex pin. Insulate the Molex pin with a 2" piece of 1/8" heatshrink tubing and apply heat. Plug the Molex pin into location P102 on the power supply. Remove resistors R103 and R104. Reinstall a 75 ohm 1/2W resistor (P/N RR350) into location R103.
6. Attach the tie wrap stick-down (P/N HC121) on the power supply bracket (at the location directly under the transformer of the power supply PWA. Mount the power supply PWA to the bracket using four 4-40x1/4 BHMS (P/N HS301). The power supply should be positioned with location J102 towards the AC harness. Plug the AMP connector from the AC harness into location J102 on the power supply.
7. Strip the BLU wire from location P101 1/8". Slip a 1" piece of 1/8" heatshrink tubing over the wire, and solder the wire to the voltage selector switch at the upper center lead. Slip a 1/8" piece of heatshrink tubing over the BLU wire from location P102. Solder that wire to the upper left lead of the voltage selector switch. Slide the heatshrink tubing over the voltage selector switch leads. Insulate the remaining upper lead of the voltage selector switch with heatshrink tubing. Apply heat to the heatshrink tubing.
8. Attach the adhesive backed rubber feet to the power supply bracket on the underside (opposite the power supply) 1/2" in from either corner.
9. Test the power supply assembly according to the test procedure.

E-mu Systems, Inc.
Engineering Change Order

ECO # 122

ECO by: B.H.M. Checked by: S.D. Appr. by: m Date: 850610

Product affected: Emulator 2 Model #: 6018/6028

Approx. starting S/N: 400 / 955

This ECO is for: [X] In house use [X] Service Manual

The purpose for this ECO is: to increase the reset time period on the Z80CPU so that the display will have time to reset prior to the CPU writing to it.

Fix: Change R9 from a 10k 5% 1/4W to a 22k 5% 1/4W.

This ECO is to be implemented on all:

- [ ] Finished goods
- [ ] field units
- [ ] Units in process
- [ ] Units available for repair
- [x] Future units
- [x] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE312	Assy Emul2 Digital Wave Solder	[x]		[x]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]

Documents affected	Document #	New rev #
Emulator 2 Digital Rev 1 Schemtics	S-6149-001	C

PCB affected	E-mu P/N	New rev #	Starting S/N

E-mu Systems, Inc.
Engineering Change Order

ECO # 123

ECO by: B.H.M. Checked by: D.M. Appr. by: [signature] Date: 850610

Product affected: Emulator 2 Model #: 6018 / 6028

Approx. starting S/N: 400 / 955

This ECO is for: [X] In house use [X] Service Manual

The purpose for this ECO is: to add a pull down resistor to keep the +DSR.V signal false to prevent spurious indication of the presence of a terminal. Combination of break on MIDI or RS422 and DSR true causes software to invoke monitor which has been deleted - cuts off MIDI.

NOTE: This ECO only applies to Digital PCB art rev 1 boards only.

This ECO is to be implemented on all:

- [X] Finished goods
- [X] Units in process
- [X] Future units
- [ ] field units
- [ ] Units available for repair
- [X] Units that problem exists

Parts affected:

E-mu P/N	Part description:	BOM	New rev #	Attached
AE311	Assy Emul2 Digital Backload Assy	[X]	C	[X]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]
		[ ]		[ ]

Documents affected	Document #	New rev #
Emulator 2 Rev1 Digital PWA Bkld Assy Drwg	A-6189-016	C
Emulator 2 Rev1 Digital Schematic	S-6149-001	C

PCB affected	E-mu P/N	New rev #	Starting S/N

E-2 parts list

Part numbering conventions.

1. Capacitors

CA = Aluminimum Electrolitic
CC = Cermanic
CM = Mica
CP = Plastic (Polystyrene)
CT = Tantalum

2. Connecters

JA = Jack
JC = IC Socket
JP = Plug
JR = Ribbon Cable Connecter

3. Resistors

RR = 5%
RP = 1%
RN = Resistor Pack
RT = Trimmer Pot
RC = Potienometer

4. IC's

IC = CMOS
II = Interface
IL = Linear
IM = NMOS
IT = TTL or Equivlent

5. Hardware

EM = Metal Enclosure or Bracket
HC = Cable ties and Clamps
HK = Knobs
HN = Nuts
HS = Screws and Spacers
HW = Washers
SW = Switch

6. Miscellaneous

DD = Diode
FI = Instruction Manual
OE = Optoisolater
QQ = Transistor
ZX = Chrystal
WW = Wire
ZH = Heatshrink
ZK = Keyboard
ZR = Rubber foot
ZV = Power supply

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OUTPUT PCB

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Capacitors

Value	E-MU P/N	Ref. Desg.
10 pf	CC301	C28,C29,C76
33 pf	CC329	C49
47 pf	CC326	C39
100 pf	CC103	C85,C166-C174
470 pf	CM300	C68-C75,C77-C84
470 pf	CC305	C104,C106
1000 pf	CC106	C41-C48,C50-C59,C60-C65
2000 pf	CC327	C114-121
3900 pf	CC325	C138-C145
4700 pf	CP108	C40
.02 uf	CC313	C122-C129,C147-C154
.1 uf	CC314	C1-C5,C11-C26,C30-C38,C96-C103 C105,C163,C164
1 uf	CT315	C27,C87-C95
3.3 uf	CT320	C130-C137
4.7 uf	CT319	C86
4.7 uf	CA323	C66,C67
10 uf	CT317	C6-C10,C165

Integrated Circuits

Type	E-MU P/N	Ref. Desg.
S3528 Digital Filter	II334	~~IC46-IC53~~ IC 78-86
4051 Mux.	IC208	IC77,IC87,97
4559 SAR	IC133	IC11
6072 COMDAC	II305	IC54-IC61
7524 MDAC	IC63	IC63
TL084 Op-Amp	IL302	IC44,IC64,IC66,IC67,IC69 IC70,IC72,IC73,IC75
LF311 Comparator	IL332	IC62
LF356 Op-Amp	IL301	IC46-IC53
2045 LPF	IL315	IC88-IC95
DG202 Analog Switch	IL319	IC96
13202 Analog Switch	IL316	IC65A,IC65B,IC68A,IC68B IC71A,IC71B,IC74A,IC74B
MC3404 Op-Amp	IL320	IC96
7805 +5 Regulator	IL307	VR2
7905 -5 Regulator	IL112	VR1
8254-2 Timer	IM341	IC1,IC2,IC3

74LS04	IT306	IC7,IC16,IC19,IC22
74LS08	IT105	IC8,IC15,IC18,IC21,IC24
74LS11	IT107	IC25
74LS27	IT317	IC28,IC31,IC32,IC35,IC36 IC39,IC40
74LS32	IT308	IC4,IC5
74LS37	IT321	IC43
74LS74	IT310	IC10,IC14,IC17,IC20,IC23
74LS86	IT328	IC9
74LS138	IT311	IC6,IC27
74LS151	IT326	IC26
74LS174	IT327	IC45
74LS244	IT329	IC12,IC13
74LS393	IT325	IC29,IC30,IC33,IC34,IC37 IC38,IC41,IC42

Resistors

Value	E-MU P/N	Ref. Desg.
100 ohm	RR301	R103
200 ohm 1%	RP307	R20-R27
470 ohm	RR106	R76-R83
1 kohm 1%	RP102	R106-R113
1 kohm	RR305	R115,R156-R163
2.49 kohm 1%	RP301	R2-R9,R11-R18
4.7 kohm	RR307	R1,R60-R67,R85-R92,R94-R101 R104,R148-R155
5 kohm trimmer	RT306	RT1
10 kohm rpack	RN318	RN1
10 kohm 1%	RP106	R28-R35
10 kohm	RR309	R45,R48,R52-R59,R68-R74,R75 R93,R102,R105,R164-R171
11 kohm	RR310	R51
22 kohm	RR313	R114,R140-R147
22.6 kohm 1%	RP303	R116-R123
33 kohm	RR316	R46,R47
68 kohm	RR346	R132-R139
124 kohm	RR304	R124-R131
100 kohm	RR318	R10,R19,R40,R84
110 kohm	RR342	R50
1 mohm	RR325	R49

Connecters

Type	E-MU P/N	Reference Designator
IC socket 8 Pin	JC102	
IC Socket 14 Pin	JC103	
IC Socket 16 Pin	JC311	
IC Socket 18 Pin	JC105	
IC Socket 20 Pin	JC106	

IC Socket 24 Pin	JC107	
1/4" Phone Jack	JA301	J1-J10
Molex PC Conn. 3 Pin	JP110	CN1,CN6
Molex PC Conn. 9 Pin	JP112	CN9
36 Pin Header	JR306	CN8A,CN8B

Miscellaneous

Type	E-MU P/N	Ref. Desg.
1N914 Diode	DD301	D1-D5

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DIGITAL PCB

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Capacitors

Value	E-MU P/N	Ref. Desg.
68 pf	CM117	C111
1000 pf	CC106	C112,C140
.01 uf	CC311	C138
.01 uf 20%	CC312	C87
.02	CC313	C162
.1 uf	CC314	C2,C3,C24,C26,C27,C30,C33, C34-C40,C42,C46,C51-C60,C64 C67,C72-C79,C86,C90,C93,C96 C99,C101,C103,C105,C108,C110 C113,C114,C118,C121,C124,C127 C130,C132,C134,C137,C141,C142 C144,C147,C150,C153,C156,C159 C161,C115
10 uf	CT317	C63,C81-C83

Connectors

Type	E-MU P/N	Ref. Desg.
1/4 Phone Jack Mono	JA301	J1-J5
1/4 Phone Jack Stereo	JA306	J6
IC Socket 8 Pin	JC102	
IC Socket 14 Pin	JC 103	
IC Socket 16 Pin	JC311	
IC Socket 18 Pin	JC105	
IC Socket 20 Pin	JC106	
IC Socket 24 Pin	JC107	
IC Socket 28 Pin	JC308	
IC Socket 40 Pin	JC309	

36 Pin Piggyback Socket	JI304	CN15,CN16
5 Pin DIN Conn. (MIDI)	JI302	CN13,CN14
DB25 Conn. (RS232)	JI305	CN12
Molex PC Conn. 9 Pin	JP112	CN9
34 Pin Ribbon Conn.	JR123	CN11
26 Pin Ribbon Conn.	JR300	CN10
50 Pin Ribbon Conn.	CN3	JR301
36 Pin Mating Conn. Male	CN8,CN8	JR304

Intregrated Circuits

Type	E-MU P/N	Ref. Desg
6N138	OE300	IC133
4070	IC131	IC131
6116 SRAM	IC343	IC29,IC59
74C244	IC341	IC5
1488 RS232 Driver	II143	IC132
1489 RS232 Reciever	II144	IC108
2651 UART	II335	IC107
ADC0809 A/D	II336	IC27
4164 DRAM	IM338	IC13-IC20,IC32-IC39,IC51-IC58 IC71-IC78
2149 SRAM	IM339	IC142-IC147
Z-80A CTC	IM346	IC45,IC60
Z-80A CPU	IM343	IC21,IC66
Z-80A DMA	IM342	IC82
Z-80A PIO	IM345	IC24,IC46
Z-80A SIO/2	IM344	IC128
PROM UCD0.6	IP319	IC137
2764 EPROM Main	IP317	IC42
2764 EPROM Scanner	IP318	IC28
PROM UCD11.1	IP308	IC135
74LS00	IT305	IC81
74S00	IT342	IC7,IC8
74LS04	IT306	IC25,IC48
7407	IT104	IC1,IC22
74LS08	IT105	IC84,IC115
74LS10	IT106	IC43,IC129
74S10	IT340	IC67
74LS11	IT107	IC2
74LS14	IT307	IC62
74LS20	IT351	IC44
74LS32	IT308	IC26,IC41,IC83,IC109
74S37	IT339	IC12,IC30,IC89,IC90,IC99,IC116
74LS42	IT309	IC3,IC4
74LS54	IT346	IC88
74LS74	IT310	IC87,IC61,IC92,IC105
74S74	IT337	IC68
74LS86	IT328	IC117
74LS92	IT344	IC91
74LS112	IT336	IC23,IC85,IC113,IC114
74S112	IT350	IC49
74LS138	IT311	IC47,IC80,IC86

74S138	IT345	IC11,IC98
74S161	IT331	IC111,IC112
74LS164	IT348	IC110
74S174	IT149	IC140
74S175	IT334	IC31,IC141
74LS221	IT316	IC106,IC130
74LS240	IT373	IC79
74LS244	IT329	IC6,IC9,IC65,IC94,IC95,IC104
74S244	IT332	IC50,IC70,IC118
74S283	IT343	IC123-IC127
74LS374	IT321	IC40,IC96,IC97,IC100-IC103, IC119-122
74LS393	IT325	IC63
74S374	IT330	IC10,IC69,IC136,IC138,IC148, IC150,IC152
74LS670	IT324	IC64

Resistors

Value	E-MU P/N	Ref. Desg.
100 ohm	RR301	R34
270 ohm	RR347	R10
330 ohm	RR305	R7,R13
680 ohm	RR343	R6
1 kohm	RR305	R22-R26,R33,R36,R37
1.8 kohm	RR344	R3
4.7 kohm	RR307	R1,R8,R11,R15,R27-R29,R31,R32
4.7 kohm RPACK	RN319	RN1
10 kohmh	RR309	R9,R16,R17,R35,R39,R45
15 kohm	RR311	R20
47 kohm	RR122	R30,R44
48.7 kohm	RP310	R18
90.9 kohm 1%	RP110	R21
100 kohm	RR318	R38
226 kohm	RP309	R19
1 mohm	RR325	R40

Miscellaneous

Type	E-MU P/N	Ref. Desg.
1N914 Diode	DD301	D1-D6
2N4121 Transistor	QQ101	Q2
2N5172	QQ302	Q1,Q3
Xtal 20.0 Mhz	ZX304	Y1

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MEMORY PIGGYBACK PCB

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Capacitors

Value	E-MU P/N	Ref. Desg.
.1 uf	CC314	C1-C37

Connectors

IC Socket 14 Pin	JC103	
IC Socket 16 Pin	JC311	
IC Socket 20 Pin	JC106	
Piggyback Conn. 36 Pin	JI303	CN15,CN16

Integrated Circuits

4164 DRAM	IM338	IC2-IC9,IC11-IC18,IC20-IC27 IC29-IC36
74S244	IT332	IC19,IC28
74S175	IT334	IC10,
74S37	IT339	IC1
74LS240	IT373	IC37

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LEFT PANEL PCB

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Capacitors

Value	E-MU P/N	Ref. Desg.
.1 uf	CC314	C1,C2
1 uf	CT315	C3

Connectors

Type	E-MU P/N	Ref. Desg.
IC Socket 16 Pin	JC101	CN1
IC Socket 20 Pin	JC106	IC1
Molex PC Conn. 3 Pin	JP110	CN6
Molex PC Conn. 6 Pin	JP111	CN7
50 Pin Ribbon Conn.	JR310	CN3

IC's

Type	E-MU P/N	Ref. Desg.
74LS174	IT327	IC2,IC3
74LS273	IT317	IC1

Resistors

Value	E-MU P/N	Ref. Desg.
330 ohm RPACK	RN315	RN1,RN2
523 ohm 1%	RP308	R1
5 kohm Trimmer	RT306	RT6,RT7
10 kohm 1%	RP106	R2
10 kohm Pot	RC302	RT5
10 kohm Slider Pot	RC311	RT1-RT4

Switchs

Type	E-MU P/N	Ref. Desg.
Pushbutton Red	SW306	SW11
Pushbutton Black	SW307	SW1-SW10,SW12-SW30

Misc.

Type	E-MU P/N	Ref. Desg.
1N914 Diode	DD301	D1-D21
LED Red	LP302	LP1-LP10
LCD Display	LP304	
4-40 3/8 Screw	HS302	
4-40 Nut	HN304	
3/8 32 Nut for Pot	HN311	
Nylon Spacer for Slider	HS305	
Nylon Spacer on Display	HW210	
14 Wire Flexstrip	WW313	
Power Supply for LCD	ZV300	VR1

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RIGHT PANEL

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Type	E-MU P/N	Ref. Desg.
DIP Plug 16 Pin	JC101	CN1
Molex Body Cable 3 Pin	JP130	
Molex Pin Female	JP305	
Molex Pin Male	JP306	

330 ohm RPACK	RN315	RN1,RN2
Red Pushbutton	SW306	SW1
Black Pushbutton	SW307	SW2-SW9
1N914 Diode	DD301	D1-D9
LED	LP302	LP1-LP9
10 kohm Pot	RC302	
Heatshrink 1/16	ZH305	
Tie Wrap	HC302	
2 Cond. Shielded Wire	WW312	
3/8 32 Nut for Pot	HN311	

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WHEEL ASSEMBLIES

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Type	E-MU P/N	Quantity
Wheel Bracket	EM331	2
Plastic Wheel	EP318	2
Left Wheel Spring	HB300	1
Spring Retainer Clip	HW321	1
Tie wrap Medium	HC118	1
Tie Wrap Small	HC302	5
3/8-32 Nut	HN311	4
6-32 1/2" Allen Screw	HS103	2
3/8" Lock Washer	HW312	2
Molex Connector cable mount 6 pin	JP131	1
Molex Pin female	JP305	5
10 kohm Plastic Pot	RC101	1
10 Kohm Metal Pot	RC310	1
Orange 22 Ga. wire	WW124	2'
Violet 22 Ga. wire	WW125	2'
Green 22 Ga. wire	WW301	2.75'
Red 22 Ga. wire	WW302	2'
Blue 22 Ga. wire	WW304	2'
1/8" Heatshrink	ZH119	.25'

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POWER SUPPLY

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Type	E-MU P/N
AC receptacle	JP129
Amp Connector 8 Pin	JP307
Amp Polarizing Pin	JP308
Amp Pin	09
Bracket for mounting power supply	32
Cable stickdown	HC121
Fan 3"	ZE319

Fuse 2 amp slow blow	ZF102
Fuse holder	JC124
Fuse cap	JC137
Heatshrink 1/8"	ZH119
Heatshrink 1/16"	ZH105
L Bracket for fan mount	HE114
Nut 4-40 Kepf	HN304
Nut 8-32 Kepf	HN308
Power Switch	SW103
Quick Connect Lug	JL311
Screw 4-40 1/4"	HS301
Screw 8-32 3/8"	HS122
Slide Switch 115/230 Volt	SW107
Solder Lug #4	JL126
Switching Power Supply	ZV301
Tie wrap mini	HC302
Warning Sticker	ZL335
Wire 18 Ga. Black	WW101
Wire 22 Ga. Blue	WW304
Wire 18 Ga. Green	WW106
Wire 18 Ga. White	WW110

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CHASSIS

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Cables and Harnesses

Type	E-MU P/N
Disk Ribbon Cable	AE319
DC Power Cable	AE318
Front Panel Ribbon Cable	AE320
Interpanel Ribbon Cable	AE321
Keyboard Ribbon Cable	AE324
Volume Cable (shielded)	AE323
AC Power Cable (not power cord)	AE329

Miscellaneous

Type	E-MU P/N	Ref. Desg.
Blank Disk DSDD-	ZM323	
Bottom Panel	EM330	
Cable Stickdown	HC121	
Disk Drive Bracket	EM329	
Disk Drive	ZM302	
Disk Drive Mounting Screws	HS325	
Disk Label	ZL336	
Disk Set production sounds	ZD303	
Fish Paper for jack insulation on back panel	ZP319	
Housing	EP312	

GLOSSARY OF TERMS AND ABBREVIATIONS

This list covers all the terms found in this manual

A

A	Ampere
ac	Alternating Curent
ACK	Acknowledge
ADC	Analog to Digital Converter
ADDR	Address
ADSR	Attack Decay Sustain Release The function of
ALU	Arithmetic Logic Unit
ASSY	Assembly

B

B	Binary
BLK	Black
BLU	Blue
BRN	Brown

C

C	Capacitor
CAS	Column Address Strobe used on dynamic RAM's
CE	Chip Enable
CLK	Clock signal
CLR	Clear
cm	Centimeter
CMOS	Complementary Metal Oxide Semiconductor
CNTR	Counter
CPU	Central Processing Unit
CTC	Counter Timer Circuit
CS	Chip Select
CV	Control Voltage
CW	Clockwise

D

D0	Data Bit 0 (can be 0-7)
D	Diode
DAC	Digital to Analog Converter
db	Decibel
DC	Direct Current
DIP	Dual Inline Package
DMA	Direct Memory Access
DMM	Digital MultiMeter
DMUX	Demultiplexer
DRAM	Dynamic Random Access Memory
DVM	Digital Volt Meter

E

ECO	Engineering Change Order
EL	Electoluminescent
EOC	End of Conversion
EPROM	Eraseable Programmable Read Only Memory
EXT	External

G

GND	Ground
GRN	Green

H

HCT	High speed CMOS with TTL thresholds
HEX	Hexadecimal
HV	High Voltage
Hz	Hertz

I

IC	Integrated Circuit
IN	Input
INT	Interupt
I/O	Input/Output
IORQ	Input/Output Request

K

K	Kilo (thousand)

L

LCD	Liquid Crystal Display
LED	Light Emitting Diode
LFO	Low Frequency Oscillator
LIN	Linear
LOG	Logarithmic
LSB	Least Significant Bit
LSI	Large Scale Intergration

M

M	Mega (Million)
MA	Memory Address
MAX	Maximum
MEM	Memory
MHz	Megahertz
MIN	Minimum
MIDI	Musical Instrument Digital Interface
MOS	Metal Oxide Semiconducter
MSB	Most Significant Bit
MSI	Medium Scale Intergration
MUX	Multiplexer

N

n	Nano (10 -9)
NC	No Connection
NO	Normally Open
NVM	Non-Volatile Memory
NVRAM	Non-Volatile Random Access Memory

O

OEM	Original Equipment Manufacturer
ORG	Orange
OUT	Output

P

p	Pico (10 -12)
PB	Push Button
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIO	Parallel Input/Output
POT	Potentiometer A Weed
PROM	Programmable Read Only Memory
PS	Power Supply

R

R	Resistor
RAM	Random Access Memory
RAS	Row Address Strobe used on dynamic RAM'
REF	Reference
REV	Revision
RMA	Return Material Authorization
ROM	Read Only Memory
RQ	Request
RS-232	A standard serial computer interface
RST	Reset or Restart

S

S	Switch
SAR	Successive Approximation Register
S/H	Sample and Hold
SIO	Serial Input Output
SMPTE	Society of Motion Picture and Television Engineers
S/N	Signal to Noise Ratio
SRAM	Static Random Acess Memory
SYNC	Synchronization

T

TP	Test Point
TTL	Transistor Transistor Logic

U

uC	Microcontroller
UART	Universial Asyncronous Reciever Transmitter

V

V	Voltage
VAC	Volts Alternating Current
VCA	Voltage Controlled Amplifier
VCF	Voltage Controlled Filter

W

W	Wire
WHT	White

Y

YEL	Yellow