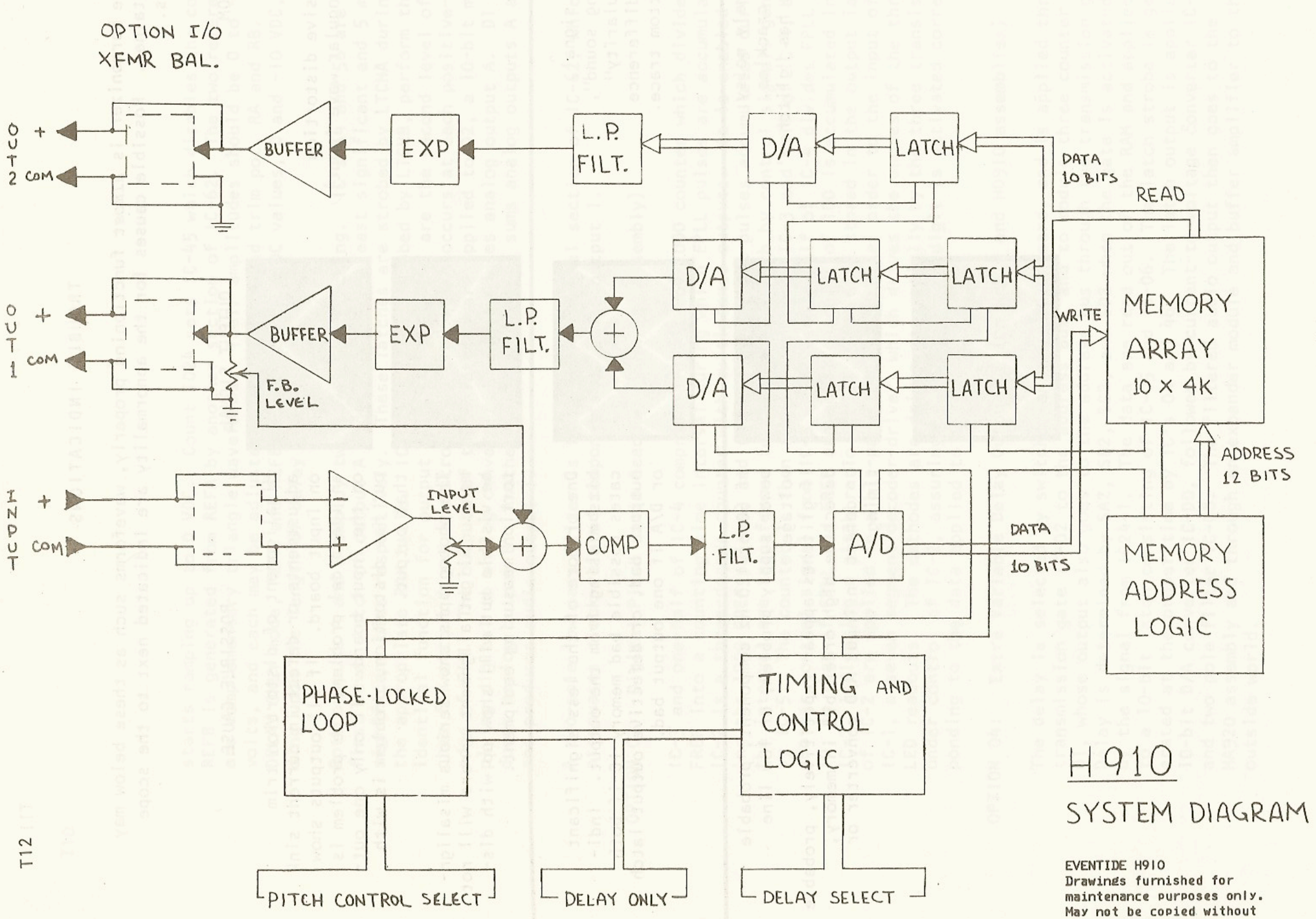
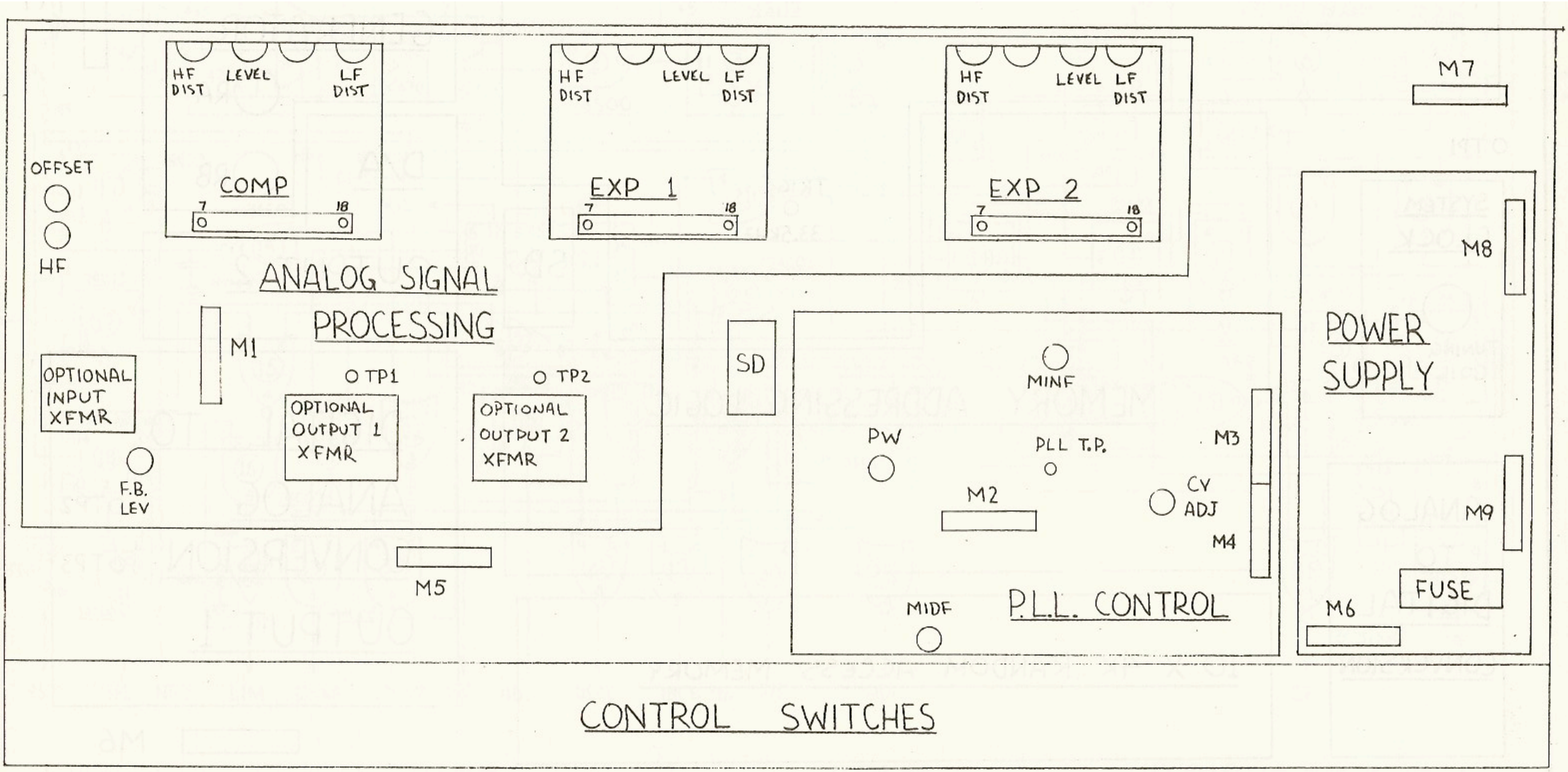
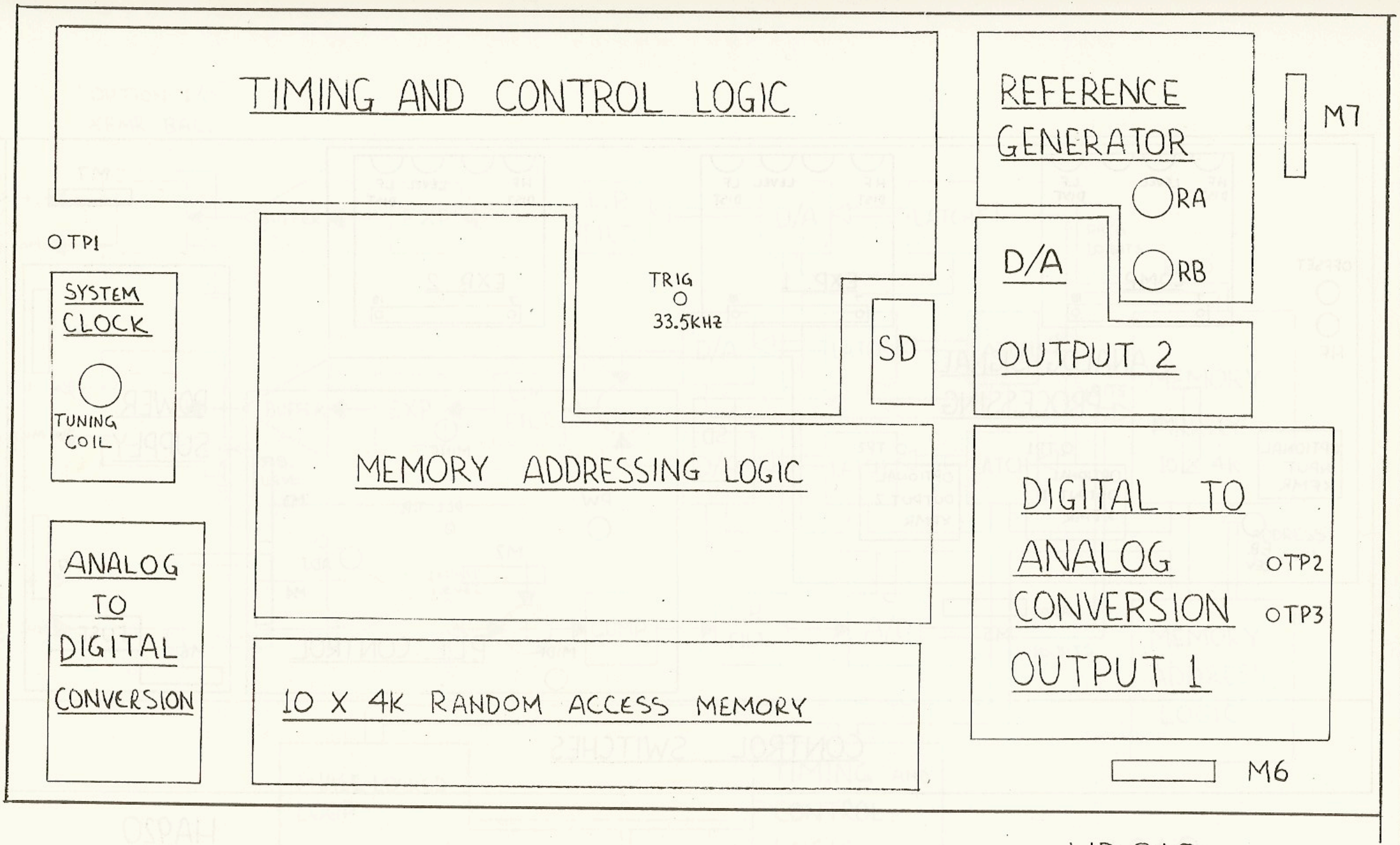


H910

SYSTEM DIAGRAM



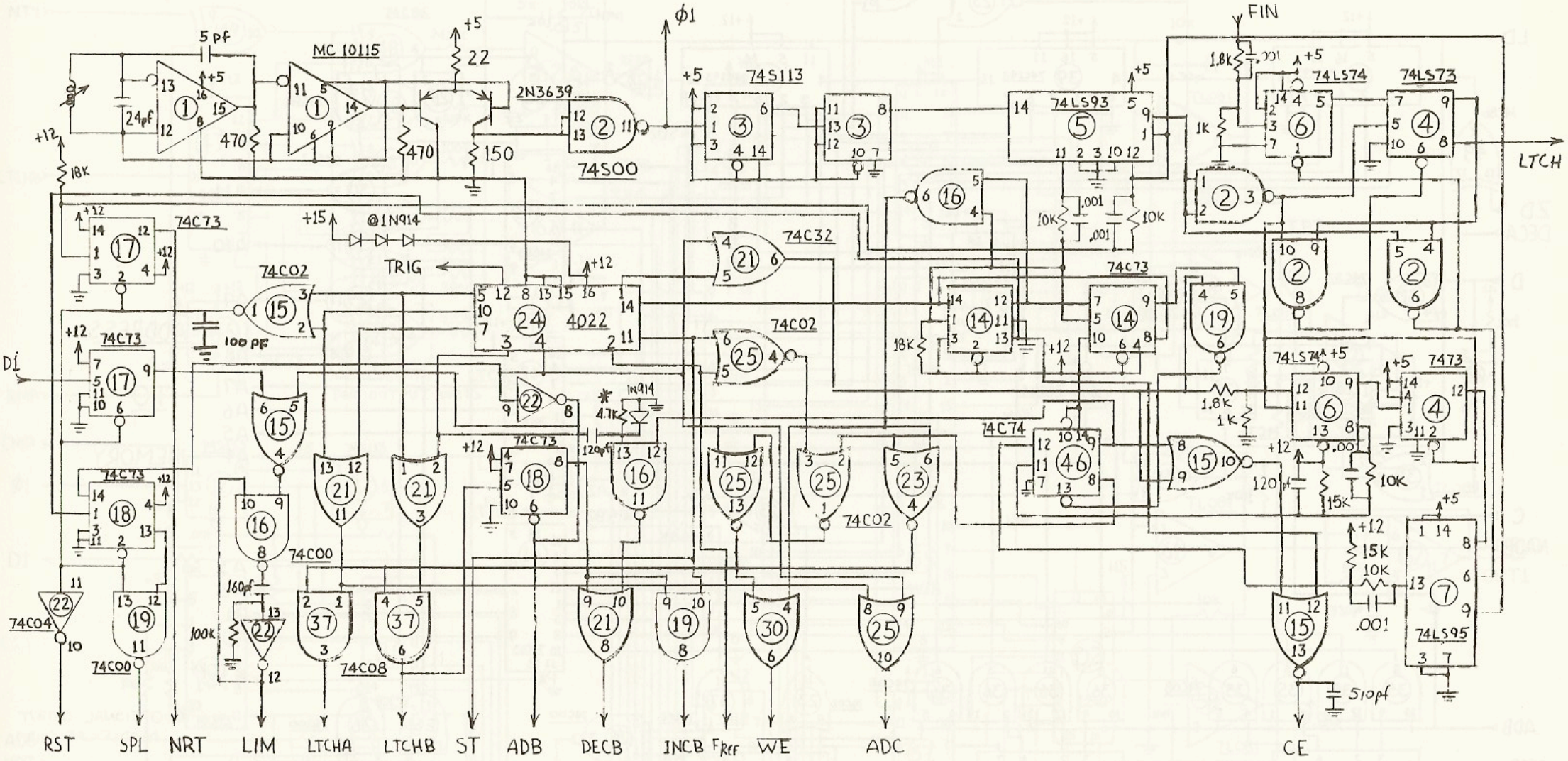
HA920
TOPOLOGY



HD910

TOPOLOGY

T14



* AVERAGE VALUE MIGHT VARY ± 1.5 KΩ

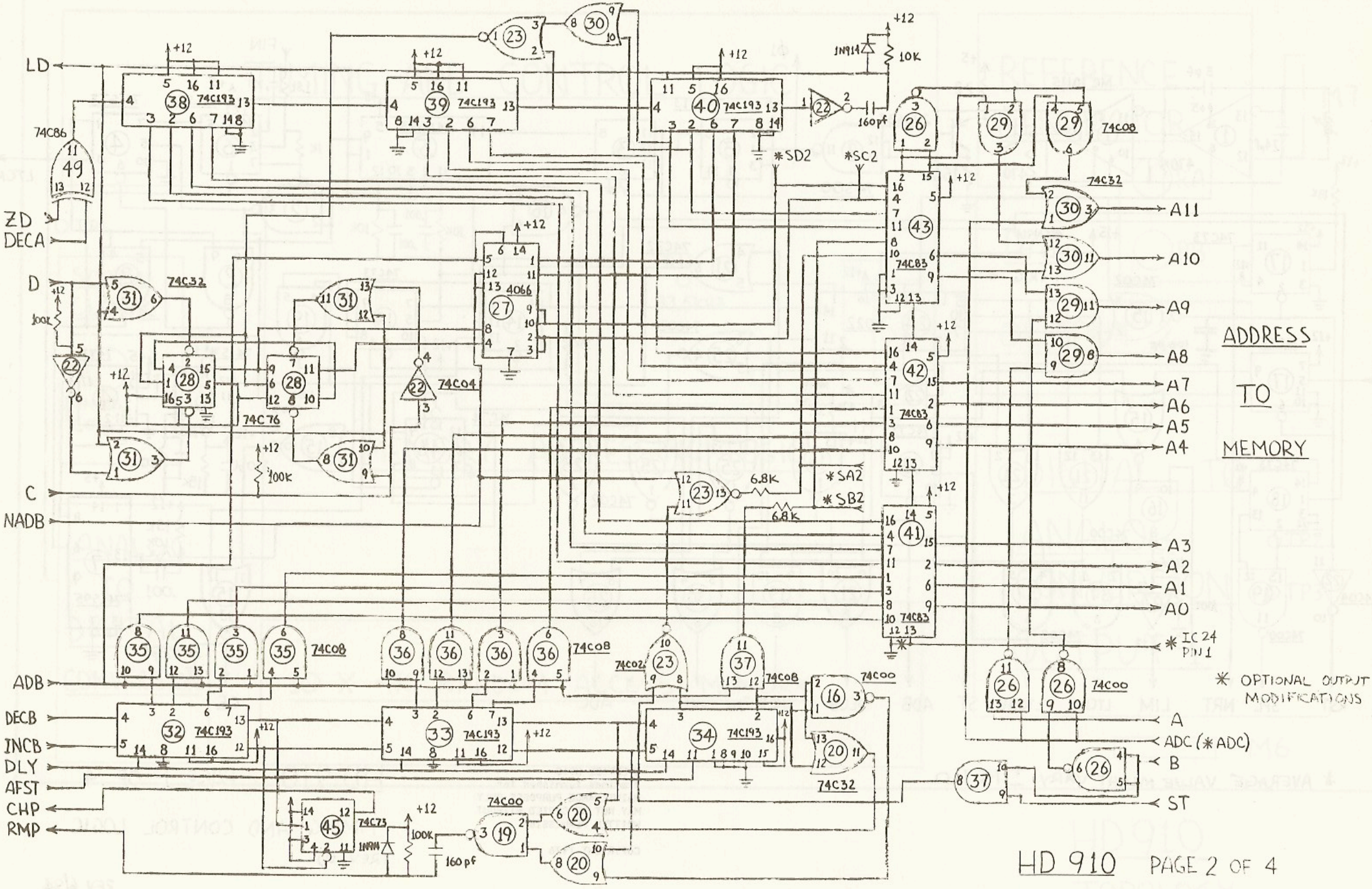
HD 910 PAGE 1 OF 4

TIMING AND CONTROL LOGIC

(REV. D)

REV 6/94

T15



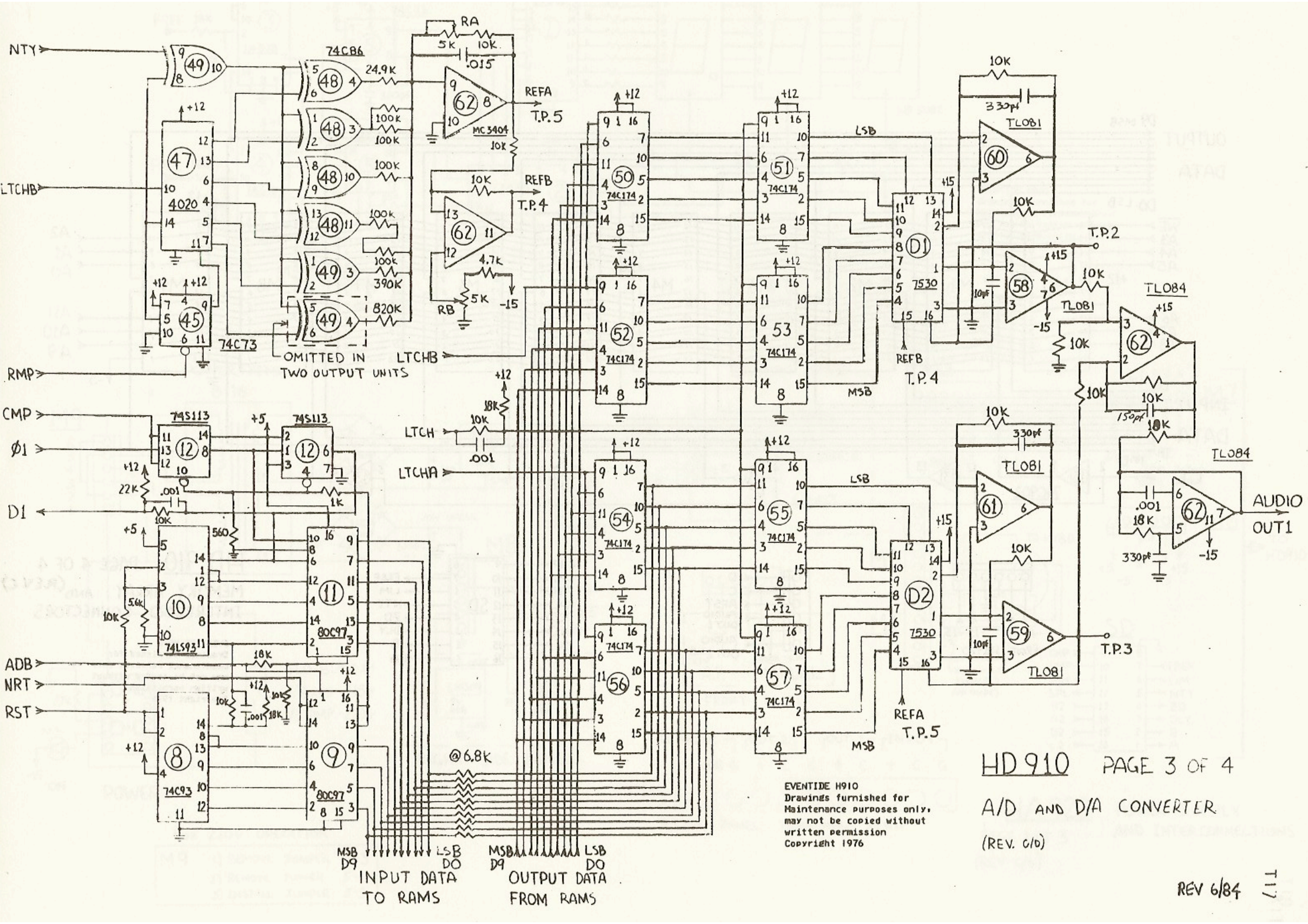
HD 910 PAGE 2 OF 4

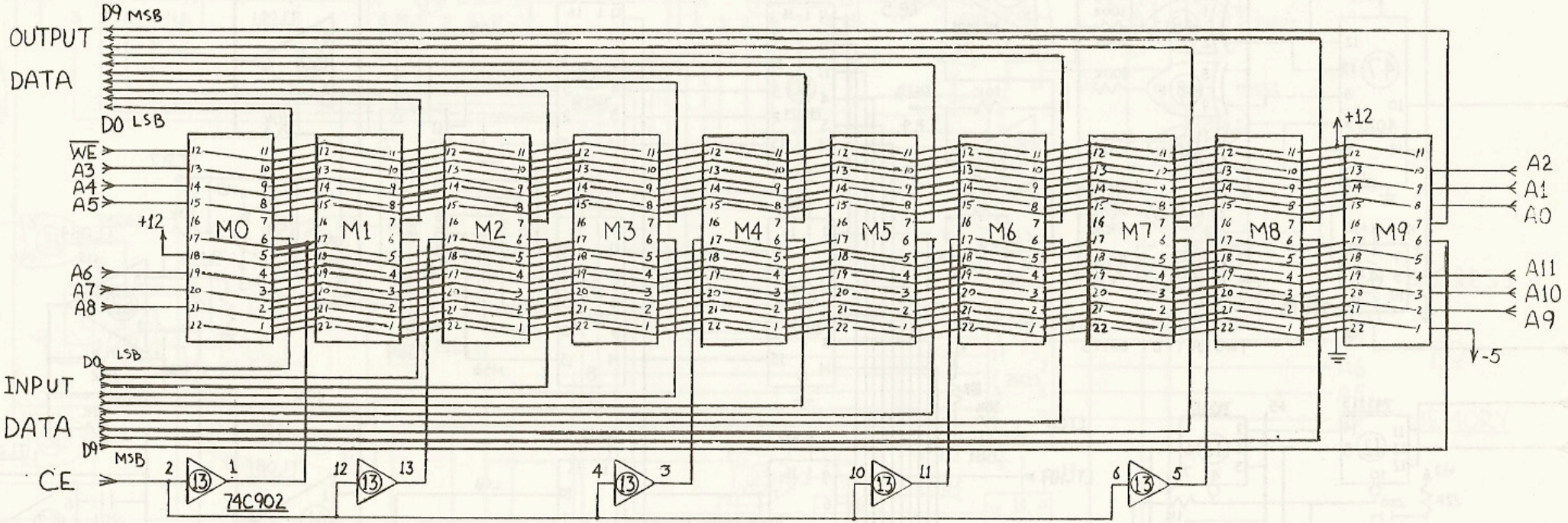
MEMORY ADDRESSING LOGIC

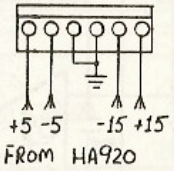
(REV. 5/0)

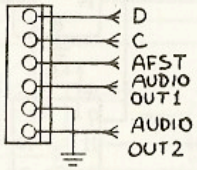
REV 6/84

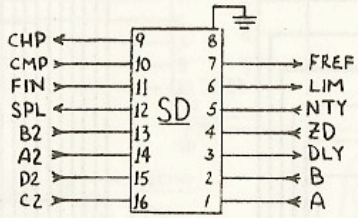
T16


NTY
LTCHB
RMP
CMP
Ø1
D1
ADB
NRT
RST
LTCHA
LTCH
74C86
74C73
4020
74LS113
74LS93
74C93
80C97
74C174
7530
MC3404
TL081
TL084
RA
5K
10K
.015
24.9K
100K
390K
820K
4.7K
RB
REFA
REFB
T.P.5
T.P.4
T.P.2
T.P.3
LSB
MSB
+12
+15
-15
+5
OMITTED IN TWO OUTPUT UNITS
@6.8K
MSB D9
LSB D0
INPUT DATA TO RAMS
OUTPUT DATA FROM RAMS
AUDIO OUT1
EVENTIDE H910
Drawings furnished for Maintenance purposes only, may not be copied without written permission
Copyright 1976
HD 910 PAGE 3 OF 4
A/D AND D/A CONVERTER
(REV. C/D)
REV 6/84





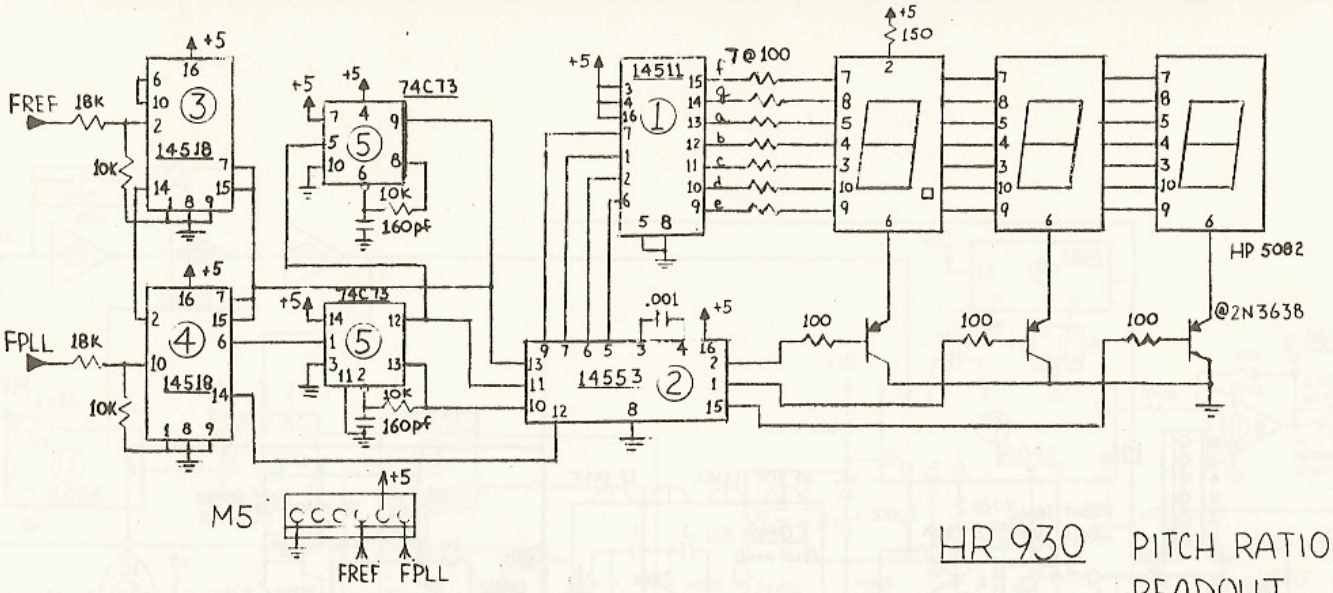




HD 910 PAGE 4 OF 4

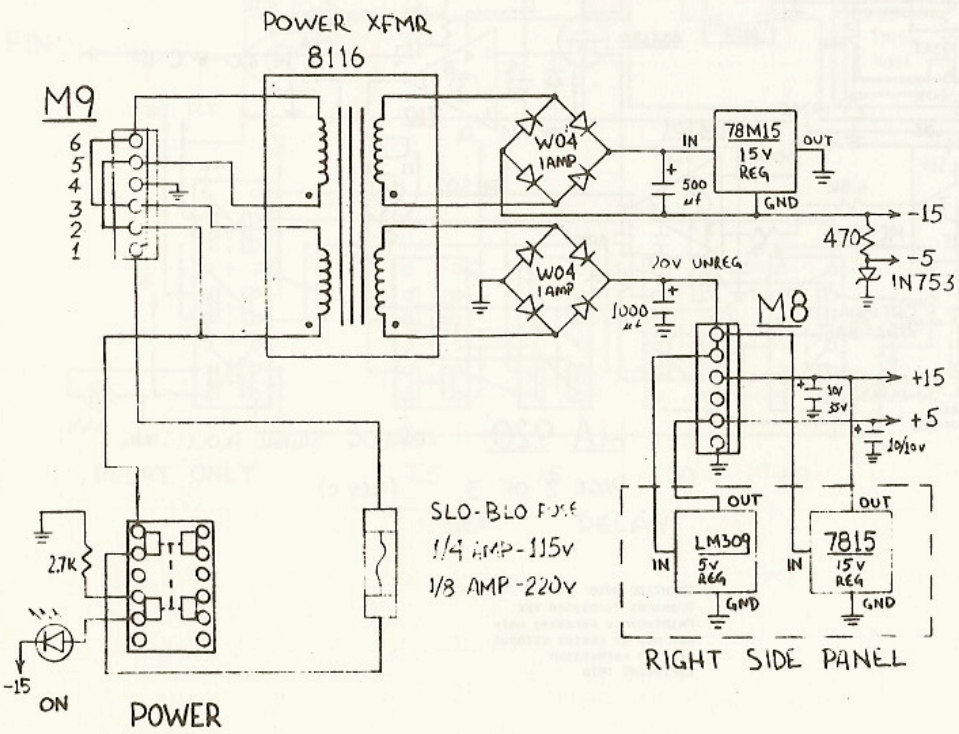
MEMORY ARRAY AND INTERBOARD CONNECTORS (REV.C)

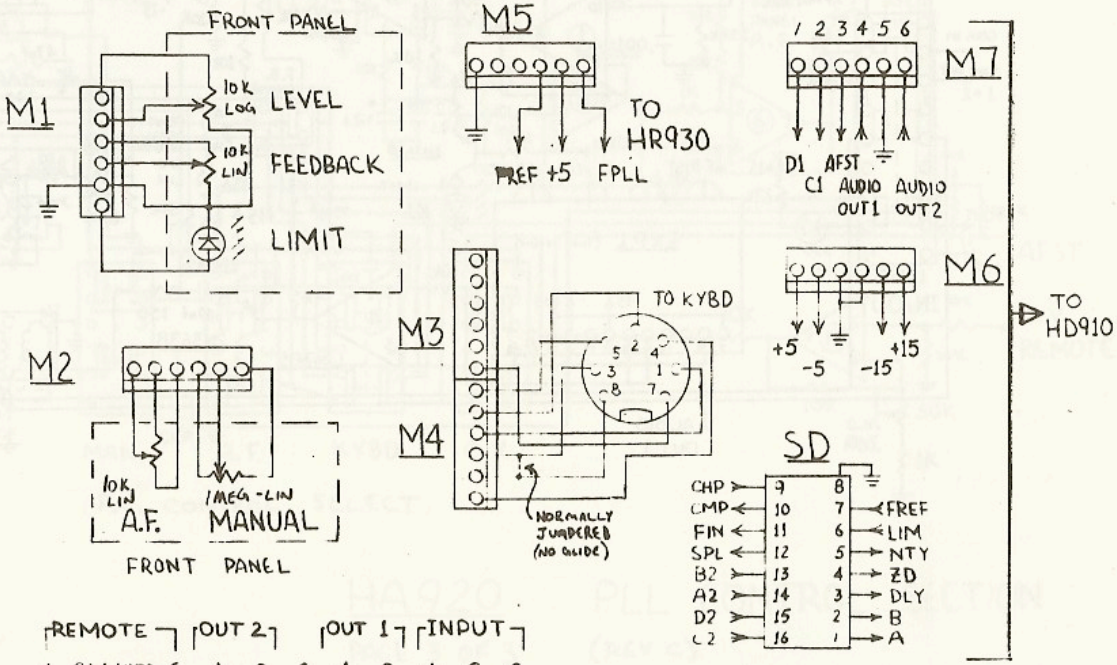
T18



EVENTIDE H910
Drawings furnished for
Maintenance Purposes Only
May not be copied without
written permission.
Copyright 1976

HR 930 PITCH RATIO READOUT





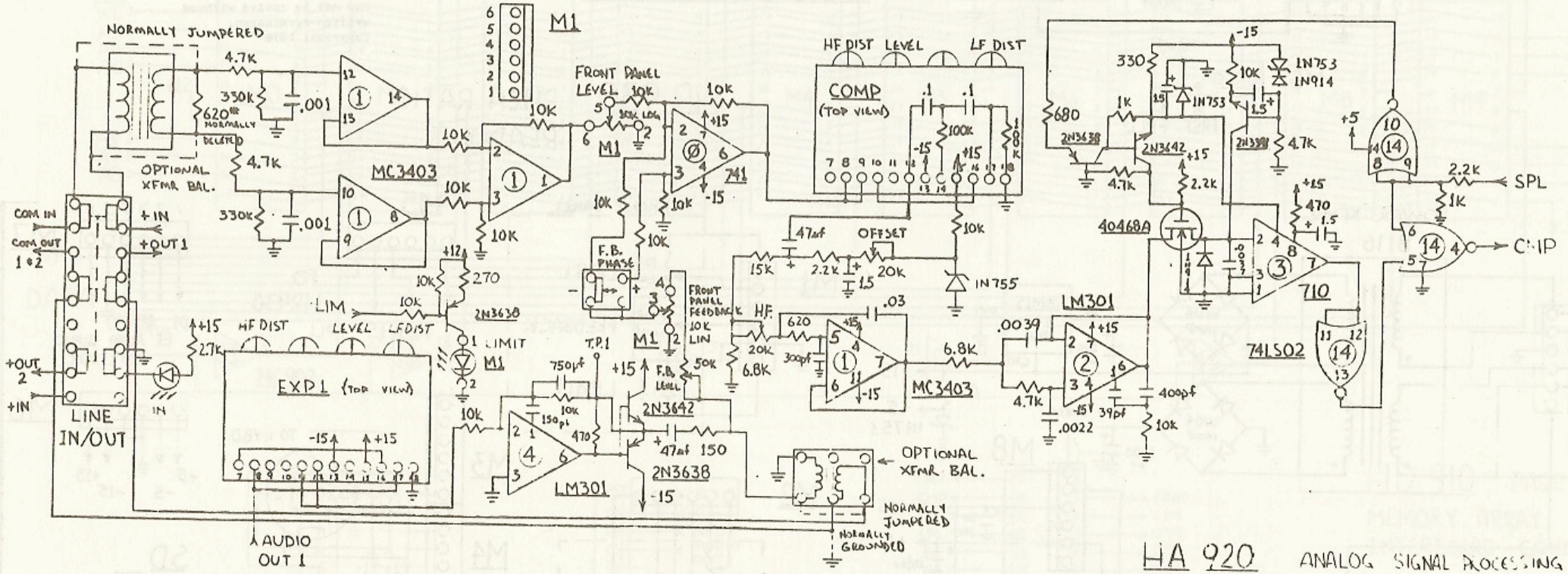
FOR 220V OPERATION

M9	1) REMOVE JUMPER	6-3
	2) REMOVE JUMPER	5-2
	3) INSTALL JUMPER	5-3

HA 920 POWER SUPPLY AND INTERCONNECTIONS

PAGE 1 OF 3
(REV C/D)

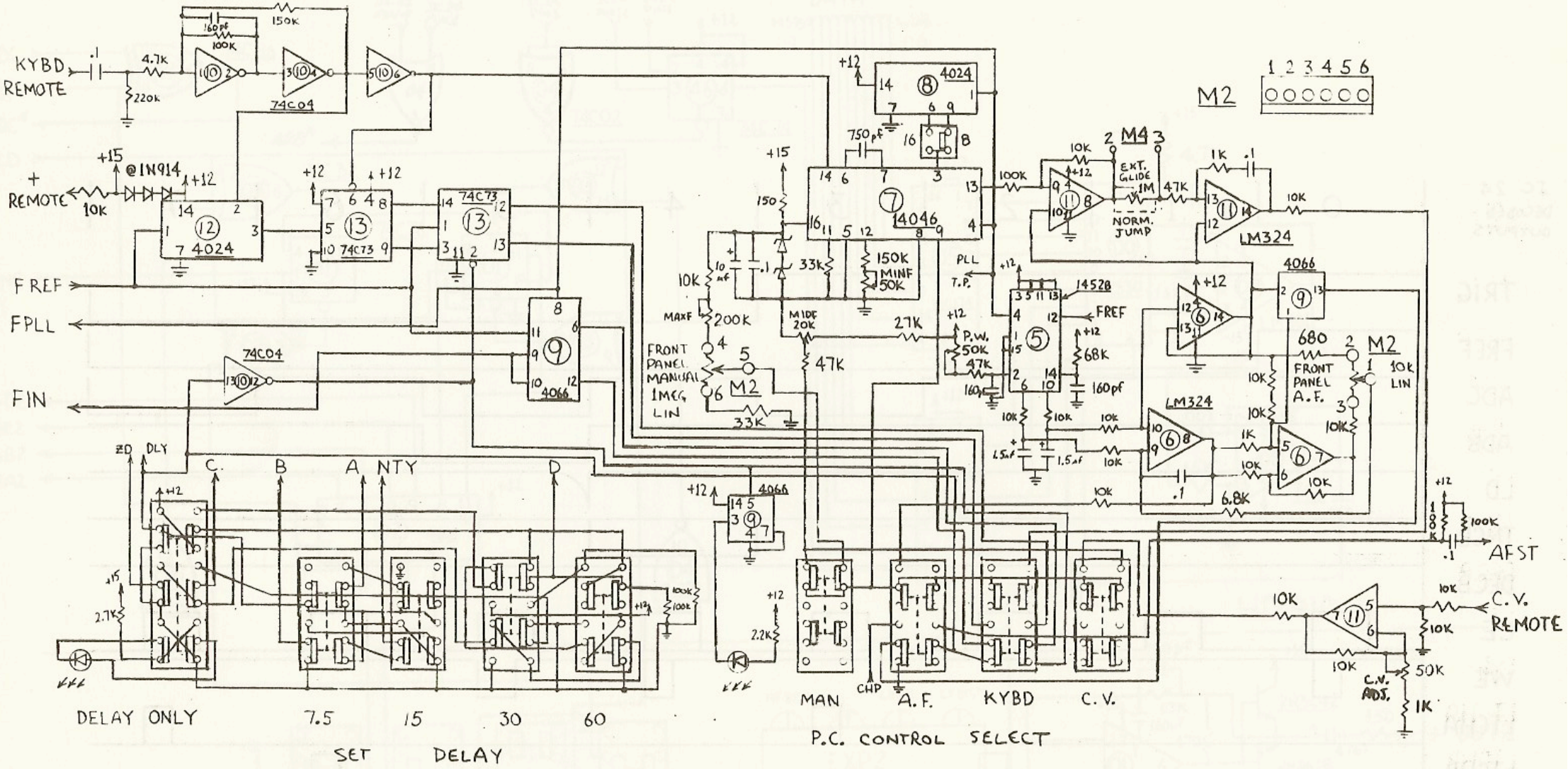
T19



HA 920 ANALOG SIGNAL PROCESSING

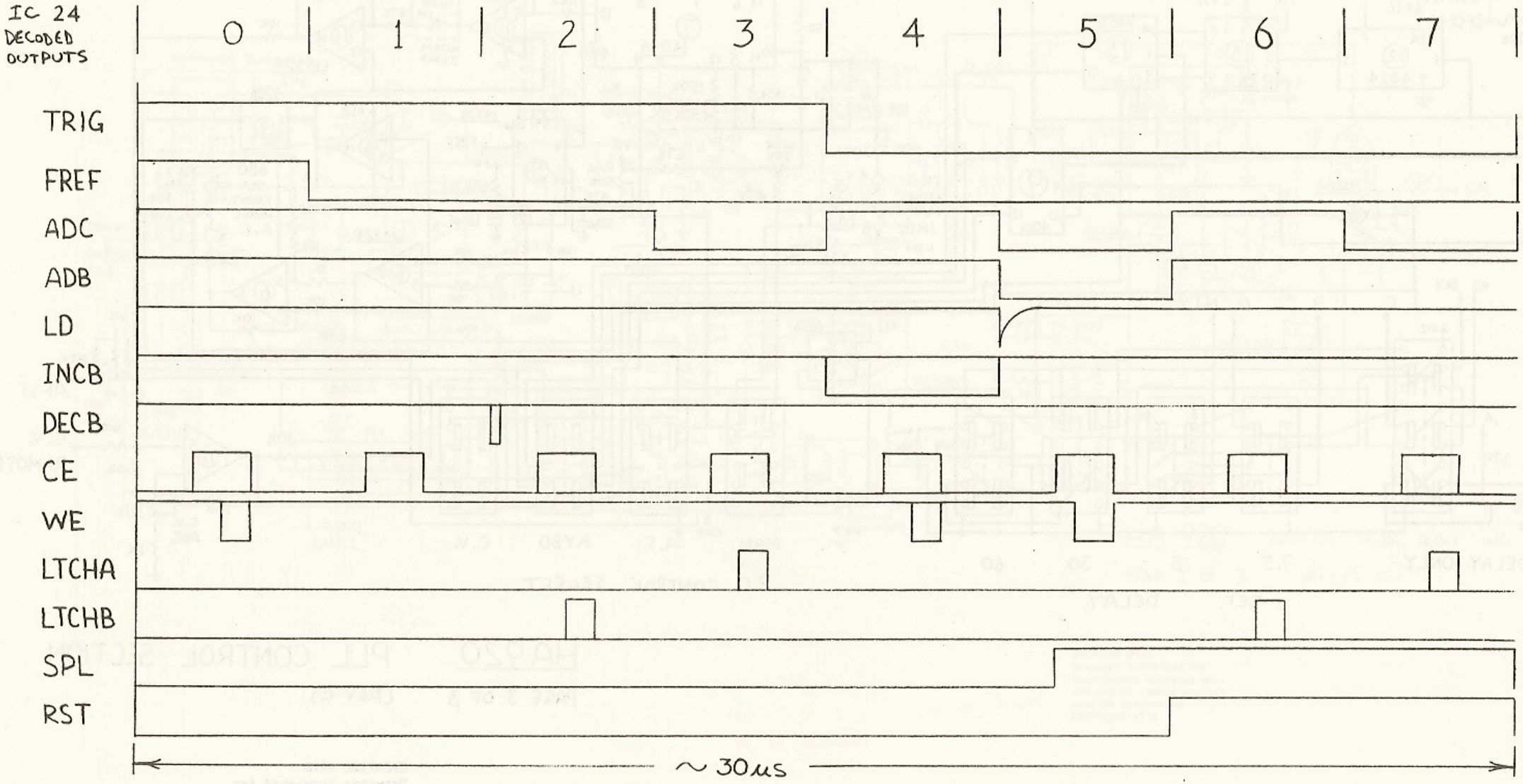
PAGE 2 OF 3 (REV C)

T20



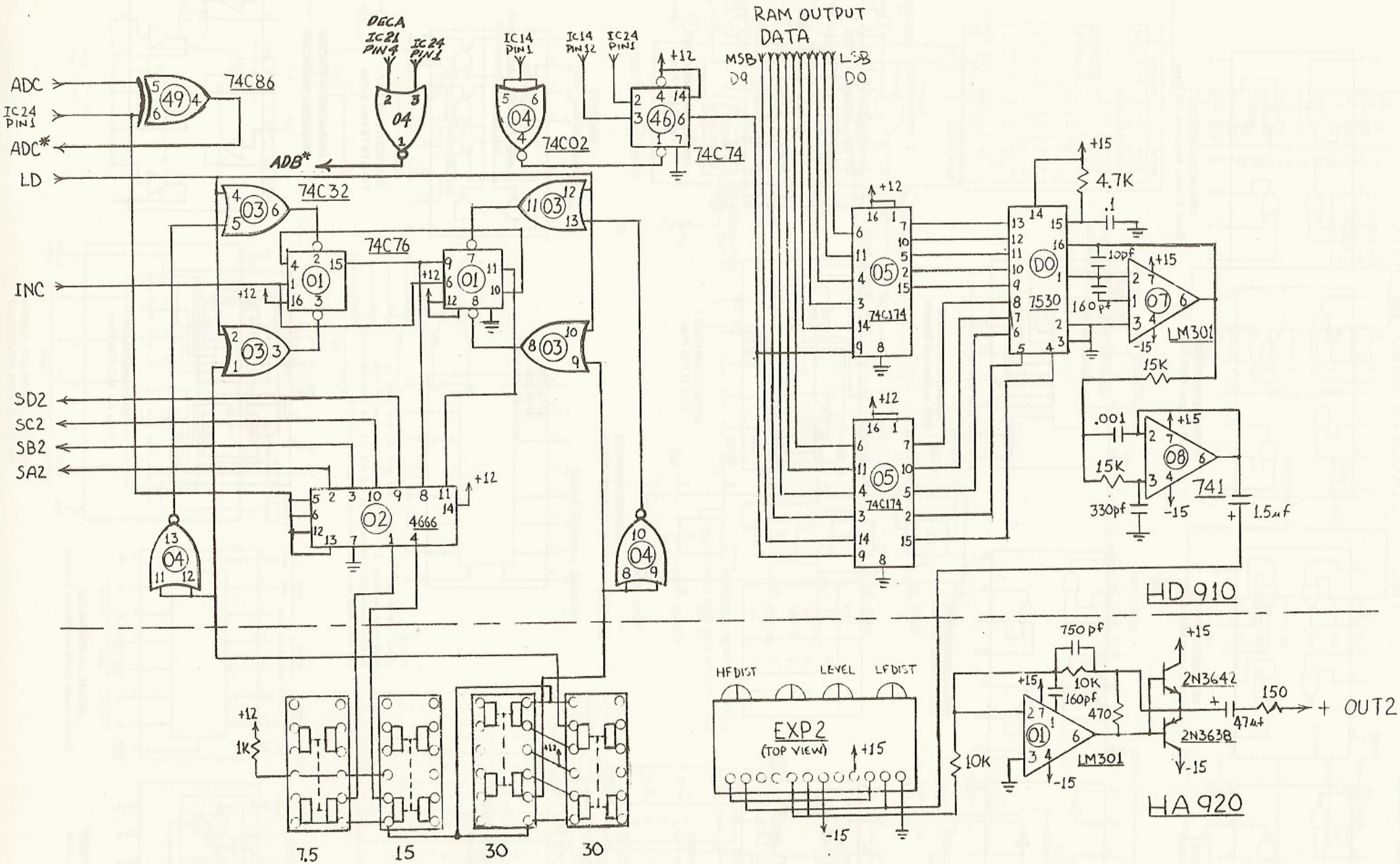
HA920 PLL CONTROL SECTION

PAGE 3 OF 3 (REV C)



HD 910 TIMING DIAGRAM

T22



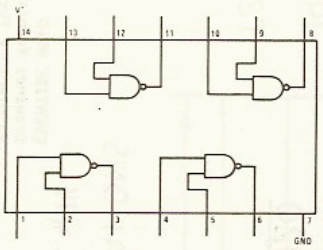
OPTIONAL OUTPUT

ADDITIONS AND MODIFICATIONS

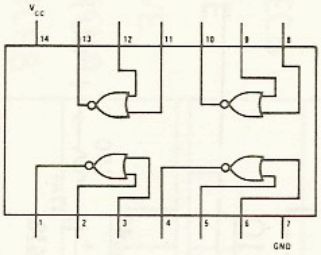
P.F.V. 11/84

T23

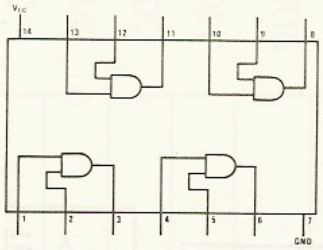
74C--- CIRCUITS USED IN H910



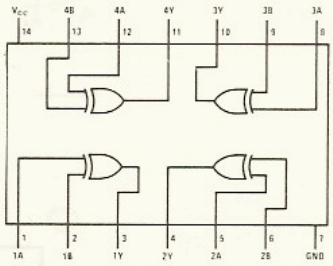
MM54C00/MM74C00
Quad 2-Input NAND Gate



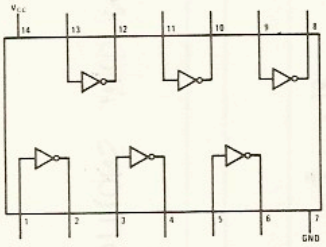
MM54C02/MM74C02
Quad 2-Input NOR Gate



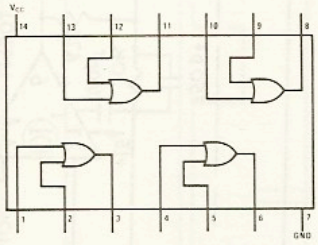
MM54C08/MM74C08
Quad 2-Input AND Gate



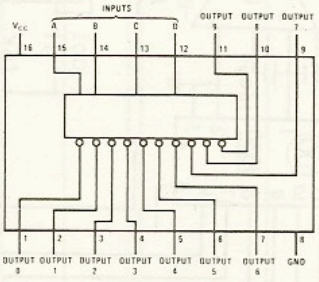
MM54C86/MM74C86
Quad 2-Input Exclusive OR Gate



MM54C04/MM74C04
Hex Inverter

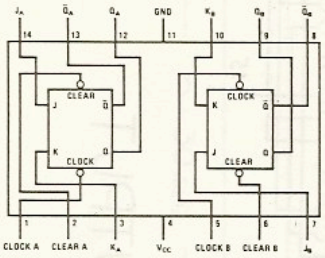


MM54C32/MM74C32†
Quad 2-Input OR Gate



MM54C42/MM74C42
BCD to Decimal Decoder

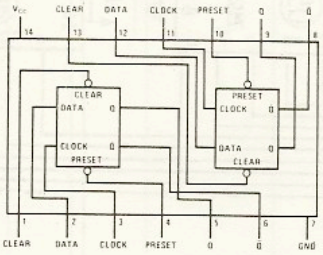
INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1



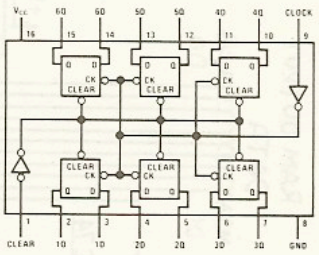
MM54C73/MM74C73
Dual J-K M/S Flip Flop

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.



MM54C74/MM74C74
Dual D Flip-Flop

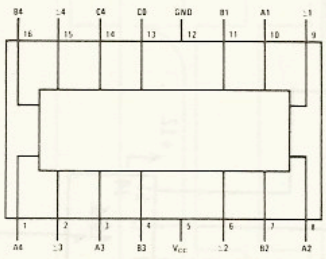


MM54C174/MM74C174†
Hex D Flip-Flop

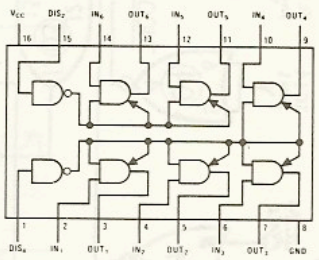
FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

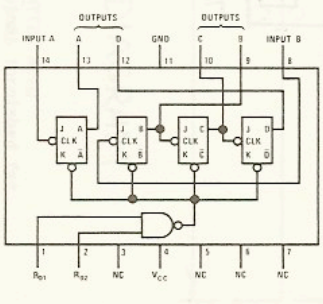
MM54C83/MM74C83
4-bit Binary Full Adder



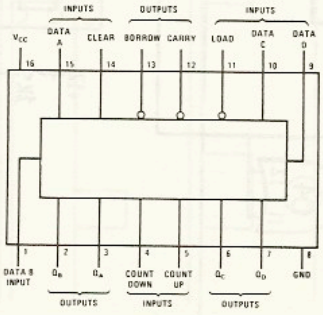
NOTE:
Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.



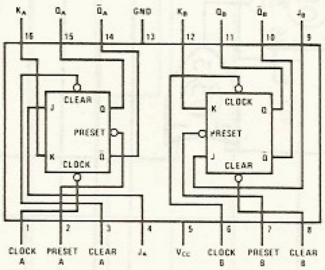
MM70C97/MM80C97
TRI-STATE Hex Buffer



MM54C93/MM74C93†
4-Bit Binary Counter

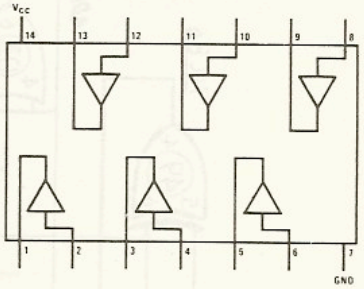


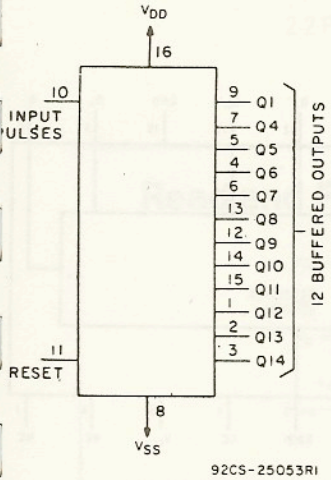
MM54C193/MM74C193
Synchronous Up/Down Binary Counter



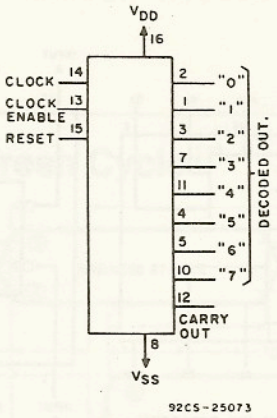
MM54C76/MM74C76
Dual J-K M/S Flip-Flop

MM54C902/MM74C902
MM54C904/MM74C904

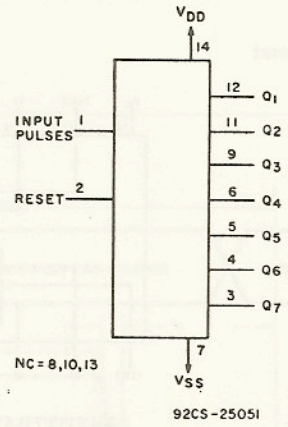




CD4020
14-Stage

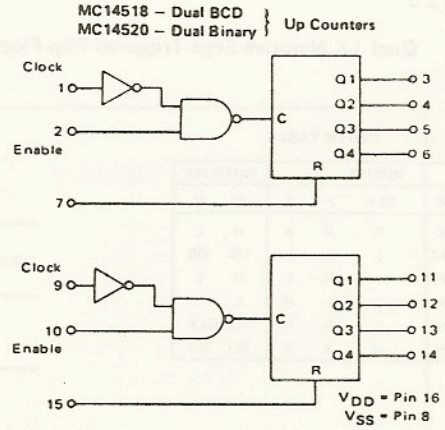


CD4022
Divide-by-8 Counter/Divider with 8 Decimal Outputs

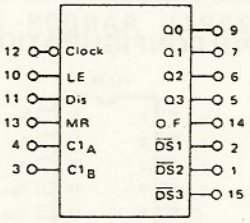


14-Lead D,E,and K Packages

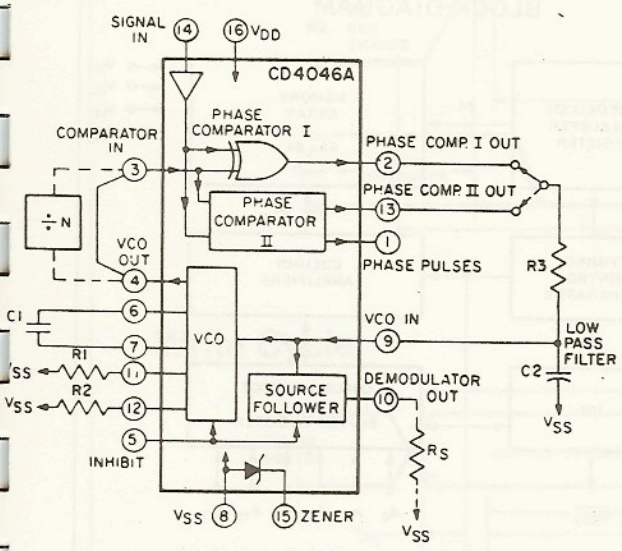
CD4024
7-Stage



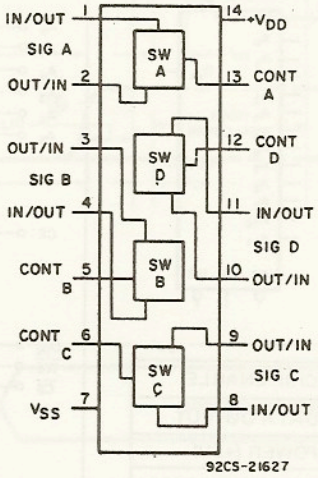
MC14553
Three-Digit BCD Counter



V_{DD} = Pin 16
V_{SS} = Pin 8

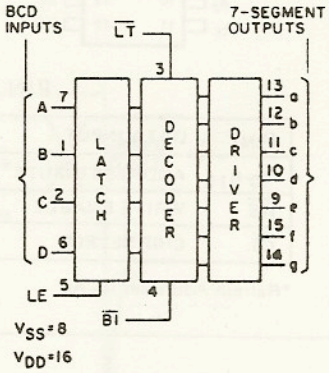


CD4046
Phase-Locked Loop



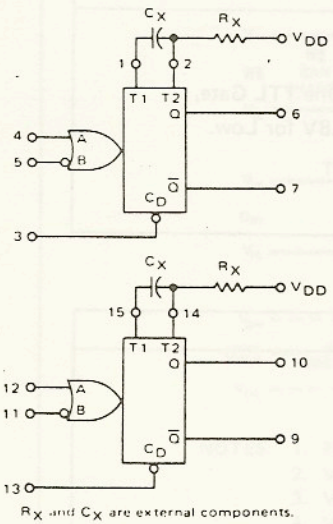
CD4016 **CD4066**

Quad Bilateral Switch



CD4511
BCD-to-7-Segment Latch Decoder Driver

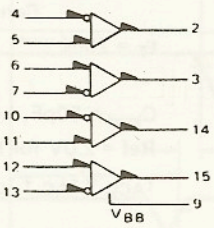
MC14528
Dual Retriggerable/Resettable Monostable Multivibrator

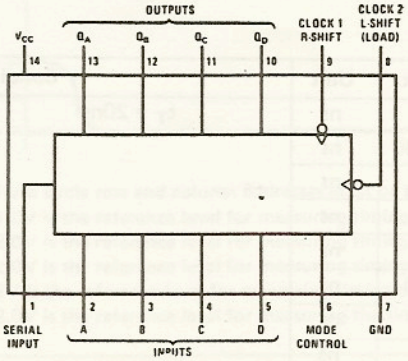


R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

MC10115
MC10515
Quad Line Receiver



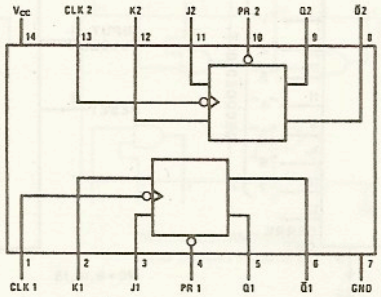


5495(J), (W); 7495(J), (N), (W);
54LS95B/74LS95B(J), (N), (W)

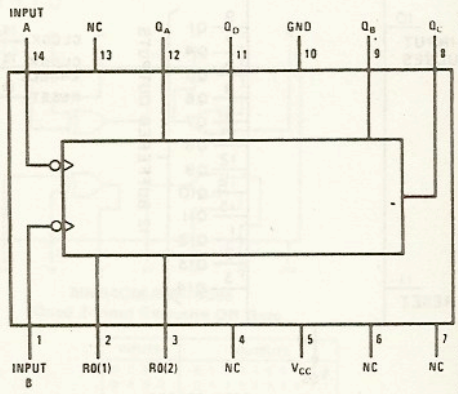
Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q0}$



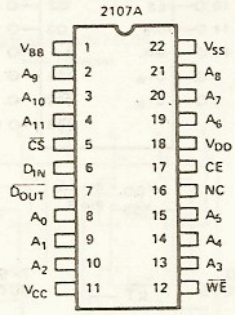
54LS113/74LS113(J), (N), (W); 74S113(N)



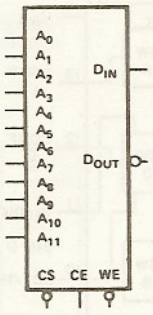
5493A/7493A(J), (N), (W);
54LS93/74LS93(J), (N), (W)

22PIN RANDOM ACCESS MEMORY

PIN CONFIGURATION



LOGIC SYMBOL



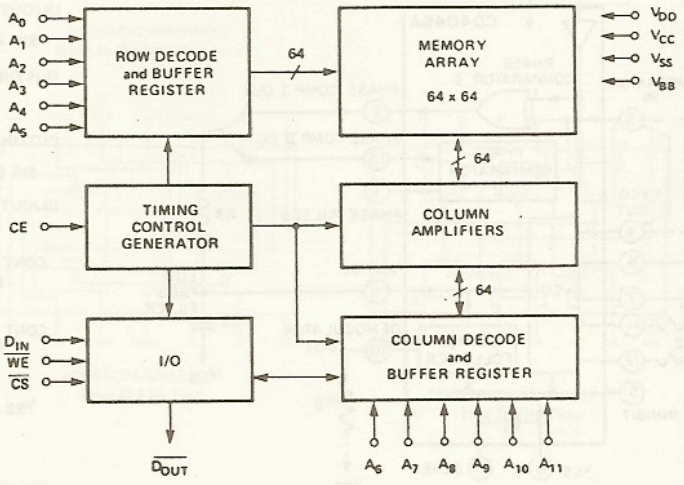
PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

TYPICAL OF MANY MANUFACTURERS

BLOCK DIAGRAM



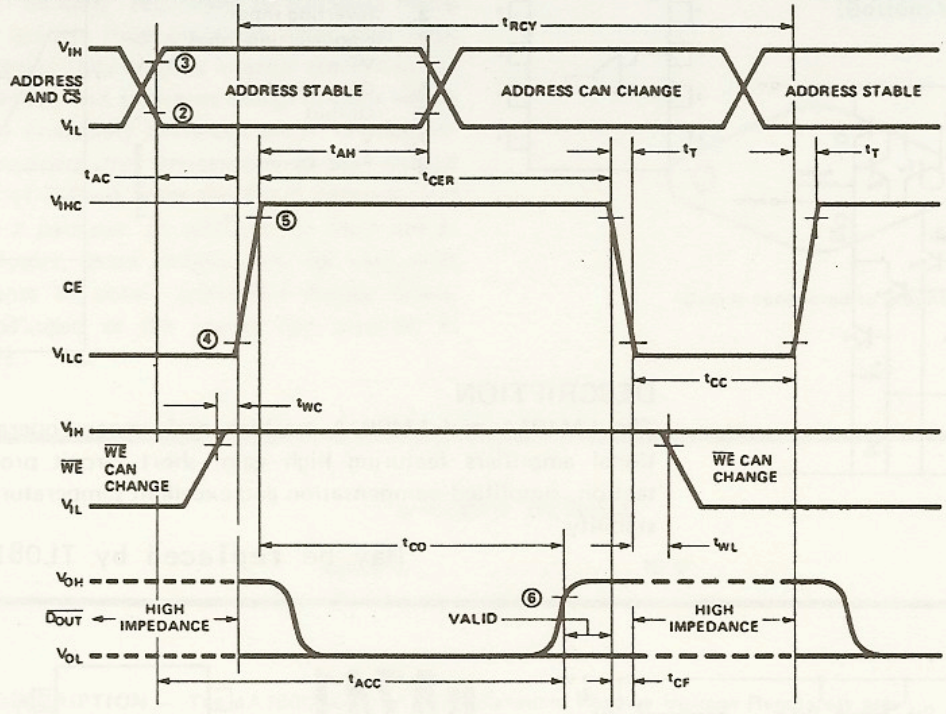
READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	690		ns	t_T = 20ns
t_{CER}	CE On Time During Read	400	3000	ns	
t_{CO}	CE Output Delay		400	ns	C_{load} = 50pF, Load = One TTL Gate,
t_{ACC}	Address to Output Access		420	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

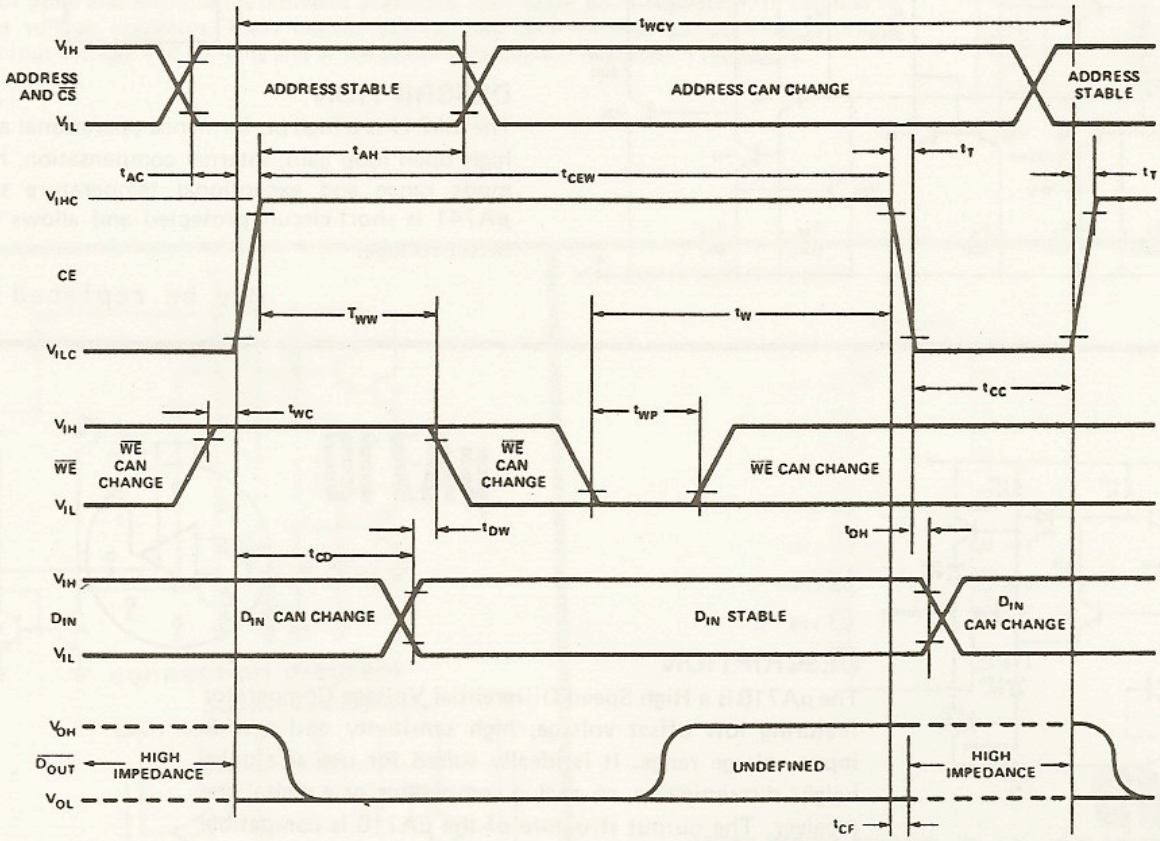
WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	970		ns	t_T = 20ns
t_{CEW}	CE Width During Write	680	3000	ns	
t_W	$\overline{WE}$ to CE Off	450		ns	
t_{WP}	$\overline{WE}$ Pulse Width	200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD} [1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WW}	$\overline{WE}$ Wait	200		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Read and Refresh Cycle [1]



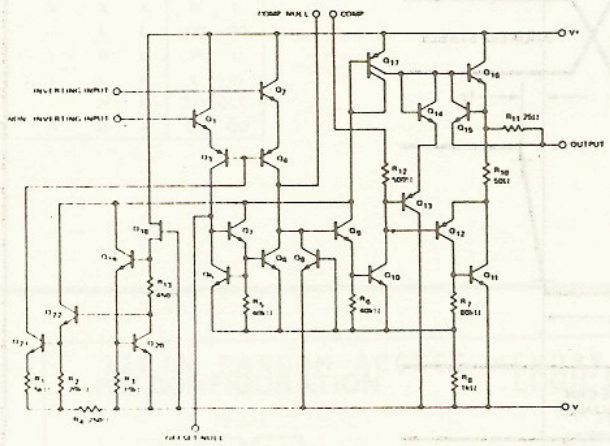
Write Cycle

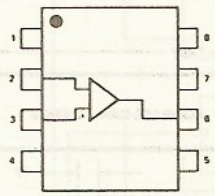


NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

LM301A

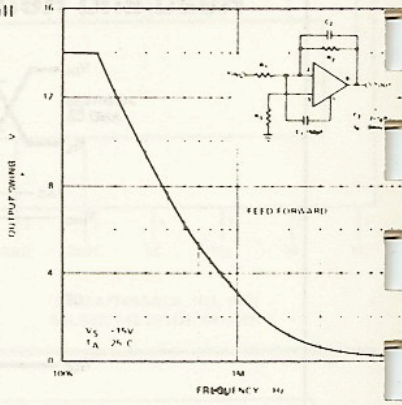
EQUIVALENT CIRCUIT





1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

LARGE SIGNAL FREQUENCY RESPONSE

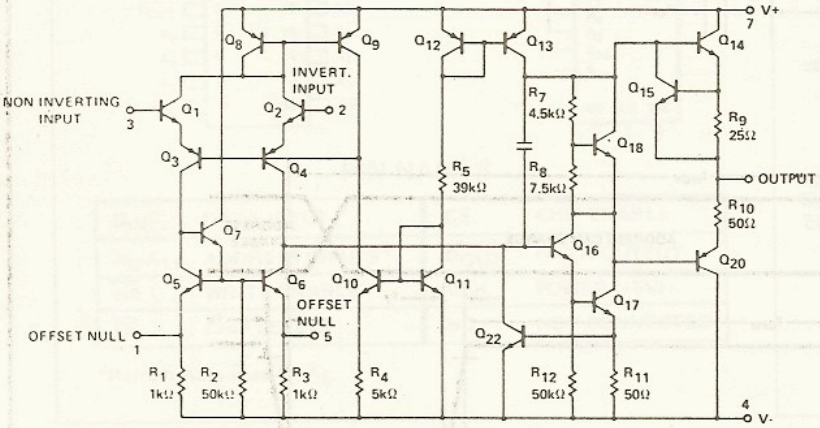


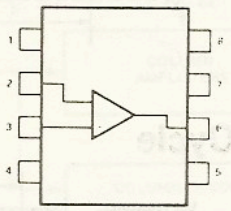
DESCRIPTION

The LM101A and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

May be replaced by TL081

µA741





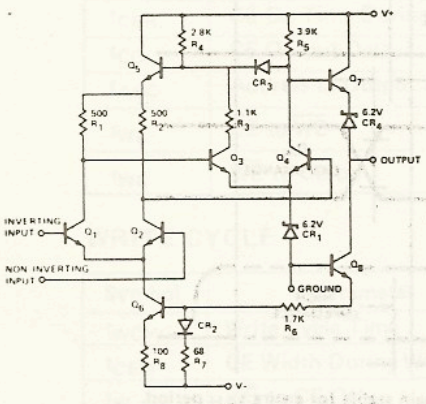
1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

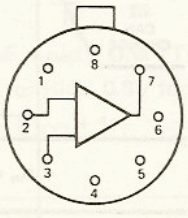
DESCRIPTION

The µA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The µA741 is short-circuit protected and allows for nulling of offset voltage.

May be replaced by TL081

µA710





1. Ground
2. Non-Inverting Input
3. Inverting Input
4. V^-
5. NC
6. NC
7. Output
8. V^+

DESCRIPTION

The µA710 is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the µA710 is compatible with DTL, TTL and Utilogic integrated circuits.

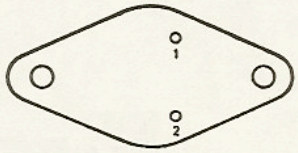
Voltage Regulators

LM309

DESCRIPTION

The LM109 and LM309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

K PACKAGE
(Bottom View)



1. Input
2. Output

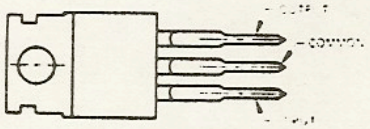
Case is connected to ground.

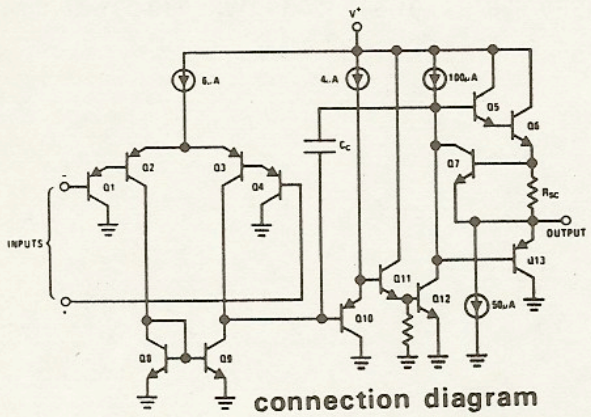
μA7800 SERIES

μA7815 . . . . . 15 V

GENERAL DESCRIPTION — The μA7800 series of Three-Terminal Positive Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

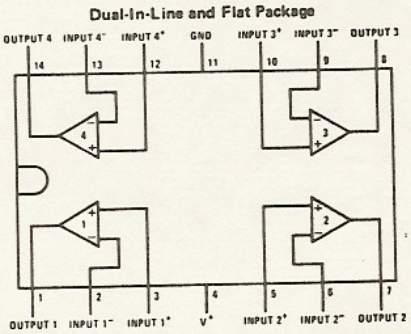
CONNECTION DIAGRAMS
TO-220 PLASTIC POWER PACKAGE
(TOP VIEW)





connection diagram

Dual-In-Line and Flat Package



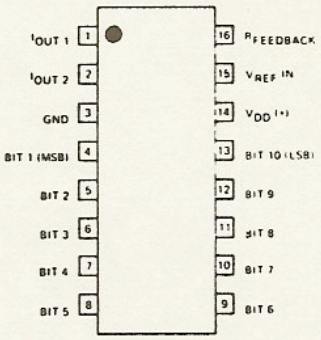
LM324D

LM324D-ABOVE
3403-SAME PINOUT
QUAD 741 EQUIVALENT

May be replaced by TL084

PIN CONFIGURATION

TOP VIEW



CMOS
MULTIPLYING D/A CONVERTER
AD7530