Eventide's harmonizer model H949

TECHNICAL SECTION

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ALIGNMENT INSTRUCTIONS

The trimpots referred to in the following instructions may be located on the 949's circuit boards by consulting the topological drawing in the section on each board.

AUDIO ALIGNMENT

NOTE: For the following adjustments both FEEDBACK level controls should be OFF, DELAY should be set to zero for each output, and ALGORITHM 2 should be selected unless otherwise indicated.

COMPRESSOR DISTORTION AND LEVEL ADJUSTMENT

1) Apply a +6dBm 1kHz low-distortion sine wave to the 949.
2) Turn the INPUT LEVEL knob until the sine wave appears clipped at the COMPRESSOR input.
3) Reduce the input signal level by 3dB.
4) Adjust the COMPRESSOR GAIN trimpot (G) so that the red LIMIT LED just begins to light.
5) Attach the distortion meter to the COMPRESSOR output.
6) Adjust the HIGH FREQUENCY DISTORTION trimpot (H) for minimum distortion.
7) Reduce the input sine-wave frequency to 100Hz.
8) Adjust the LOW FREQUENCY DISTORTION trimpot (L) for minimum distortion.
9) Repeat steps 4-8 as necessary.

OFFSET ADJUST

1) Apply a 1kHz, +6dBm sine-wave to the 949.
2) Adjust the INPUT LEVEL pot so that the LIMIT LED begins to light.
3) Reduce the input signal level by 45dB.
4) Adjust the OFFSET trimpot so that the yellow PRESENT LED just turns off or is flickering.

NOTE: If a significant adjustment of the OFFSET trimpot (greater than 10 degree rotation) is necessary, the COMPRESSOR DISTORTION AND LEVEL ADJUSTMENT should be repeated.

MAIN OUTPUT DISTORTION AND LEVEL ADJUSTMENT

1) Select MAIN OUTPUT RANDOM FUNCTION, KEYBOARD CONTROL MODE (PITCH RATIO should read 1.000).
2) With a 1kHz signal applied to the input, set the INPUT LEVEL pot so that the top GREEN level LED just begins to turn on.
3) Adjust the MAIN OUTPUT EXPANDER GAIN trimpot (G) for a peak-to-peak swing of 20 volts.
4) Reduce the input signal by 3dB and adjust the HIGH FREQUENCY trimpot (H) for minimum distortion.
5) Reduce the input frequency to 100Hz.
6) Adjust the LOW FREQUENCY trimpot (L) for minimum distortion.
7) Increase the input signal by 3dB and re-adjust the GAIN trimpot for a 20 volt output swing.
8) Select DELAY FUNCTION
9) Adjust the DELAY LEVL trimpot on the top board, HD921, for a 20 volt output swing.

DELAY OUTPUT DISTORTION AND LEVEL ADJUSTMENT

Follow steps 1-7 described above for MAIN OUTPUT.

FEEDBACK LEVEL

1) Select MAIN OUTPUT DELAY FUNCTION.
2) Apply a 1kHz input signal with sufficient level to light the LIMIT LED.
3) Set MAIN DELAY equal to 200 msec.
4) Set both FEEDBACK EQ pots to FULL CUT.
5) Turn MAIN FEEDBACK LEVEL pot full clockwise.
6) Turn INPUT LEVEL pot off (counter clockwise) and observe output signal.
7) Adjust FEEDBACK LEVL trimpot so that output decays gradually.

TIMING AND CONTROL ALIGNMENT

The following alignment instructions should be followed carefully and in the indicated sequence to assure proper performance.

MASTER OSCILLATOR TUNING

1) Connect frequency counter (or 'scope) to PIN 7 of IC47.
2) Swing board up and adjust COIL (variable inductor) using a plastic hex alignment tool for a frequency of 40.96kHz
CAUTION-Take care not to crack the brittle tuning slug.

MANUAL CONTROL

1) Select NORMAL pitch change mode and MANUAL CONTROL MODE.
2) Rotate MANUAL pot fully counter-clockwise and adjust trimpot MINF, located on front panel board HP941 for a PITCH RATIO of approximately .240.
3) Rotate MANUAL pot fully clockwise and adjust trimpot MAXF, located on lower board HA931, for a PITCH RATIO of approximately 2.10.
4) Repeat steps 2 & 3 as necessary.

EXTERNAL CONTROL VOLTAGE

1) Select NORMAL pitch change mode and MANUAL CONTROL MODE.
2) Adjust MANUAL pot for PITCH RATIO of 1.00.
3) Select CV+MAN CONTROL MODE.
3) Apply minimum desired control voltage to the rear panel terminal strip input CV IN.
4) Adjust trimpot ECV OFFSET for a PITCH RATIO of .500
5) Apply maximum desired control voltage to CV IN.
6) Adjust trimpot ECV LEV for a PITCH RATIO of 2.00
7) Repeat steps 3, 4, 5 & 6.

The 949 is factory adjusted for a +12 volt to ground ECV range so that the pitch can be controlled by an external potentiometer connected to the BIAS OUT rear panel terminal.

SINGLE SIDE BAND GENERATOR

NOTE: This adjustment should not be performed without using a SPECTRUM ANALYZER capable of resolving an 82kHz signal with 300Hz sidebands. Fortunately this adjustment is not very critical; re-adjustment should be necesary only if one of the modulator IC's (IC's 38 & 39) is replaced.

1) Set SPECTRUM ANALYZER for a center frequency of 82kHz and resolution of 300Hz.
2) Attach SPECTRUM ANALYZER to PIN 1 of IC41.
3) Select uPC# function and MANUAL CONTROL MODE with the MANUAL pot set at twelve o'clock.

4) Null 82kHz signal by alternately adjusting trimpots SSB1 and SSB2.
5) Select uPCb.
6) Repeat step 4.

TAPE CAPSTAN DRIVE

1) Disconnect keyboard (if necessary).
2) Select KEYBOARD CONTROL MODE.
3) Connect frequency counter (or 'scope) to the 19.2kHz CAPSTAN DRIVE terminal strip output.
4) Adjust trimpot CAP CAL for 19.2kHz

SERVICE SECTION

INTRODUCTION TO SERVICE SECTION

The circuitry of the H949 is contained on three printed circuit boards, with the exception of the unit's power transformers, a bridge rectifier, and three of the voltage regulators. These conponents are mounted on the right side and rear panels of the chassis. The part numbers of the three circuit boards are:

1) HA 931 Rev _ -Mounted horizontally on the bottom of the chassis. HA 931 contains power supply, audio processing, pitch change timing and function control circuitry. It is attached to the chassis at the rear panel terminal strip and to the bottom cover by 8 size 4-40 screws.

2) HD 921 Rev _ -Supported by five stand-offs above HA931 and attached to the rear panel by two hinged stand-offs. When the five size 6-32 screws are removed HD 921 can be swung up on its hinges allowing "power-on" access to the lower and front panel boards.

3) HP 941 Rev _ -Mounted vertically behind and attached to the front panel by six stand-offs, it supports all front panel switches with the exception of the line and power switches. It also supports the PITCH RATIO READOUT and all indicator LED's. Mounted on HP941 is the following: AUDIO FEEDBACK, READOUT timing and DELAY SET circuitry.

POWER SUPPLY

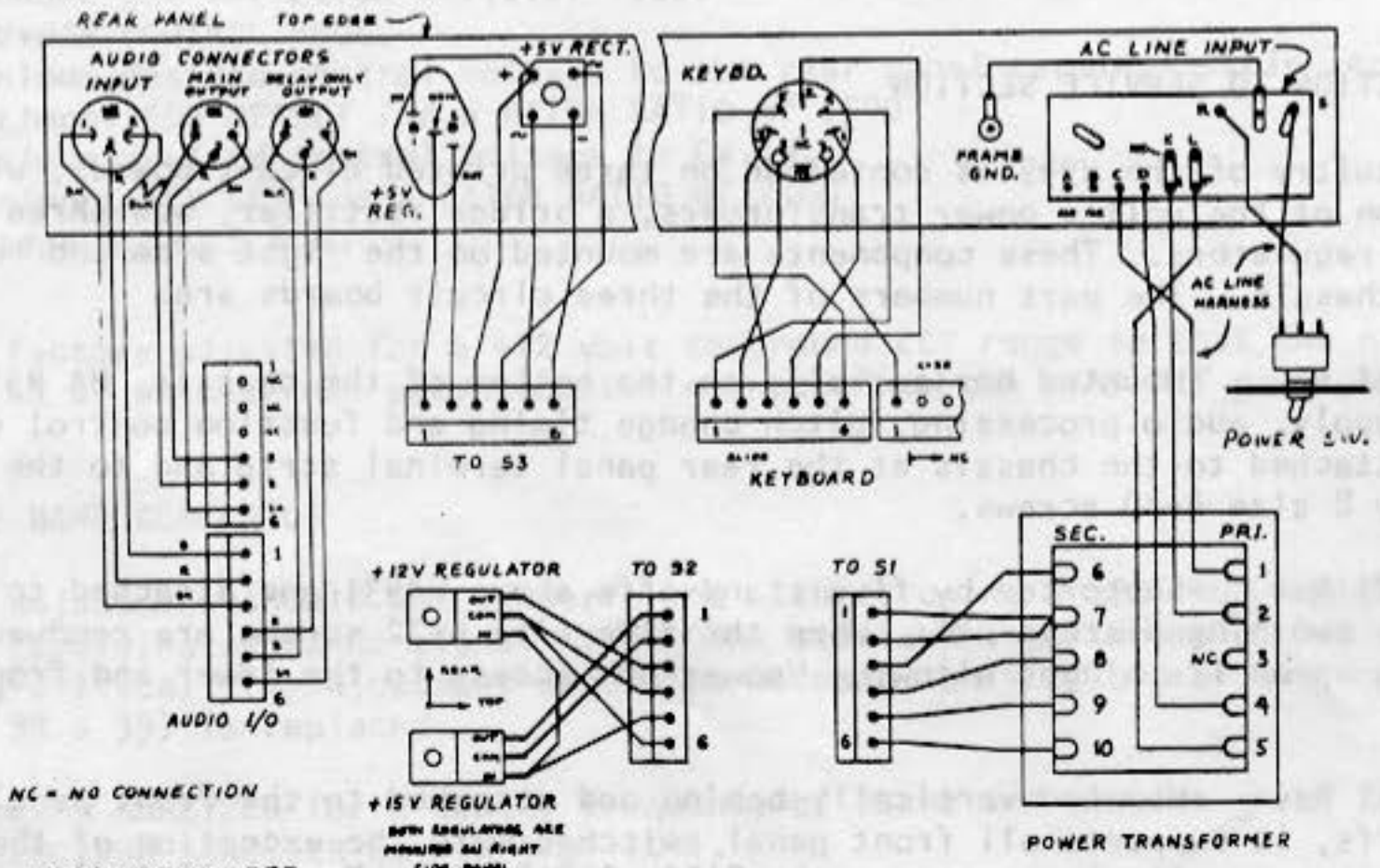
The 949's power supply provides regulated +15, -15, +12 and +5 DC volts to the circuitry contained on the three p.c. boards. The power supply circuitry is mounted on lower p.c. board HA 931 and the right and rear chassis sides.

The AC input receptacle is mounted on the rear panel and accepts a standard IEC line cord. The receptacle also contains the unit's 1/2 amp "slow-blow" fuse (3/8 amp for 230 volt operation) and a small plug-in circuit card which determines the operating line voltage. This permits conversion to and from 230 volts without removing the unit's covers.

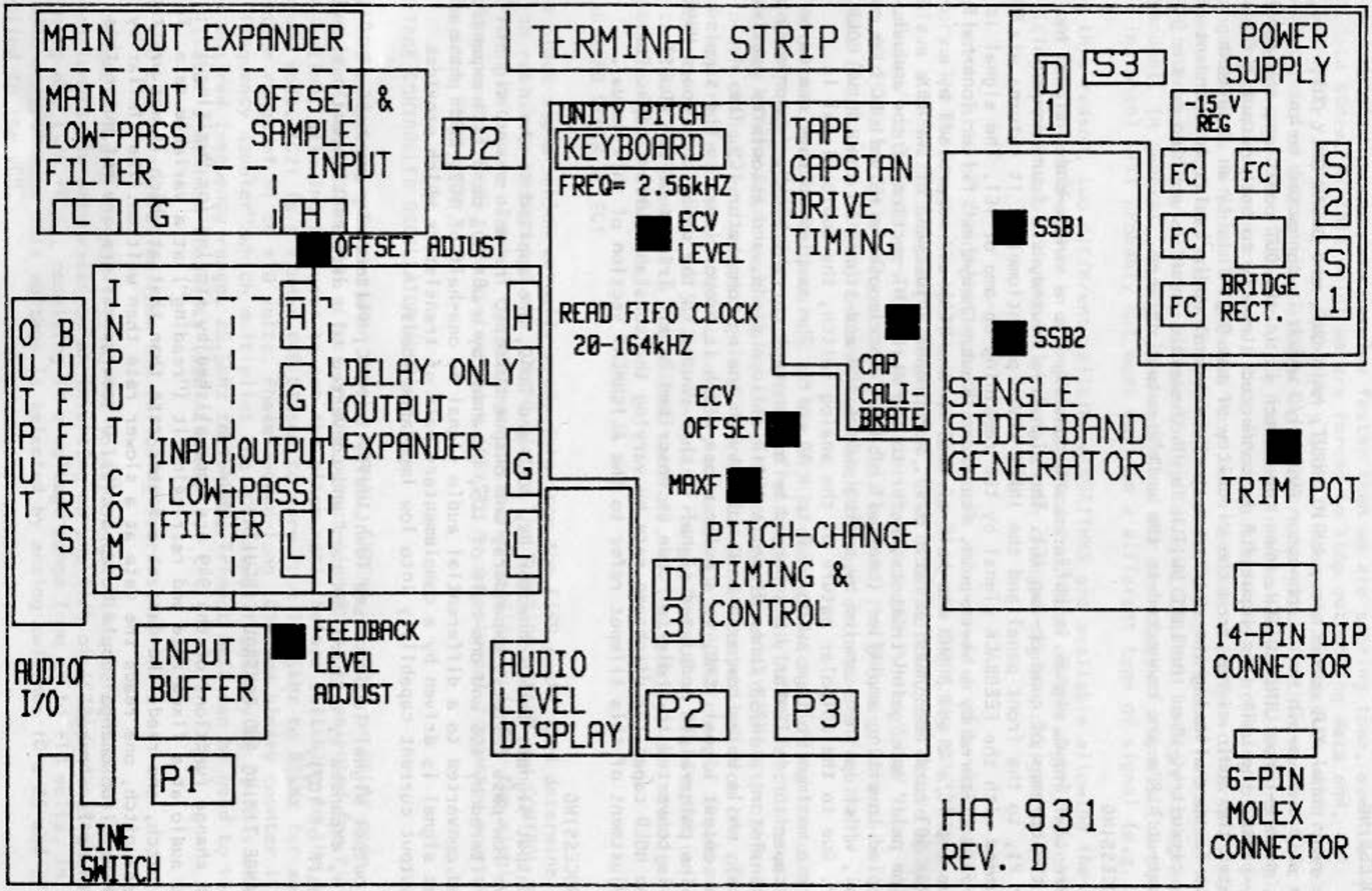
Line voltage is connected to the POWER TRANSFORMER's primary windings (mounted on the right side of the chassis) via the front panel POWER switch. The power transformer has two secondary windings; one low voltage-high current for the +5 volt supply and the other high voltage-low current for +15, +12, and -15 volts. The secondary windings are connected to HA 931 via 6 conductor Molex connector S1.

The +5 volt winding is routed directly to Molex connector S3 which is connected to a 5-amp bridge rectifier and 3-amp LM323 voltage regulator which are mounted on the rear panel heat sink. The rectifier output (approx. +8.5 volts unregulated) and the regulator output (regulated +5 volts) return to HA 931 via S3. The rectifier output is connected to the electrolytic filter capacitor mounted on HA 931.

The other transformer secondary is connected to a bridge rectifier mounted on HA 931. Both a positive and negative rectified voltage are output from the bridge and filtered by a pair of electrolytic capacitors. The negative voltage is input to a 1/2-amp, -15 volt regulator, LM7915, mounted on HA 931. The positive rectified voltage is routed, via Molex connector S2, to two 1/2-amp positive voltage regulators, LM78M12 (+12 volts) and LM7815 (+15 volts), mounted on the right side of the chassis. The regulator outputs return via S2.



H949 HARMONIZER
REAR AND RIGHT SIDE PANEL
WIRING HARNESSES


MAIN OUT EXPANDER
MAIN OUT LOW-PASS FILTER
OFFSET & SAMPLE INPUT
L
G
H
D2
OFFSET ADJUST
TERMINAL STRIP
UNITY PITCH KEYBOARD
FREQ= 2.56kHZ
ECV LEVEL
READ FIFO CLOCK 20-164kHZ
TAPE CAPSTAN DRIVE TIMING
CAP CALI-BRATE
ECV OFFSET
MAXF
PITCH-CHANGE TIMING & CONTROL
D3
P2
P3
D1
S3
POWER SUPPLY
-15 V REG
FC
FC
FC
FC
BRIDGE RECT.
S2
S1
SSB1
SSB2
SINGLE SIDE-BAND GENERATOR
TRIM POT
14-PIN DIP CONNECTOR
6-PIN MOLEX CONNECTOR
INPUT COMP
INPUT LOW-PASS FILTER
INPUT OUTPUT
DELAY ONLY OUTPUT EXPANDER
OUTPUT BUFFERS
AUDIO I/O
INPUT BUFFER
FEEDBACK LEVEL ADJUST
AUDIO LEVEL DISPLAY
P1
LINE SWITCH
HA 931
REV. D

AUDIO PROCESSING

The three rear panel XLR connectors, AUDIO INPUT, MAIN OUT, and DELAY ONLY OUT, terminate at a twelve-pin Molex connector AUDIO I/O which is connected to the six-pole, double-throw LINE SWITCH. When the switch is in the OUT position, the audio signal by-passes the unit (the input XLR is connected directly to both output XLR's) and isolates the audio signal from the circuitry of the 949. This is an important diagnostic feature allowing the user to test the external audio cables independent of the 949's circuitry. When the LINE SWITCH is IN the audio input is applied to the 949 and the output XLR's are connected to the unit's output drivers.

INPUT PROCESSING

The differential input signal is buffered and converted to a single-ended signal by three of the op-amps of quad op-amp IC1. The signal is routed, via fourteen-pin connector P1, to the front panel and the INPUT LEVEL potentiometer. It returns via P1, and is summed with the FEEDBACK signal by the remaining op-amp of IC1. The signal is then low-pass filtered by a seven-pole, four-zero "Cauer-Chebychev" filter (one-half of quad op-amp IC's 2 and 3 and one-half of dual op-amp IC4) and compressed by a plug-in DBX 303 card (compression ratio 2/1). For proper adjustment of the DBX "distortion null" and "gain" trimpots, refer to the ALIGNMENT section of the manual. An AC-coupled inverting amplifier (one-half of IC6) superimposes a +5 volt DC bias on the signal, which is then sampled by analog switch IC8 and stored on the .001uF HOLD capacitor. Due to the unipolar nature of the analog switch, the audio signal is limited to a maximum voltage swing of 0 to + 10 volts. The sampled voltage stored on the HOLD capacitor is linearly discharged by a "constant current sink", (comprising a 2N3391 transistor, a 1N753 Zener diode, a 1N914 silicon diode, and associated passive components), while being compared to 0 volts by an analog comparator IC9. The comparator output signal, CMP, is a pulse whose width is proportional to the sampled voltage. The pulse-width modulated signal is then routed to the upper p.c. board HD921 where it is converted to a digital code as described later. Trimpot OFFSET ADJUST varies the HOLD capacitor discharge rate by varying the constant current sink. For proper adjustment of this trimpot refer to the ALIGNMENT section of this manual.

OUTPUT PROCESSING

The two output signals from connector D2, MDAC and DDAC, are applied to their respective low-pass filters, expanders, and output buffers. The main output signal MDAC is filtered by IC6 and one-half of IC5, expanded by a DBX 303 card (2/1 expansion ratio) and converted to a differential audio signal by one-half of IC7. Each phase of the output signal is driven by a complementary pair of transistors which provides greater output current capability into low impedance loads.

The DDAC output signal is processed identically to MDAC; filtered by one-half of IC's 2, 3 and 4, expanded by a third DBX card and converted to a differential audio signal (second-half of IC7).

PITCH CHANGE TIMING AND CONTROL CIRCUITRY

The pitch change functions of the 949 are accomplished by storing (or "writing") digitized audio at a fixed rate and retrieving it ("reading") at a variable rate. To increase pitch, one reads the data at a faster rate than that at which it was written; to decrease pitch, one reads the data at a slower rate than written.(The similarity to tape machine pitch change should be apparent). Of course matters are not quite this simple; there is a rub.

THE RUB: Let's suppose we are increasing the pitch of an audio signal as described above. We must remove data samples faster than we are storing them, eventually emptying our data store. At this point we are forced to stop outputting data and, not surprisingly, this does not sound very good. A moment's reflection will reveal that a similar problem arises when attempting to decrease pitch in this manner. This underlying physical dilemma must be resolved in some way by all "real-time" pitch changing devices; in most cases, this involves some form of splicing of the pitch changed signal. A number of schemes have been devised to perform this splicing; from "crummy and cheap" to "sophisticated and expensive". Our research has shown that the effectiveness of any splicing scheme (or splicing ALGORITHM) is highly program dependent. In general, an algorithm optimized for one class of signals (baroque music, for instance) will probably not work well on a different type of signal (e.g. speech).

For this reason, two different splicing ALGORITHMS are available allowing the user to select the more effective in any given application. Both of the algorithms are based on splicing between two independently read, pitch changed signals designated OUTA and OUTB.

The pitch ratio of the 949 is determined by the rate at which data are read from the memory. The "write-data" rate is fixed and equal to the SAMPLING RATE, 41kHz. To achieve a three octave pitch change range, (two octaves down, one octave up), the "read-data" rate must vary from one-quarter to twice the "write-data" rate, that is, from 10.25kHz to 82kHz. The actual read-data rate of the 949 must be double these values (20.5kHz to 164kHz) because two pitch changed outputs are required.

A large portion of the circuitry of the 949 is dedicated to providing the user with a wide range of controllable pitch change effects. All MAIN OUTPUT functions with the exception of the DELAY mode employ the pitch change capabilities of the 949. The degree of pitch change, equivalent to the PITCH RATIO, can be controlled from one of four sources; the front panel MANUAL control, an external KEYBOARD control (keyboard frequency range 1.28kHz to 5.12kHz for pitch ratios from .5 to 2), CV+MAN (an external control voltage summed with the MANUAL control), or (optionally) an intelligent remote controller (IEEE-488 bus).

READ FIFO CLOCK SELECT

The clock signal which actually reads data from the FIFO ARRAY (and determines the pitch ratio) is designated the RDFIFO clock. The FUNCTION SELECT and CONTROL MODE SWITCHES determine whether the voltage-controlled oscillator (VCO), the single side band generator (SSB), the system clock (FSYS), or an external frequency source (KYBD) reads the FIFO ARRAY.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The VCO output is selected when in the NORMAL, EXTEND, REVERSE or DELAY mode. In the DELAY mode, the VCO has no effect on the output signal but is selected for PITCH RATIO indication, allowing the user to set the pitch ratio before switching to the pitch change mode. IC21 is a linear VCO biased to vary from 10.25kHz to 82kHz for an input voltage range of +1 to +10 volts. Phase-locked-loop IC14 and binary counter IC17 form a "frequency doubler" which multiplies the VCO output frequency by 2. This results in the desired frequency range, 20.5kHz to 164kHz. Trimpot MAXF can be used to vary the oscillator's maximum frequency (see ALIGNMENT).

The VCO can be controlled from the following sources:

1: MANUAL - The DC output (-15 to +12 volts) of the linear, front panel 10k ohm potentiometer is attenuated by an inverting op-amp (1/4 of IC22) and offset by a summing amp (1/4 IC22), resulting in a voltage range from +1 to +10 volts. In the MANUAL control mode this voltage is selected by analog switches IC's 25 and 37 and applied to the VCO.

2: CV+MAN - This mode allows an external control voltage, connected at the rear panel terminal strip, to be added to the MANUAL control. Inverting op-amp, IC22, and a pair of 50k trimpots allow a wide range of control voltages to be accommodated. Trimpot ECV LEVEL varies the gain of the op amp allowing a small control voltage range to vary the pitch ratio over a wide range or alternately, a large control voltage range can be made to control pitch over a limited range. Trimpot ECV OFFSET allows the center of the external control voltage range to be varied. The trimpots are factory adjusted so that an external control voltage of from 0 to +12 volts results in a two octave variation of pitch ratio centered about the MANUAL control setting. (See ALIGNMENT for details.)

3: KEYBOARD - The preferred means of externally controlling the pitch ratio is by an external oscillator with a frequency range of 1.28kHz to 5.12kHz. This results in a two octave pitch change range, -1/+1. In this control mode, the VCO is phase-locked to the external oscillator frequency resulting in precise pitch control with excellent long-term stability (providing, of course, that the external control frequency is stable). The KEYBOARD mode allows the pitch to be changed by precise musical intervals (25 notes over a two octave range), and is particularly useful for generating harmonies. Any keyboard instrument can be used to control the 949 if it meets the following requirements:
a) The instrument must have a continuous output when a key is depressed
b) The output frequency must vary from 1.28kHz to 5.12kHz.
c) The waveform must have at least a 3 volt peak-to-peak swing
d) The signal must be a "simple" waveform, e.g. sine, triangle or square wave.
Ideally, the external frequency is generated by an EVENTIDE HK940 KEYBOARD. This keyboard controller assures ABSOLUTE stability by synchronizing to the 949's system clock. It also features a GLIDE (portamento) control, a LOCK-mode, which maintains the pitch-ratio of the last key pressed, and the ability to control up to three 949's independently and simultaneously.

When the KEYBOARD mode is selected, the VCO becomes part of a phase-locked-loop which locks to the external KYBD INPUT frequency. This external signal is AC coupled to comparator IC9 whose square-wave output is one input to phase comparator IC15. The other input to the phase comparator is the VCO output frequency divided by 8 from IC16. The phase comparator output is low-pass filtered by the loop filter, comprised of one half of IC13. This results in the VCO running at precisely eight times the keyboard input frequency. When used with an EVENTIDE HK940 keyboard the time constant of the "frequency doubler" described above may be varied by the GLIDE potentiometer.

IC's 30 and 31 implement an important feature of the keyboard mode by detecting the absence of a keyboard input signal, such as when the keyboard is an organ or synthesizer and no keys are depressed. In this case, the pitch ratio is instantly set to unity (no delay change) by causing analog switch IC19 to select the system clock FSYS.

Apart from its function in keyboard operation, this feature is important in its own right. It allows the user to instantly "freeze" delay change in any of the pitch change modes by switching to the KYBD control mode with no keyboard input present. This is particularly useful in the FLANGE mode since it can be used to freeze the FLANGE at any stage.

REMOTE CONTROL VOLTAGE - Analog switch IC25 allows the pitch ratio to be OPTIONALLY varied by an intelligent controller interfaced to the standard IEEE-488 bus.

SINGLE SIDE BAND GENERATOR - SSB

The SSB is selected in the uPC, FLANGE and RANDOM modes where stable, precise control of small pitch variations is desired. The circuitry of the SSB can be divided into three sub-sections: a pair of amplitude modulators, the carrier frequency generator, and the quadrature oscillator.

An amplitude modulator is a device which multiplies two analog signals. As per convention the higher frequency signal is called the CARRIER and the lower frequency signal the MODULATION. Theoretically if the carrier and modulation inputs are sine waves, the output will be the sum of two sine waves, one whose frequency is equal to the sum of the two input frequencies (CAR+MOD) and the other's equal to the difference of the input frequencies (CAR-MOD). These two signals are called the UPPER and LOWER SIDEBANDS.

If two such modulators are connected so that the carrier inputs are of the same frequency but 90 degrees out of phase (in quadrature) and the modulation inputs are also in quadrature, then adding the two modulator outputs will yield only one sideband; either UPPER SIDE BAND (CAR+MOD) or LOWER SIDE BAND (CAR-MOD).

In the 949 the CARRIER input is FSYS (=82kHz) and the modulation is the output of a voltage controlled quadrature oscillator which can be varied from approx. 50Hz to 2000Hz.

MODULATORS: IC's 38 and 39 are monolithic modulators which will accept an AC-coupled carrier input and an AC-coupled modulation input and generate a suppressed-carrier, sum and difference frequency, output signal. Trimpots SSB1 and SSB2 can be adjusted to null the carrier component at the SSB output. (This adjustment should not be attempted without a spectrum analyzer; for details see ALIGNMENT). Each modulator has differential open-collector outputs which are cross-coupled and connected to the input of a difference amplifier (1/4 of IC41). This amplifier's output is band-pass filtered (1/4 of IC41) to remove spurious harmonics which are the result of the modulation process. The SSB signal is converted to a square wave by comparator IC18.

CARRIER FREQUENCY GENERATION: The carrier frequency of the SSB generator is derived from PC2, the 1.64MHz output of the uPROGRAM COUNTER located on the upper p.c.board, which is routed thru connector D3 (pin6). This TTL level signal is biased to drive IC44, a decoded output decade counter. Two of the ten 164kHz outputs, which are 180 degrees out of phase, drive dual data flip-flop IC42, each half of which is connected as a "toggle" flip-flop. The outputs of these flip-flops are a pair of 82kHz square waves which are 90 degrees out of phase. The output of one flip-flop, CARRIER 2, is applied to modulator IC39, while one of the two complementary outputs of the other flip-flop, CARRIER 1, is selected by a pair of analog switches, two quarters of IC43. Depending on which switch is turned on, CARRIER 1 will either LEAD or LAG CARRIER 2 by 90 degrees; which causes the SSB to generate either the UPPER or LOWER side band. Selecting the UPPER side band assures that the pitch ratio will be greater than unity while selecting the LOWER side band guarantees a pitch ratio lower than unity. One half of dual flip-flop IC46 determines which of the switches is selected. The flip-flop's state depends on a number of conditions, in particular the selected FUNCTION .

On "power-on" this circuit is synchronized by a pair of RC time constants which reset the decade counter IC44 and the dual flip-flop IC42. To insure proper sequencing the time constant of the counter is an order of magnitude greater than that of the flip-flops. It is possible, by switching the unit on and off rapidly, to throw this circuit "out of synch" rendering all SSB functions inoperative. To re-synch, turn the unit off for 10 seconds before re-applying power.

If either of the uPC (micro-pitch change) FUNCTIONS is selected, the appropriate switch of IC43 is enabled bringing one input of a pair of comparators, (1/2 of IC47), to either +12 or approx. +1 volts. This enables the appropriate comparator output which in turn sets or resets IC46 causing the SSB to generate the UPPER side band for uPC# and the LOWER for uPCb.

In the FLANGE mode, the objective is to switch alternately between UPPER and LOWER side bands thereby sweeping the delay back and forth between two "fixed" delay times. These fixed delay times are determined by a resistive, voltage-divider network which feeds an approx. +3 volt signal to one comparator and an approx. +7 volt signal to the other. With both switches of IC43 turned off the remaining input of each comparator is an analog equivalent of the CPU POINTER register from the upper p.c. board. This voltage is an accurate, linear indication of the current delay of the pitch change signal. The POINTER voltage swing in pitch change modes is normally 0 to 10 volts (0 to 25 msec respectively). In FLANGE, the comparators restrict this range to +3 to +7 volts (corresponding to a delay of approx. 7.5 to 17.5 msec), by switching to the UPPER side band (decrease delay) whenever the POINTER voltage exceeds +7 volts and the LOWER side band (increase delay) if it is less than +3 volts.

Flanging is created by adding a pitch changed (varying delay) signal and a fixed delay signal. In the FLANGE mode, the 949 automatically adds a fixed delay signal (12.5 msec) to the pitch changed signal (whose delay varies from approx. 7.5 to 17.5 msec).

In the RANDOM mode, analog switch IC45 is turned on, changing the fixed voltages at the comparator inputs to approx. +1 and approx. +9 volts, constraining the delay change to between 2.5 and 22.5 msec. Within this 20 msec range the delay is free to change according to the state of flip-flop IC46. If the flip-flop is neither being set nor reset by the comparators, then its state is dependent on PRN; the output of a digital, pseudo random noise generator. This means that, providing the delay is within the allowed range, there is a 50% probability that the delay will be increasing or decreasing, resulting in a natural, "random-walk" through the allowable delay range. If the delay exceeds either delay limit, the comparator sets (or resets) IC46 forcing the delay away from the limit.

VOLTAGE CONTROLLED QUADRATURE OSCILLATOR

Two integrating amplifiers (1/2 of IC41) connected with positive feedback, oscillate at a frequency determined by their associated RC time constants. This type of oscillator is called a "quadrature oscillator" because the outputs of the two amplifiers are sine waves which are 90 degrees out of phase. These quadrature sine waves are the modulation inputs to the modulator IC's. Three analog switches (3/4 of IC40) are employed as the voltage-controlled variable "resistors". Actually it is the average resistance of the analog switch which is varied by controlling the duty cycle of a high frequency control signal. The wider the pulse width, the lower the average resistance; with a 100% duty cycle the switch is always on and the resistance is approx. 100 ohms. At the other extreme, 0% duty cycle, the switch is always off and the resistance is approx. 1M ohm.

Comparator IC47 generates the switch control signal with a pulse width proportional to the control voltage output from op-amp IC22 (0 to +10 volt range). The control voltage is compared to a triangle waveform which is generated by low-pass filtering the square wave output of IC22. The source of this control voltage can be either the MAN, MAN + CV, or with the optional REMOTE interface card installed, a REMOTE control voltage. The KEYBOARD has no effect in any of the SSB modes

In the two uPC modes, a pair of analog switches (1/2 of IC45) are turned on and the quadrature oscillator varies from approx. 20Hz to approx. 6kHz, resulting in pitch ratios from unity to approx. .93 in uPCb and from unity to approx. 1.07 in uPC# . In FLANGE or RANDOM the switches (IC45) are turned off and the frequency is variable from approx. 20Hz to approx. 600Hz, for a pitch ratio from approx. .993 to 1.007.

PSEUDO RANDOM NOISE GENERATOR

When the RANDOM FUNCTION is selected a digital pseudo random noise generator is clocked at 820Hz (signal FSYS divided by 100, IC's 48 & 50) outputting digital noise signal PRN. PRN is the input to 1/2 of IC46, a dual data flip-flop, which controls the SSB modulator selecting pitch ratios above or below unity (decreasing or increasing delay). The noise generator is a 19 bit maximal-length shift register comprised of IC26, an 18 stage shift register, and the second half of flip-flop IC46 connected in series. Two of the outputs are fed back to the input thru XOR gate IC20.
The shift register can "latch up" if all the outputs are at zero. IC23, a seven stage binary counter, detects the "all-zero" condition and sets the flip-flop thereby re-initiating the sequence.

TAPE CAPSTAN DRIVE

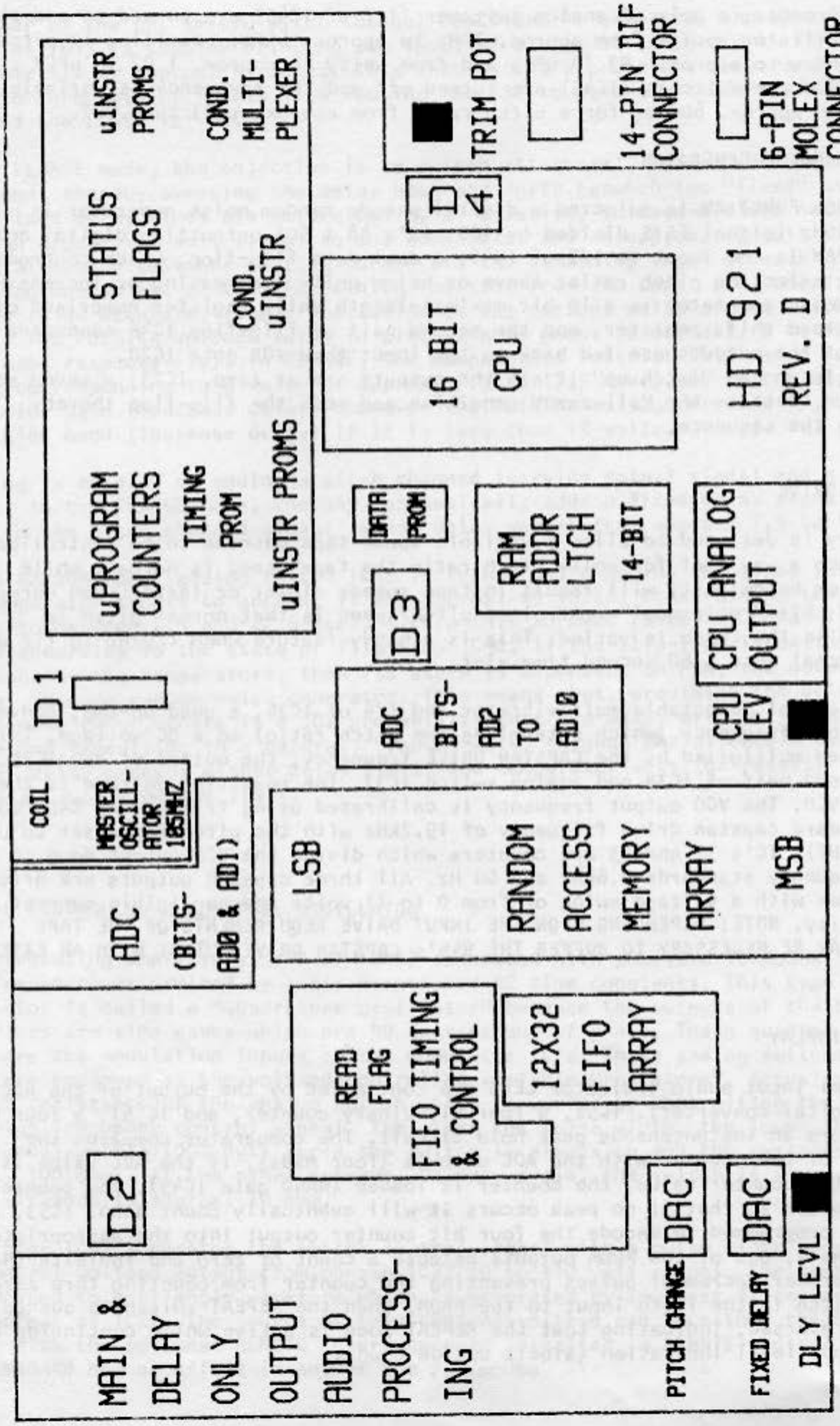
This circuitry is designed to allow a variable speed tape machine to be controlled by the 949 in such a way that for unity pitch ratio the tape speed is normal, while ratios above or below unity will result in tape speeds slower or faster than normal. The result of this "reciprocal" control of pitch/speed is that normal pitch is maintained while the tempo is varied. This is a handy feature when trying to fit a 62 second commercial into a 60 second time slot.

1/2 of IC34, a dual monostable multivibrator and 1/4 of IC36, a quad op-amp, convert the RDFIFO clock frequency (which determines the pitch ratio) to a DC voltage. This voltage is then multiplied by the CAPSTAN DRIVE frequency, the output of VCO IC35, using the second half of IC34 and analog switch IC37. The resulting voltage is the input to the VCO. The VCO output frequency is calibrated using trimpot CAP CAL, to output a standard capstan drive frequency of 19.2kHz with the pitch ratio set to unity (see ALIIGNMENT). IC's 32 and 33 are counters which divide the VCO output down to the two other frequency standards 9.6kHz and 60 Hz. All three capstan outputs are driven by CMOS devices with a voltage swing of from 0 to 12 volts and negligible current drive capability. NOTE: DEPENDING UPON THE INPUT DRIVE REQUIREMENTS OF THE TAPE MACHINE, IT MAY BE NECESSARY TO BUFFER THE 949's CAPSTAN DRIVE OUTPUT WITH AN EXTERNAL AMPLIFIER.

AUDIO LEVEL DISPLAY

The front panel input audio indicator LEDS are controlled by the output of the ADC (analog to digital converter). IC52, a four bit binary counter, and IC 51, a four bit comparator, form an instantaneous peak hold circuit. The comparator compares the current value of the counter with the ADC outputs (four MSBs). If the ADC value is greater than the counter value, the counter is loaded (NAND gate IC49). The counter is slowly decremented so that if no peak occurs it will eventually count down. IC53, an 8 X 32 PROM, is programmed to decode the four bit counter output into the appropriate LED drive signals. One of the PROM outputs detects a count of zero and inhibits (NAND gate, IC49) further decrement pulses preventing the counter from counting thru zero. The REPEAT switch is the fifth input to the PROM. When the REPEAT switch is pushed in, LED order is reversed, indicating that the REPEAT mode is active while continuing to display an input level indication (albeit upside down).

HD 921 REV. D - Upper P.C. Board



MASTER OSCILLATOR

Transistor Q1, a pair of 3pf capacitors and a variable inductor (located beneath the board) form a high frequency, tuned-circuit oscillator tuned to 105MHz. Transistor Q2 amplifies the oscillator output and provides the proper levels to drive TTL and ECL devices. Two dual flip-flops, IC's 29 and 30, connected in series, divide the 105 MHz signal by sixteen.

PROGRAM COUNTERS

The 6.56MHz output of IC30 drives synchronous 4-bit binary counter IC44 which outputs a 410kHz signal to IC45, a synchronous 4-bit decade counter. The 41kHz output of IC45 (pin 7) is the 949's sampling frequency. The least significant output of IC44 (pin 3), at a frequency equal to 205kHz, is the CPU clock signal CCPU. The seven most significant outputs of IC's 44 & 45 comprise an eighty count PROGRAM COUNTER with outputs designated PC1-PC7. The program counter outputs access the micro-instructions stored in the uINST proms.

TIMING PROM

Program counter outputs PC3 to PC7 are the address inputs to IC46, a 8X32 programmable read only memory (PROM). In normal operation only 20 of the 32 8-bit words are accessed (because PC4-PC7 are the outputs of a decade counter). The outputs are defined as follows:

IC 46

PIN#	NAME	DESCRIPTION
1	NSPTR	SAMPLE POINTER VOLTAGE not
2	SAMP	SAMPLE INPUT AUDIO SIGNAL
3	SELECT	ENABLE uINST PROM OUTPUTS
4	T5	uINST PROM ADDRESS BIT
5	T4	uINST PROM ADDRESS BIT
6	NRSTAD	RESET ADC not
7	NENAD	ENABLE ADC not
9	SDLO	SAMPLE DELAY ONLY OUTPUT

CENTRAL PROCESSING UNIT (CPU)

The 949's sixteen-bit CPU comprises four "bit slice" bipolar IC's of four bits each, part # 2901. Each chip contains a four-bit multifunction Arithmetic Logic Unit (ALU), instruction decoding and timing logic, and sixteen four-bit general purpose registers. These registers are of the "two-port" variety which allow simultaneous READ/WRITE operations with independent read/write addresses or simultaneous reads from different addresses. The 2901 also provides zero and sign status outputs.

The four 2901's, IC's 22-25, are connected to form the 16-bit CPU with IC22 being the most significant slice (MSS). The ten microinstruction inputs (I9-I0,C0) as well as the eight address lines (four A-port, four B-port address bits) are connected in parallel across all four slices. Sixteen-bit data is input to the CPU on the "D-bus" and sixteen-bit output data are output on the "Y-bus".

MICRO-INSTRUCTION (uINST) PROMS

Every sample period (approx. 25 usec) a sequence of eighty micro-instructions (uINST) is accessed by program counter outputs PC1-PC7. These uINST's are stored in eight 8X32 PROM's organized as four pairs of PROM's with the corresponding outputs of each pair connected together. This forms, in effect, a single 32X64 PROM, four PROM's wide and two PROM's deep. In this way, program storage is divided into two sections of four PROM's each. TIMING PROM bit SELECT and 1/6th of inverter IC31 enable the TRI-STATE outputs of first one group of four PROM's and then the other. IC's 47, 49, 51 and 60 store micro-instructions for the first 32 program steps and IC's 48, 50, 52 and 61 store steps 32-79. The 48 program steps 32-79 are read from the 32 bit proms by accessing 16 of the PROM addresses twice. TIMING PROM bits T4 and T5 are the two most significant address bits of the second group of PROM's. These address bits select one of four groups of eight PROM addresses. This scheme allows groups of eight micro-instructions each (sub-routines) to be repeated. The uINST PROM output designations are as follows:

IC49 & IC50

PIN#	NAME	DESCRIPTION
1	I8	CPU uINST bit
2	I0	CPU uINST bit
3	I1	CPU uINST bit
4	B0	CPU B-port addr bit
5	B1	CPU B-port addr bit
6	B3	CPU B-port addr bit
7	I4	CPU uINST bit
9	I5	CPU uINST bit

IC51 & IC52

PIN#	NAME	DESCRIPTION
1	A3	CPU A-port addr bit
2	A1	CPU A-port addr bit
3	A0	CPU A-port addr bit
4	I6	CPU uINST bit
5	CI7	COND'L uINST bit
6	CC0	COND'L CPU CARRY IN
7	CA2	COND'L A-port addr
9	I2	CPU uINST bit

IC60

1	CI3	COND'L uINST bit
2	CKRMP	Clock RAMP FLAG
3	CKDIR	Clock DIRECTION FLAG
4	CB2	COND'L B-port addr bit
5	X7C	I7 MULTIPLEXER addr bit
6	X7B	"
7	X7A	"
9	X3A	I3 MULTIPLEXER addr bit

IC61

1	CI3	COND'L uINST bit
2	-	UNUSED
3	XB2	ENABLE COND'L B2
4	CB2	COND'L B-port addr bit
5	X7C	I7 MULTIPLEXER addr bit
6	X7B	"
7	X7A	"
9	X3A	I3 MULTIPLEXER addr bit

IC47

1	-	UNUSED
2	X3B	I3 MULTIPLEXER addr bit
3	NWRT	RAM ARRAY WRITE NOT
4	XA2	ENABLE COND'L A2
5	SFXD	SAMPLE FIXED DELAY
6	MAC	RAM ARRAY ACCESS
7	CKSN	Clock SIGN FLAG
9	CKZR	Clock ZERO FLAG

IC48

1	X3B	I3 MULTIPLEXER addr bit
2	X3C	"
3	CKDAC	CPU OUT to DAC LATCH
4	SREF	SAMPLE MAIN OUT REF
5	CKFIFO	LOAD FIFO ARRAY
6	MAC	RAM ARRAY ACCESS
7	CKSN	Clock SIGN FLAG
9	CKZR	Clock ZERO FLAG

CONDITIONAL MICRO-INSTRUCTIONS

The MICRO-PROGRAM of the 949 can execute a limited type and number of conditional micro-instructions by inverting the status of up to 3 bits of the CPU uINST word (bits I3, I7 and C0) if a specified condition is true.

CONDITIONAL uINST bit I7:
With I8=0, the status of I7 determines whether or not the result of the current CPU operation is stored in the register specified by the B-port address. If I7=0 the result is not stored.

Conditional uINST bit CI7 (IC's 51 & 52) is one input to an exclusive-or (XOR) gate IC53 whose output is CPU uINST bit I7. The other input of the XOR gate is the output of an eight-in one-out multiplexer IC62. One of the 8 multiplexer inputs is selected by the three-bit address XI7 (uINST bits X7C, X7B, X7A). For unconditional instructions XI7=0 which selects input 0 of IC62. Since input 0 is connected to ground, the XOR gate passes CI7 unchanged (I7=CI7). Selecting one of the other multiplexer inputs will cause the XOR gate to invert CI7, (I7=NOT(CI7)), if the selected input is true. The multiplexer input assignments are listed below:

CONDITIONAL uINST bits I3 & C0:
These CPU uINST bits can be conditionally inverted in the same manner as described above for I7. Conditional uINST bit CI3 is one input of XOR gate IC56. The other XOR input is the output of eight-in one-out multiplexer IC63. One of the 8 multiplexer inputs is selected by three-bit address XI3 (uINST bits X3C, X3B and X3A). For unconditional instructions XI3 can be either 0 or 7 as these inputs are connected to ground. Selecting one of these inputs will cause the XOR gate to pass CI3 unchanged (I3=CI3). Selecting one of the remaining inputs will cause the XOR gate to invert CI3 (I3=NOT(CI3)) if the selected input is true.

Inverting uINST bit I3 changes an addition operation to subtraction, a pass operation to an invert, etc. To satisfy the requirements of the binary number system used by the CPU, the input carry bit C0 must be 0 for addition and 1 for subtraction. For this reason, conditional uINST bit CC0 is applied to XOR gate IC53 and conditionally inverted by the output of multiplexer IC63.

I7 MULTIPLEXER----IC 62

PIN#	INPUT	CONDITION
4	0	GROUND
3	1	ALGORITHM
2	2	NOT(RANDOM or FLANGE)
1	3	EXTEND PC
15	4	SIGN FLAG
14	5	ZERO FLAG
13	6	READ FLAG
12	7	(READ) AND (ZERO)

I3-C0 MULTIPLEXER----IC 63

PIN#	INPUT	CONDITION
4	0	GROUND
3	1	ALG1
2	2	RAMP FLAG
1	3	PC7
15	4	NOT REVERSE
14	5	DIR FLAG
13	6	SIGN FLAG
12	7	GROUND

CONDITIONAL CPU REGISTER ADDRESSES

Both A and B port CPU registers can be conditionally addressed to a limited extent. XOR gate IC53 allows uINST bit A2, (one of four A-port address bits), to be inverted if both program counter bit PC7 and uINST bit XA2 are true. XOR gate IC56 performs an identical function on uINST bit B2 (with qualifier uINST bit XB2). This conditional addressing scheme allows the same uINST to be executed more than once using different source and destination registers each time.

STATUS FLAGS

The 949's micro-program employs five status flags as conditional micro-instruction qualifiers. Two of these flags, ZERO and SIGN, store the status of CPU operations while the three remaining flags, RAMP, DIR and READ, indicate pitch change status.

ZERO FLAG - 1/2 of dual data latch IC54 is strobed by uINST bit CKZR. When strobed the flag is set to 1 if the current CPU output is equal to zero.

SIGN FLAG - 1/2 of dual data latch IC54 is strobed by uINST bit CKSN. When strobed the flag is set to 1 if the current CPU output is negative.

RAMP FLAG - 1/2 of dual data latch IC55 is strobed by uINST bit CKRMP. The RAMP FLAG initiates ALGORITM 2 splicing ramps and is a convenient oscilloscope trigger point for observing ALGORITHM 2's splicing operation.

DIR FLAG - 1/2 of dual data latch IC55 is strobed by uINST bit CKDIR. The DIR FLAG indicates the direction of delay change (pitch ratio increasing or decreasing). In all pitch change modes the DIR FLAG is set to 1 if the pitch ratio is greater than unity (delay decreasing) and 0 if less than unity (delay increasing). If the pitch ratio is precisely unity (delay not changing) the DIR FLAG's status indicates the direction of the last delay change. The DIR FLAG is an important diagnostic aid in that its proper operation indicates that a significant portion of the CPU and associated circuitry is functioning properly. NOTE: In all of the pitch change modes, delay change can be stopped by selecting the front panel KYBD CONTROL MODE and disconnecting any control frequency input such as the keyboard.

READ FLAG - 1/2 of dual data latch IC13 is strobed every sample period storing the FIFO ARRAY's status. The READ FLAG indicates that the FIFO ARRAY is half empty and requests a transfer of four data words from RAM to FIFO.

CPU DATA INPUT

The sixteen-bit CPU data input bus is referred to as the "D-bus". The DATA PROM IC43 inputs necessary 8-bit program constants to the CPU on lines D7-D14. The most significant input bit D15 is grounded and the 7 least significant bits D0-D6 are pulled-up to +5 volts by a 100k resistor network. Since IC43 is a 8X32 bit PROM it cannot output a unique constant value for each program step, instead a unique value is available for each consecutive group of four instructions. The DATA PROM's TRI-STATE outputs are disabled twice every sample period allowing MAIN and DELAY ONLY delay set data to be input to the CPU.

CPU ANALOG OUTPUT

The eight least significant bits of the CPU, Y0-Y7, are stored when uINST bit CKDAC strobes eight-bit latch IC38. IC's 36 & 37 convert the 8-bit latch output to an analog voltage designated CPU ANALOG OUT.

Three independent analog signals are generated by the CPU each sampling period; two splicing signals REFA & REFB (reference voltage inputs of the MAIN OUTPUT DAC) and a voltage corresponding to the current value of the pitch-change POINTER register. In all three cases, the voltage swing is 0 to 10 volts. In the case of the pointer voltage an output of 0 volts corresponds to 0 delay while a 10 volt output corresponds to a delay of 25msec.

11X16K DYNAMIC RAM ARRAY

Eleven 16K dynamic random access memory (RAM) IC's, M0-M10, comprise the digital audio data storage of the 949. The seven address inputs, row address strobe (NRAS), column address strobe (NCAS), write (NWRT), as well as the three power supply lines (+12, +5 and -5 volts), are connected in parallel across all eleven RAMS. NWRT goes low once per sample period to write new data into the base address location. When the REPEAT switch is depressed NWRT is disabled and no new data is written into memory.

The data inputs to the RAM are the outputs of the analog-to-digital converter (ADC) counters. The RAM ARRAY outputs data to the DELAY ONLY OUTPUT DAC and the 12X32 FIFO array.

ANALOG-TO-DIGITAL CONVERTER (ADC)

Every sample period the pulse-width modulated representation of the audio signal is converted to an eleven-bit binary word. This is accomplished as follows:
The pulse-width modulated audio signal, CMP, from HA931 via connector D2, is one input to IC26, a two input NAND gate. The second NAND gate input is TIMING PROM output NENAD which defines the conversion period. During conversion the NAND gate enables an 11 bit binary counter chain comprised of IC's 28, 32, 33 & 34. The counter chain remains enabled until either CMP goes low or the end of conversion (NENAD). In this way, the pulse width, which is proportional to the audio signal level, determines the number of positive clock transitions (105MHz input clock) input to the counter chain and hence the resultant count. At the end of the conversion period, NWRT goes low and a random access memory (RAM) write cycle is initiated, writing the 11 bit word into the 11X16K RAM array. When the data has been stored, the ADC counters are reset by TIMING PROM output NRSTAD in preparation for the next conversion cycle. In the event that the counters overflow during conversion (count greater than 2047), the carry output of IC34 sets the overflow flag IC32. The overflow flag sets the ADC to its maximum count of 2047 by setting each bit of the counter chain high. The overflow flag is cleared when the ADC is reset by NRSTAD.

DELAY ONLY OUTPUT

Eleven-bit DELAY ONLY DAC IC9 (a twelve-bit multiplying DAC) in conjunction with one-half of quad op amp IC7, converts the RAM output to an analog voltage. The DLY LVL trim pot varies the DAC's reference voltage which in turn determines the maximum output voltage swing. The reference voltage should be adjusted to approximately -10 volts resulting in a 0 to +10 volt swing at the op amp output. FOR PROPER ADJUSTMENT REFER TO ALIGNMENT INSTRUCTIONS.

The RAM ARRAY is enabled for approx. 3usec allowing the DAC output to settle and analog switch IC6 to turn on, charging the .001uF hold capacitor. uINST bit SDLO is the sample control signal which closes the switch for approx. 1.5usec. The hold capacitor voltage is buffered by op amp IC5 which is AC coupled (removing +5 volt bias) to inverting amplifier IC1. The output of IC1 runs to connector D2 and is designated DDAC.
NOTE- The analog switches employed in the 949 can only pass signals limited to a 0 to +10 volt range. For this reason, a +5 volt D.C. bias is superimposed on signals where necessary.

FIXED DELAY OUTPUT

For the MAIN OUTPUT functions of DELAY and FLANGE the main output signal must contain a stable fixed delay. In the DELAY mode, the FIXED DELAY is equal to the front panel MAIN OUTPUT DELAY SET SWITCHES. If the FLANGE mode is selected, the FIXED DELAY is equal to the switch setting plus 12.5msec. The appropriate FIXED DELAY signal is applied to the sample and hold cicuitry of analog switch IC4, a .001uF capacitor and op amp IC3. This signal is input to analog switch IC2 as well as to the phase shift network of IC1. The output of this phase shift network is applied to a 2nd switch of IC2 and the switch outputs are connected together so that either the direct or phase-shifted FIXED DELAY signal can be selected. In DELAY mode, the direct FIXED DELAY signal is selected, in FLANGE the phase-shift signal is selected; in all other modes both switches are off. The selected signal is summed at inverting amplifier IC1, whose output is desigated MDAC at connector D2.

FIRST-IN FIRST-OUT (FIFO) REGISTERS

Six 4X16 FIFO's, IC's 16-21, are organized as a 12X32 FIFO ARRAY. Eleven of the FIFO inputs come from the outputs of the dynamic RAM ARRAY with the corresponding FIFO outputs connected to the MAIN OUTPUT DAC IC8. The READ FLAG IC13 requests a RAM read operation of the CPU whenever the FIFO is less than half full (fewer than sixteen words stored). The read from RAM and write to FIFO sequence occurs as follows:

1) The CPU computes and outputs the RAM address for the next OUTA data word.
2) uINST bit MAC initiates a RAM read.
3) uINST bit CKFIFO gated with the READ FLAG clocks RAM OUTA data into the FIFO
4) Steps 1 to 3 are repeated for OUTB data
5) Steps 1 to 4 are repeated.

The result of the above sequence is that if the READ FLAG is true for a given sample period, four data words (two for OUTA and two for OUTB) are read from RAM to FIFO.

RDFIFO from connector D2 is input to a dual monostable multivibrator IC15 which ensures that the FIFO shift-out clock's pulse width is greater than 100nsec (narrower pulses may be ignored by one or more FIFO's, resulting in an "OUT OF SYNCH" condition).

Data is clocked out of the FIFO and to the DAC at a rate variable from 20.5kHz to 164kHz. The shift out clock is inhibited whenever the FIFO ARRAY is empty or the DELAY mode is selected.

As described above, data shifted thru the FIFO alternately represents samples of OUTA and OUTB. Due to the asynchronous nature of FIFO's it is impossible to determine whether a given output word is part of output A or B. It is therefore necessary to "tag" the data words so that they can be identified as belonging to the A or B output. Program counter signal PC4 is used as the "tag" bit (twelfth FIFO data bit). PC4 is zero when OUTA words are shifted into the FIFO array and one for OUTB words.

MAIN OUTPUT DAC

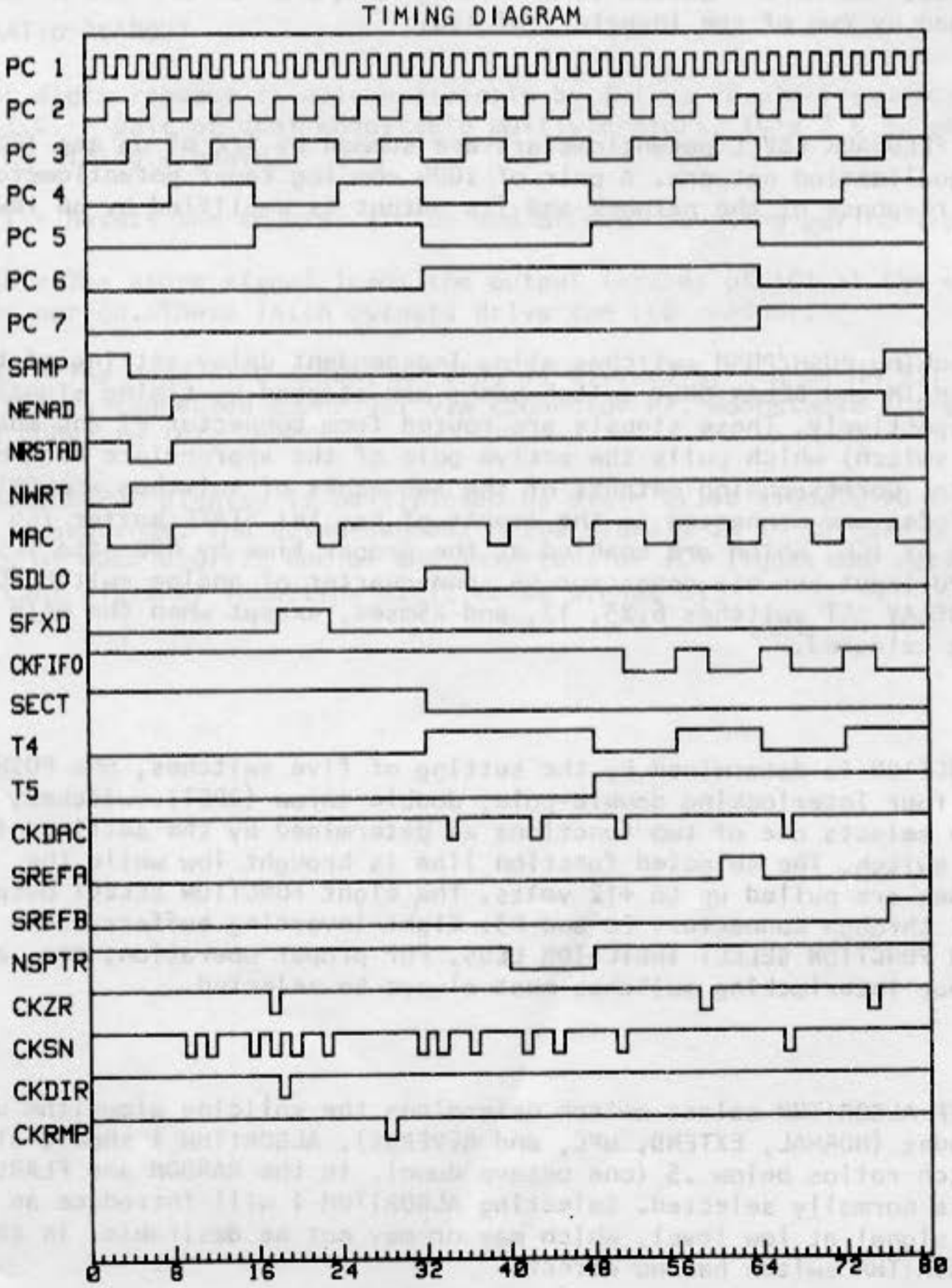
IC8, a 12-bit multiplying DAC and a pair of op amps, 1/2 of IC7, convert the FIFO outputs to an analog voltage. The output of IC7 is a multiplexed audio signal containing alternately OUTA and OUTB data at the RDFIFO clock rate. The "tag" data bit, designated A/B at the FIFO output, is used to de-multiplex the two pitch changed audio signals by appropriately gating the sample pulses of the two independent sample and hold cicuits. Two of the op amps of IC5 buffer the two output signals which are then AC coupled and summed by op amp IC1. The output of IC1 is designated MDAC and runs to connector D2.

MAIN OUTPUT REFERENCE VOLTAGE

As mentioned previously the CPU analog output contains three multiplexed signals REFA, REFB, and POINTER. The two reference signals must be applied to the MAIN OUTPUT DAC reference input during the time slot corresponding to the proper output, OUTA or OUTB. Since the output rate of the reference signals (CPU out) is system synchronous and the output rate of the two pitch changed outputs is not, the CPU output must first be de-multiplexed at a synchronous clock rate and then re-multiplexed at the pitch change rate.

A pair of analog switches, 1/2 of IC4, and 1/2 of quad op-amp IC3 sample and hold the two reference voltages, REFA and REFB. The two sample pulses are generated by NORing (IC11) uINST bit SREF with PC7. REFA and REFB are then multiplexed by a pair of analog switches, 1/2 of IC2, and summing amp IC5. FIFO "tag" output A/B and its inverse N(A/B) control the switches turning on REFA when OUTA is valid and REFB when OUTB is valid at the MAIN DAC output.

TIMING DIAGRAM



HP 941 REV. D - Front Panel P.C. Board

HP 941 supports all of the front panel controls and indicators with the exception of the POWER switch and the audio LINE switch. Three 14-pin DIP connectors, designated P1 through P3, connect the front panel p.c. board to the lower p.c. board HA 931. A fourth DIP connector, D4, routes delay set information to the upper p.c. board HD921.

P1 carries +15 and -15 volts as well as all audio connections. P2 and P3 carry +5 and +12 volts, FUNCTION and CONTROL MODE select lines, REPEAT, ALGORITHM and PITCH RATIO signals.

INPUT LEVEL

The INPUT LEVEL potentiometer is routed to connector P1. The cathodes of the LED level indicators are routed to P2 through current limiting resistors while the anodes are connected to +5 volts. The REPEAT switch is a locking PUSH-ON/PUSH-OFF switch whose output is de-glitched by two of the inverters of IC6.

FEEDBACK

The outputs of the FEEDBACK LEVEL potentiometers are summed by 1/2 of op amp IC8 which drives a passive equalization network. A pair of 100k ohm log taper potentiometers vary the frequency response of the network and its output is amplified by an inverting op amp 1/2 of IC8.

DELAY SET SWITCHES

Two banks of six locking PUSH/PUSH switches allow independent delay setting of the 949's outputs. The MAIN and DELAY ONLY switch banks are strobed by timing signals SREFB and SREFA respectively. These signals are routed from connector P3 and enable IC4 (a quad analog switch) which pulls the active pole of the appropriate bank of switches to +5 volts. Corresponding outputs of the two banks of switches are OR'd together through diodes and connected to the inputs of hex TRI STATE buffer IC6 (an 80C97). The outputs of IC6, which are enabled at the proper time by NOR gate IC5, are connected to the CPU input bus via connector D4. One-quarter of analog switch IC4 disables the MAIN DELAY SET switches 6.25, 12, and 25msec. except when the MAIN OUTPUT "DELAY" FUNCTION is selected.

FUNCTION SELECT

The MAIN OUTPUT FUNCTION is determined by the setting of five switches, one PUSH/PUSH type and a bank of four interlocking double-pole, double-throw (DPDT) switches. Each interlocking switch selects one of two functions as determined by the setting of the PUSH/PUSH FUNCTION switch. The selected function line is brought low while the remaining seven lines are pulled up to +12 volts. The eight FUNCTION SELECT outputs are routed to HA931 through connectors P2 and P3. Eight inverting buffers, IC's 5 & 6, drive the RED/GREEN FUNCTION SELECT INDICATOR LEDS. For proper operation, one, and only one, of the four interlocking switches must always be selected.

ALGORITHM SELECT

The PUSH-ON/PUSH-OFF ALGORITHM select switch determines the splicing algorithm used in the PITCH CHANGE modes (NORMAL, EXTEND, uPC, and REVERSE). ALGORITHM 1 should always be selected for pitch ratios below .5 (one octave down). In the RANDOM and FLANGE modes ALGORITHM 2 is normally selected. Selecting ALGORITHM 1 will introduce an additional delayed signal at low level, which may or may not be desirable. In the DELAY mode, the ALGORITHM switch has no effect.

CONTROL MODE SELECT

A bank of three interlocking DPDT switches selects the 949's pitch change control mode and also turns on the appropriate LED indicator. When the MANUAL control is selected, the front panel 10k linear pot controls the pitch ratio. When CV+MAN is selected the MANUAL control voltage is added to an external control voltage signal input at the rear panel terminal strip. The KEYBOARD control mode allows the pitch ratio to be controlled from an external keyboard or audio frequency oscillator (frequencies from 1.28kHz to 5.12kHz for pitch ratios from .5 to 2.00) when either the NORMAL, EXTEND or REVERSE MODE is selected.

NOTE: If the KEYBOARD CONTROL MODE is selected without applying a keyboard input signal, the PITCH RATIO is set to unity which FREEZES DELAY CHANGE. This allows delay change to be stopped at any point by pressing the KEYBOARD switch. While true in all modes, this feature is particularly useful in the FLANGE mode, allowing the user to stop the flange sweep at any point. Delay change (or flange sweep) starts again when one of the other control modes is selected.

PITCH RATIO READOUT

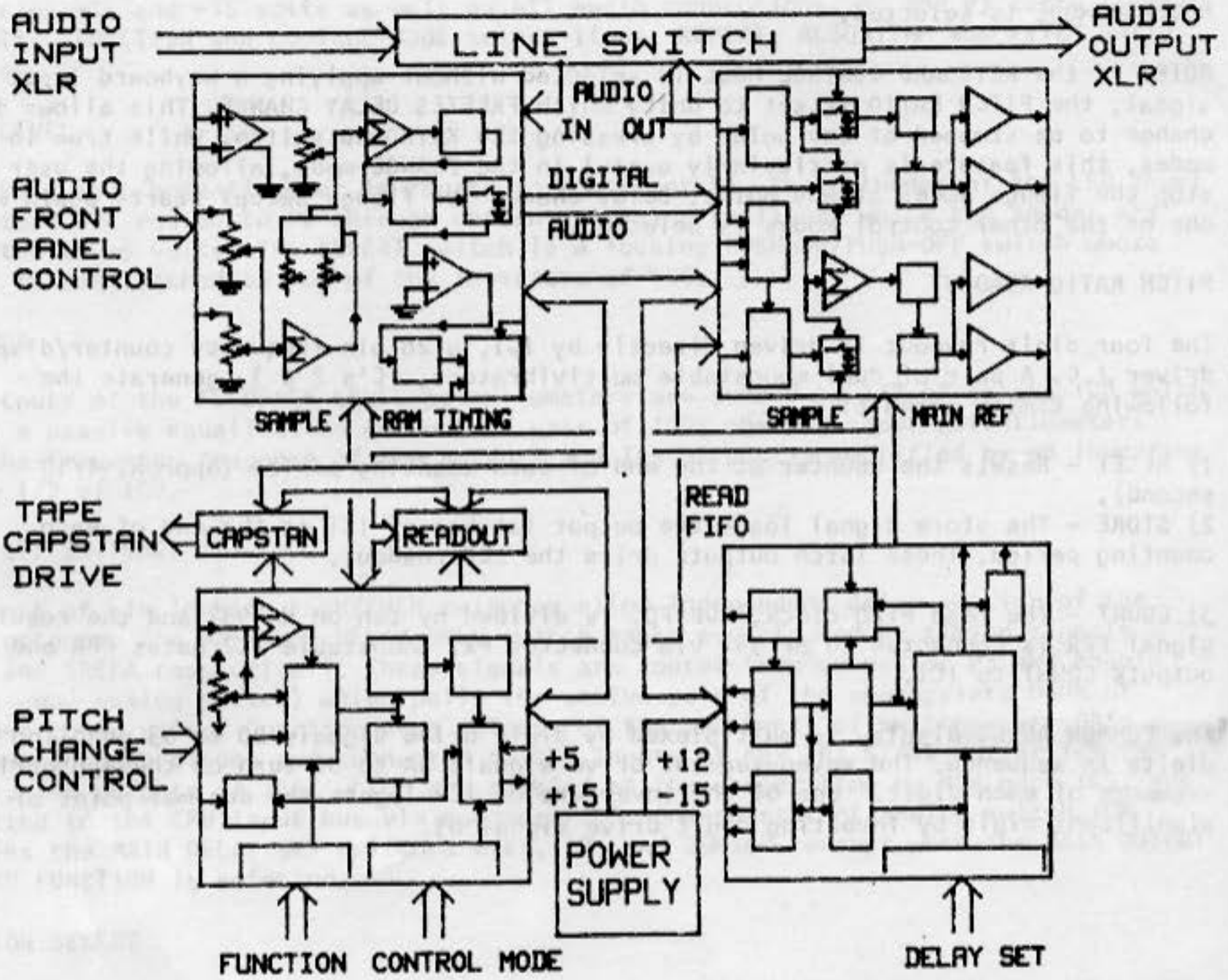
The four digit readout is driven directly by IC1, a 28 pin frequency counter/display driver I.C. A pair of dual monostable multivibrators, IC's 2 & 3, generate the following timing signals:

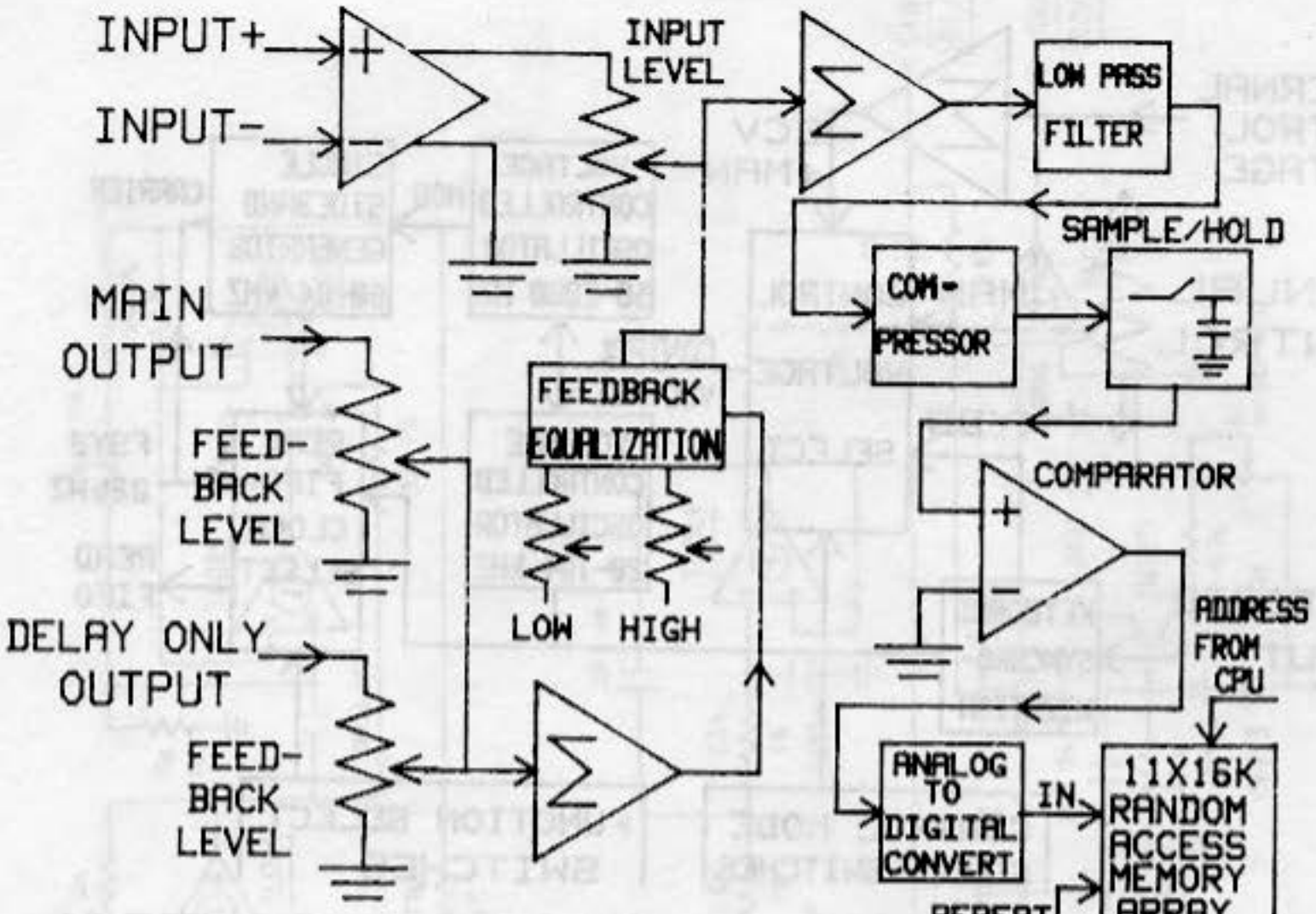
1) RESET - Resets the counter at the end of each counting period (approx. 1/10 second),
2) STORE - The store signal loads the output latches of IC1 at the end of each counting period. These latch outputs drive the LED readout.

3) COUNT - The read FIFO clock, RDFIFO, is divided by ten on HA 931 and the resulting signal FPR is connected to HP 941 via connector P2. Monostable IC2 gates FPR and outputs COUNT to IC1.

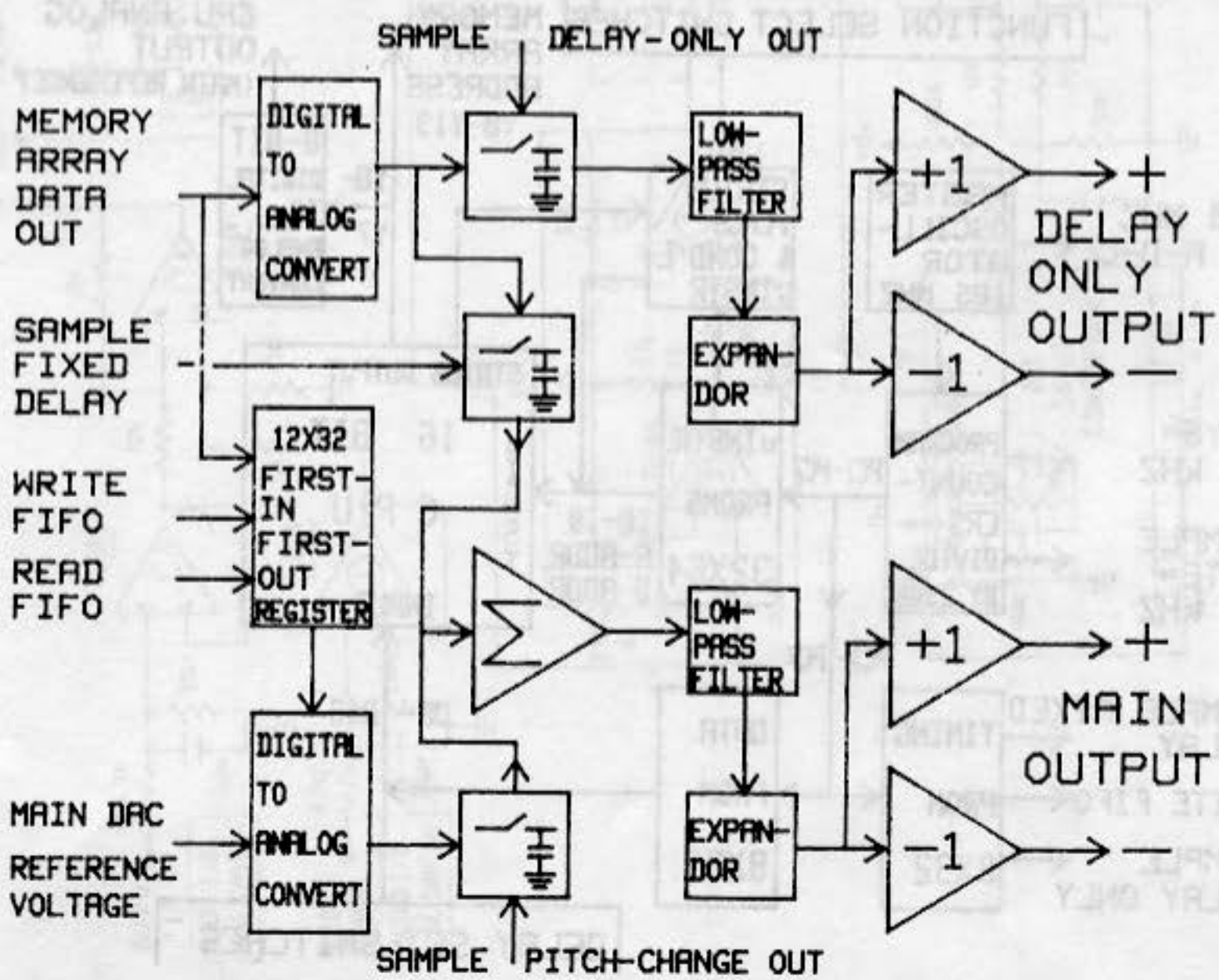
The COMMON ANODE display is multiplexed by digit drive signals D0 to D3 enabling the digits in sequence. The seven-segment drive signals SA to SG turn on the appropriate segments of each digit. One of the inverters of IC4 lights the decimal point of the most significant digit by inverting digit drive signal D3.

MASTER BLOCK DIAGRAM

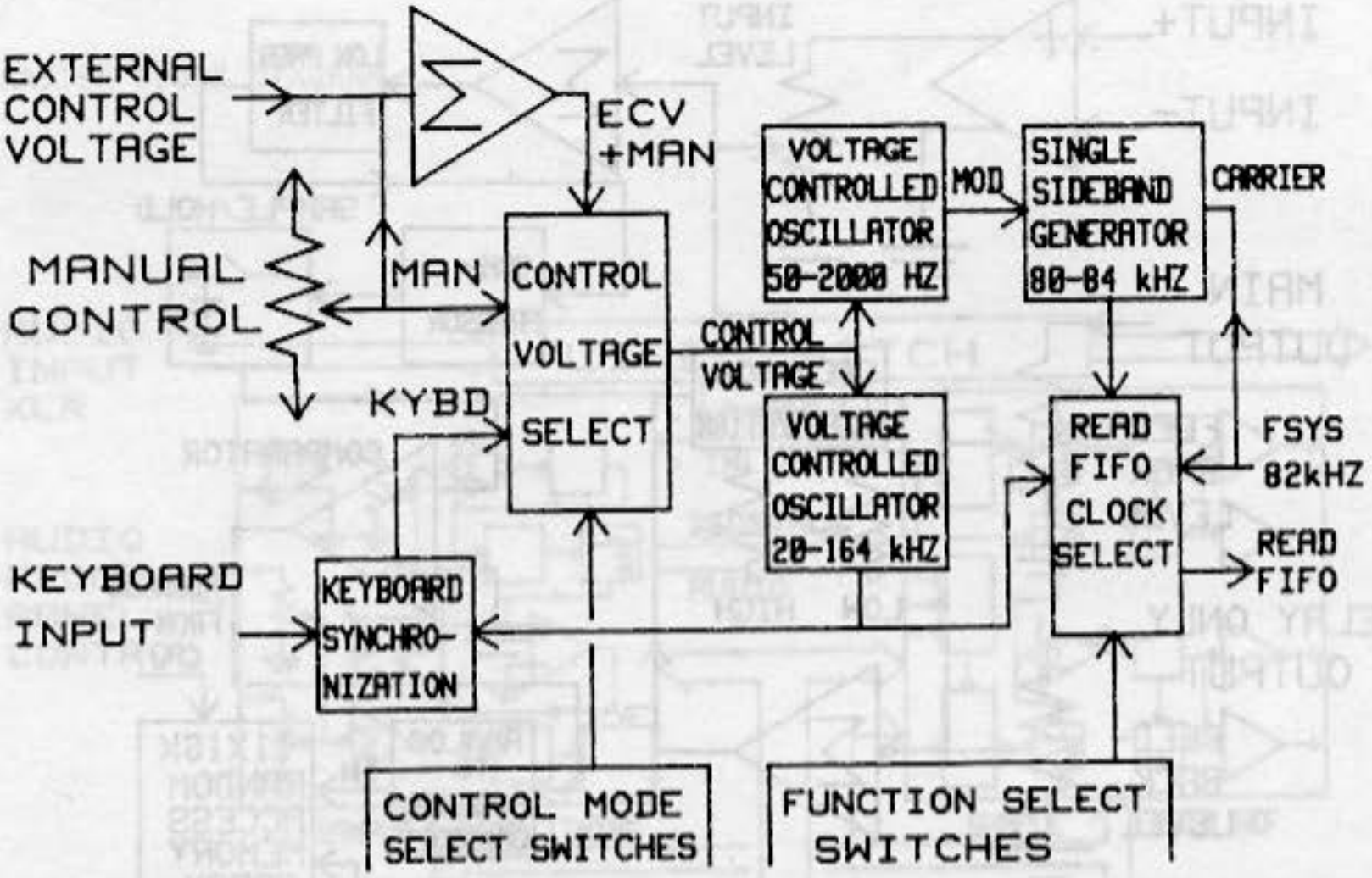




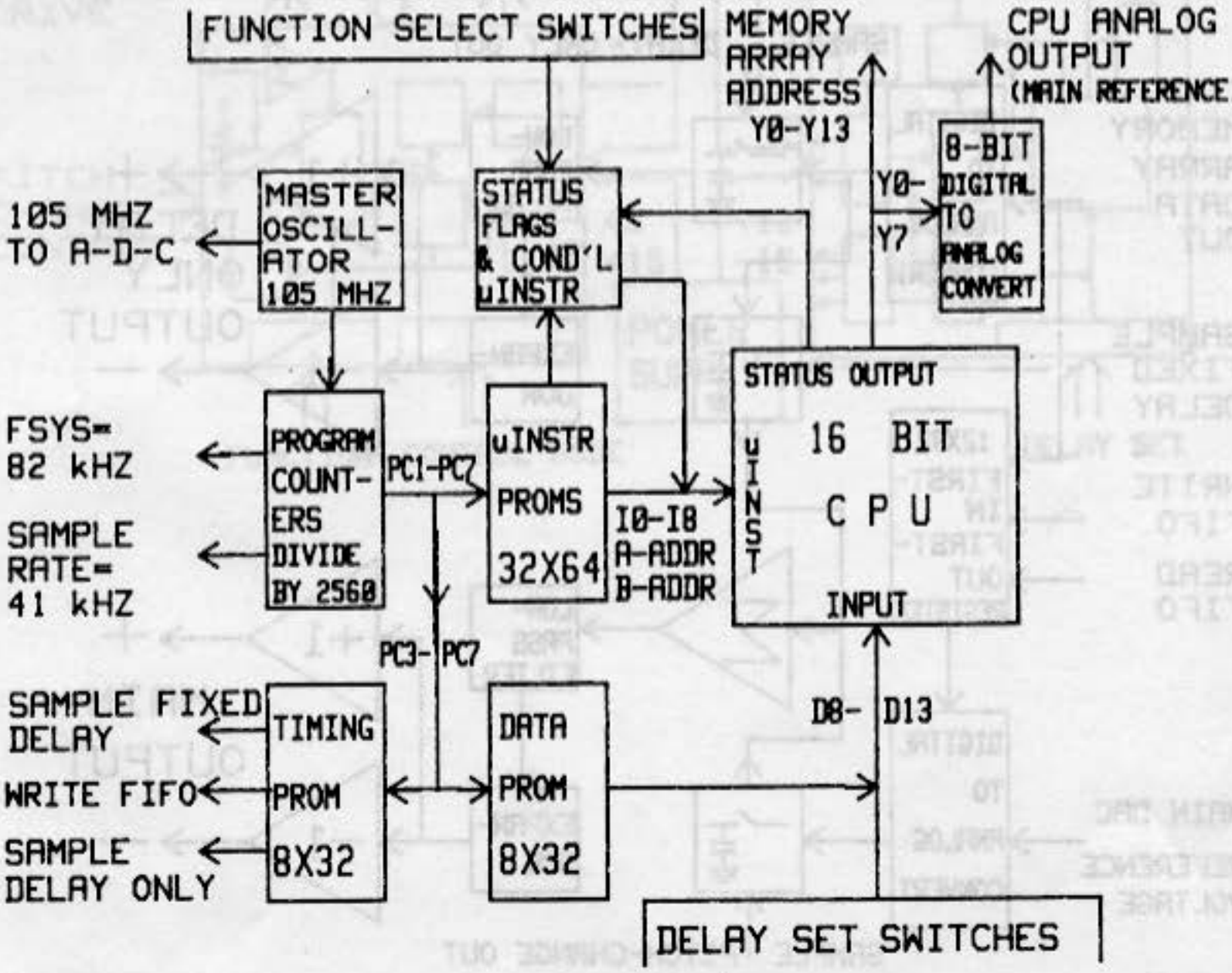
INPUT AUDIO PROCESSING



OUTPUT AUDIO PROCESSING



PITCH CHANGE TIMING & CONTROL



SYSTEM TIMING & CENTRAL PROCESSING UNIT

P1/14 LEVEL IN

P1/13 LEVEL OUT

P1/8 EQ OUT

AUDIO +IN

AUDIO I/O LINE SWITCH

AUDIO COM IN

AUDIO I/O LINE SWITCH

TL084

TL082

4066

74C909

1N914

1N753

2N3391

D8X INPUT COMPRESSOR

RMS SYM

IN LEVL

VCA SYM

FB LEVL

HIGH FREQ TRIM

OFFSET ADJ.

SAMP D2/4

CMP D2/5

INPUT AUDIO PROCESSING

HA 931 REV. C,D

SHEET 1 OF 6

VOLR 11-79

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D2/14 MDAC
(2) (DDAC)

8.66k 1%
15k 1%
576 1%
576 1%
976 1%
976 1%
976 1%
.0033 μF
TL084
.0033 μF
TL084
976 1%
2.94k 1%
24.9k 1%
140 1%
TL084
576 1%
576 1%
.0033 μF
TL084
464 1%

.044 μF
1.5k 1%
1.5k 1%
1.5k 1%
.01 μF
510Ω
TL082
(TL084)

+15v
-15v
2N3642
2N3638
470
10 μF
150
100k
TL084
MAIN OUT +
(DELAY OUT +)

10k
10k
+15v
-15v
2N3642
2N3638
470
10 μF
150
100k
TL084
MAIN OUT -
(DELAY OUT -)

* andrx till single ended

+15v
-15v
DBX EXPANDER
L
G
H
RMS SYM OUT LEVL
VCA SYM

NOTE: MAIN AND DELAY OUTPUT CIRCUITRY ARE IDENTICAL. DESIGNATIONS IN BRACKETS REFER TO DELAY ONLY OUTPUT.

LINE SWITCH

6 POLE / DOUBLE THROW PUSH - PULL SWITCH

AUDIO I/O MOLEX SOCKET

PIN ASSIGNMENTS

PIN #	SIGNAL	
1	GND	
2	COM	DELAY ONLY XLR
3	+	DELAY ONLY XLR
4	GND	
5	+	AUDIO IN XLR
6	COM	AUDIO IN XLR
7	GND	
8	COM	MAIN OUT XLR
9	+	MAIN OUT XLR

VOL.II 12-79

OUTPUT AUDIO PROCESSING

HA 931 REV. C,D SHEET 2 OF 6

* OBS Andrx 83.08.25 GS

150 MAIN OUT
DELAY OUT

P3/1 KYBD

KYBD/2 GLIDE 1

KYBD/3 GLIDE 2

TERM 7 REF FREQ

54 F SYS

TERM 9 FROM KBD

P3/2

TERM 11 CV FM ECV IN

P3/3 MANV

ECV LEVEL

ECV OFFSET

74C74

4024

4066

4046 PHASE DETECTOR

74C909

74C86

74C00

74C02

74C04

TL064

1N914

VCO 4151

CONTROL VOLTAGE

MAX F

FPR P2/9

CAPIN

16K RDFIFO D2/7

FSYS 54

SSB 54

REVS P3/12

EXT DLY P3/13 P2/8

NPC P3/14

54 CVLT

P3/6 RMPR RMCV P2/10

SELVCO 55

VOLTAGE CONTROLLED OSCILLATOR AND READ FIFO CLOCK SELECT

HA 931 REV. C,D

SHEET 3 OF 6

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DZ/11 PNTR

SHFT PRN

FSYS

RND P3/8

4066

74C909

74C74

74C04

μP11 P3/11

μP8 P3/10

CARRIER 1

CARRIER 2

1496

TL084

4017

PC2 D3/6

SSB1

SSB2

1N753

1N914

SSB

TRANG

CVLT

RVF

SINGLE SIDE BAND GENERATOR

HA931 REV. C, D SHEET 4 OF 6

D2/6 D2/10 D3/4 D3/2 D3/1 D2/9

DLAY FLNG REV RVF EXTD RSTFIFO

SHFT PRN CNT FSYS TRANG CNT

P2/8 DLY

74C04

+5v

6.8k

FUNCTION SELECT LOGIC

74C909

P3/8 RVD

P3/9 FLG

74C00

P3/12 REVS

P3/13 EXT

SELVCO

100k .01 74C86

74LS85

74C193

74C10

825123

AD6 AD7 AD8 AD9 AD10

D3

NWRT

D3/5

RPT LMT 3 2 1 PRS

NRM

P2/4

P2

74C10

5µ 10v

AUDIO LEVEL INDICATOR CIRCUITRY

+12v 100k TL064 +6v 100k 1µf

400b 74C909 74C86 4024

74C74 74C04 74C02

PSEUDO RANDOM NOISE GENERATOR

+5v 100k 33k

14518 14518

DISPLAY TIMING

TERM/5 14.2 MHz

10K

TERM/3 9.6 MHz CAPSTAN DRIVE REAR TERMINAL STRIP

TERM/1 60 MHz

Buffrade med 74LS244

10k 8.2k OUT

4046 14528 14518 4024

.0033µf 18k 10k 220n

TL064 33k 47µf 100k 5k -15v CAP CAL

4066 100 1µf

14528 18k 220n 22k .033µf

CAPSTAN DRIVE

CAPIN

FUNCTION SELECT LOGIC, AUDIO LEVEL INDICATOR, PSEUDO RANDOM NOISE GENERATOR, CAPSTAN DRIVE AND DISPLAY TIMING CIRCUITRY

HA 931 REV. C,D SHEET 5 OF 6

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AC LINE MODULE

POWER

FUSE

120V 240V

B NC C D E F

JUMPER CARD

REAR VIEW

L S R H J N

ON RIGHT SIDE

+15V REGULATOR

+12V REGULATOR

S2-5 S2-1 S2-3

1000µF 25V

1µF

+15V +12V

S2 2 4 6

1000µF 25V

NEGATIVE REGULATOR

IN OUT COM

INPUT AND TAB

-15V

POWER TRANSFORMER

5 4 2 1

6 7 8 9 10

S1-3 S1-1 S1-2 S1-4 S1-6 S1-5

S3-4 S3-5

ON CIRCUIT BOARD

ON REAR PANEL

5V REGULATOR

IN OUT COM

+5V

S3-2 S3-1 S3-3 S3-6

2200 µF 16V

UNDER S3 (COMPONENT SIDE)

(L) IS HOT SIDE OF LINE

(N) IS NEUTRAL (LOW SIDE)

AB 1/1679

POWER SUPPLY

HA931 REV C,D

SHEET 6 OF 6

ANALOG-TO-DIGITAL CONVERTER (S4) OUTPUT TO 11x16 RAM ARRAY DATA INPUT

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10

LSB MSB

+5v

10K

74C909

74C00

4.7K 4.7K

470 470 470 470 470

74LS112

74LS193

22

2N3639

560 150 560

10131 10131

NENAD (S3)

CMP (D2/5)

NRSTAD (S2)

360PF 74C00

270 50 1K 22 22PF 50

MASTER OSCILLATOR

2N3639 2N3639

33PF 1K 68PF 3.3PF

.001 10K

105MHz

74S113 74LS112

74LS193 74LS192

100K 1uF/5v

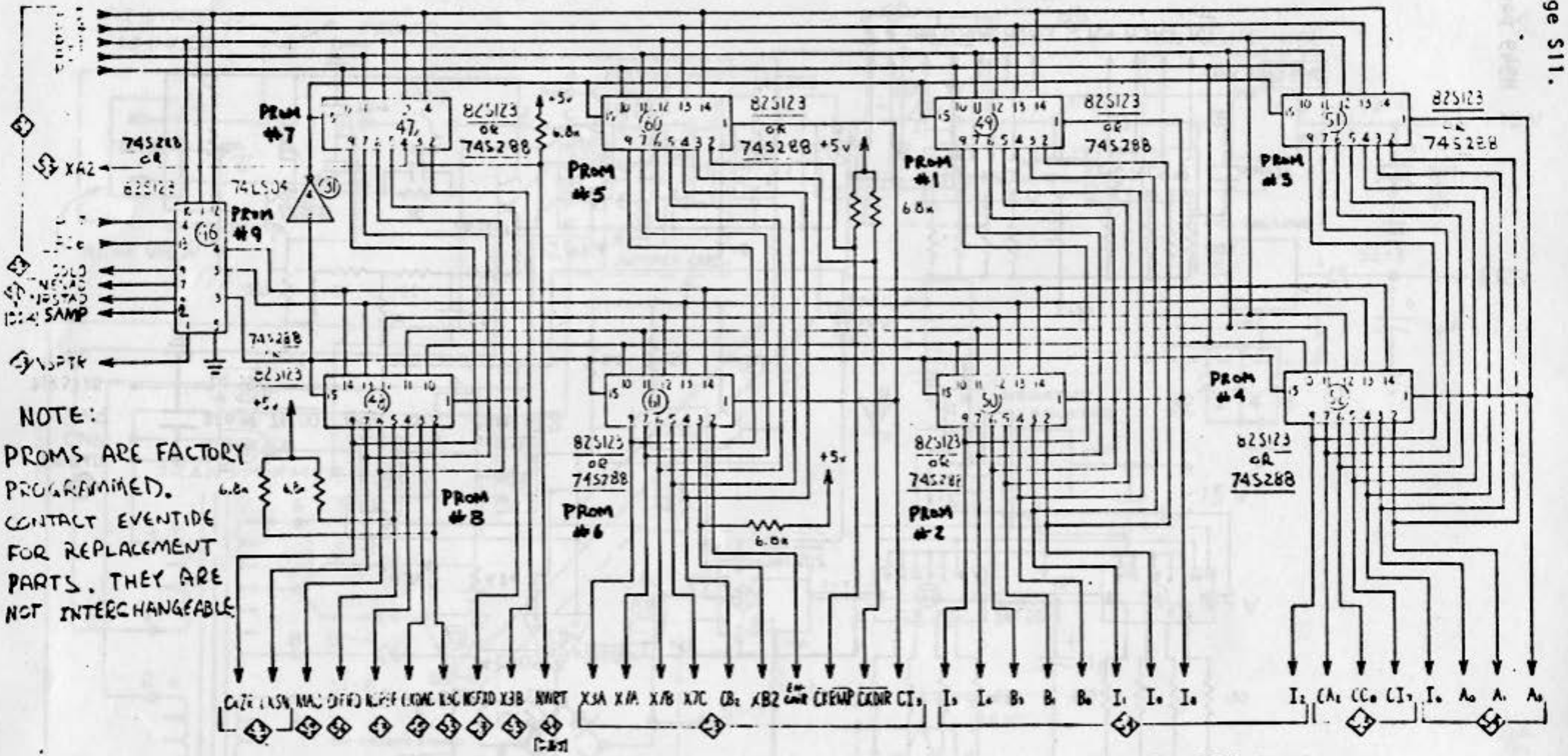
PC2 (D3/6)

Ø Ø CCPU CCPU PC1 PC2 PC3 (S5) PC4 PC5 PC6 PC7 (S2)

MASTER OSCILLATOR, PROGRAM COUNTERS, AND ANALOG-TO-DIGITAL CONVERTER

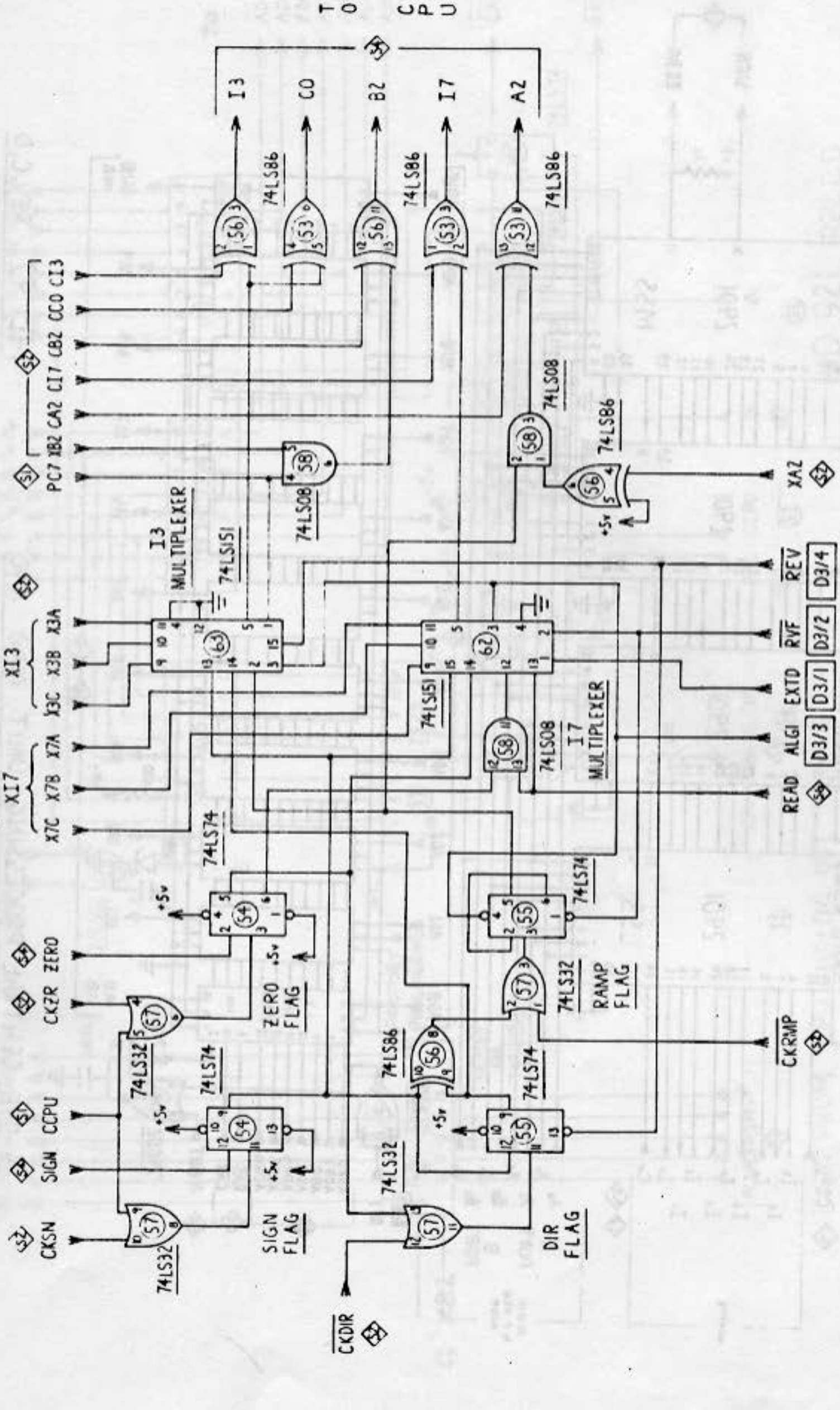
HD 921 REV. C.D

SHEET 1 OF 7



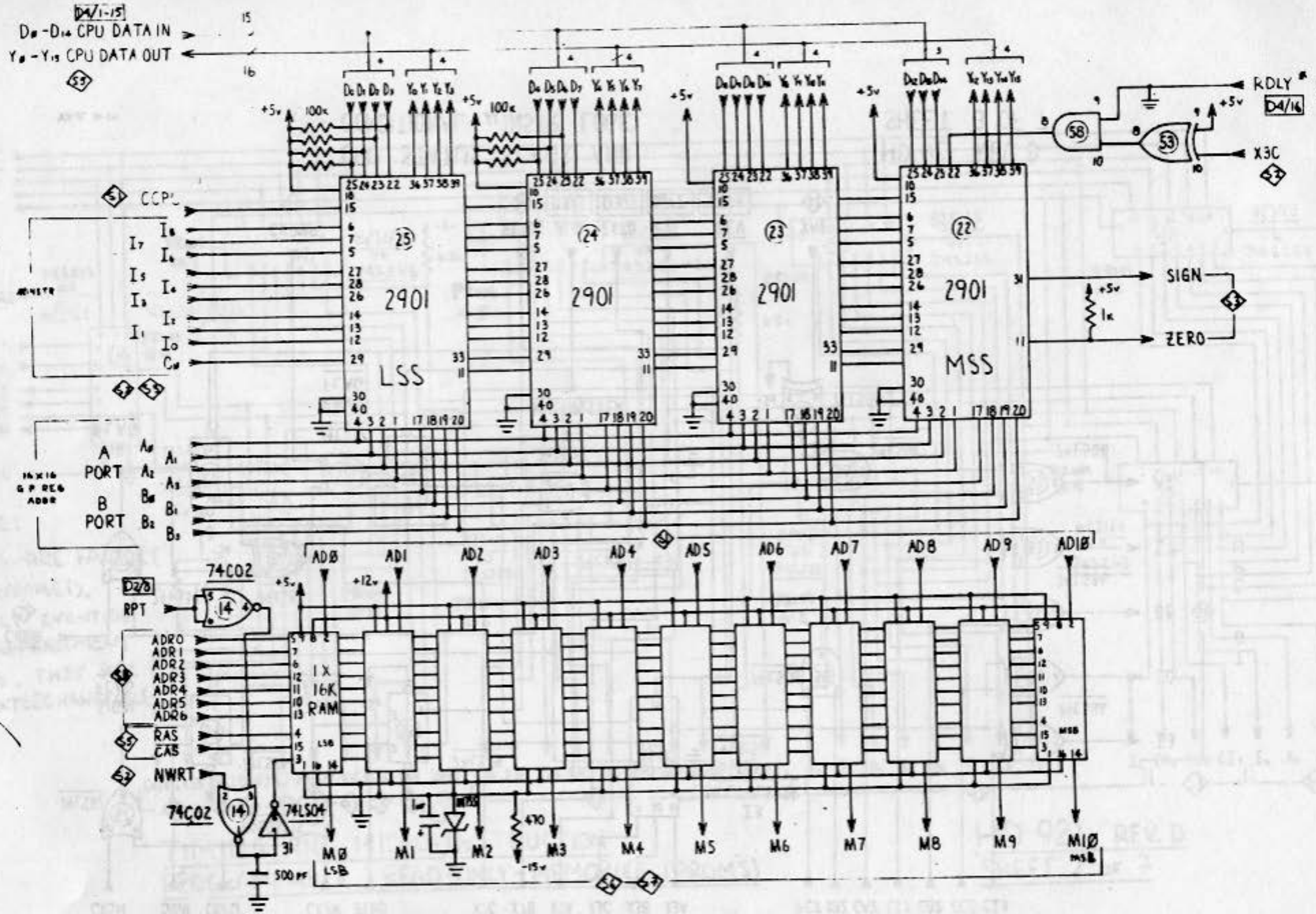
TIMING AND MICRO-INSTRUCTION
PROGRAMMABLE READ-ONLY-MEMORIES (PROMS)

HD 921 REV. D
SHEET 2 OF 7



HD 921 REV.D
SHEET 3 OF 7

CPU STATUS FLAGS AND
CONDITIONAL μINSTR LOGIC



16-BIT CENTRAL PROCESSING UNIT (CPU) AND
11 x 16K DYNAMIC RANDOM ACCESS MEMORY ARRAY (RAM)

HD 921 REV. C,D
SHEET 4 OF 7

TO CPU IN

D7 D8 D9 D10 D11 D12 D13 D14

XB2

DPROM (43) FACTORY PROGRAMMED

82S123 OR 74S288

PC3 PC4 PC5 PC6 PC7

CKDAC CCPU

72LS02 (11)

74LS374 (38)

74LS374 (39)

74LS374 (40)

FROM CPU OUT

Y15 Y0 Y1 Y2 Y3 Y4 Y5 Y6

Y14 Y7 Y8 Y9 Y10 Y11 Y12 Y13

TO RAM

ADR6
ADR5
ADR4
ADR3
ADR2
ADR1
ADR0

+5v

7523 (37)

1uF/15v

2.2k

5k CPU LEVEL

-15v

TL081 (36)

100

CPU ANALOG OUT

74LS74 (42)

74LS74 (42)

74LS74 (41)

74LS74 (41)

CAS

RAS

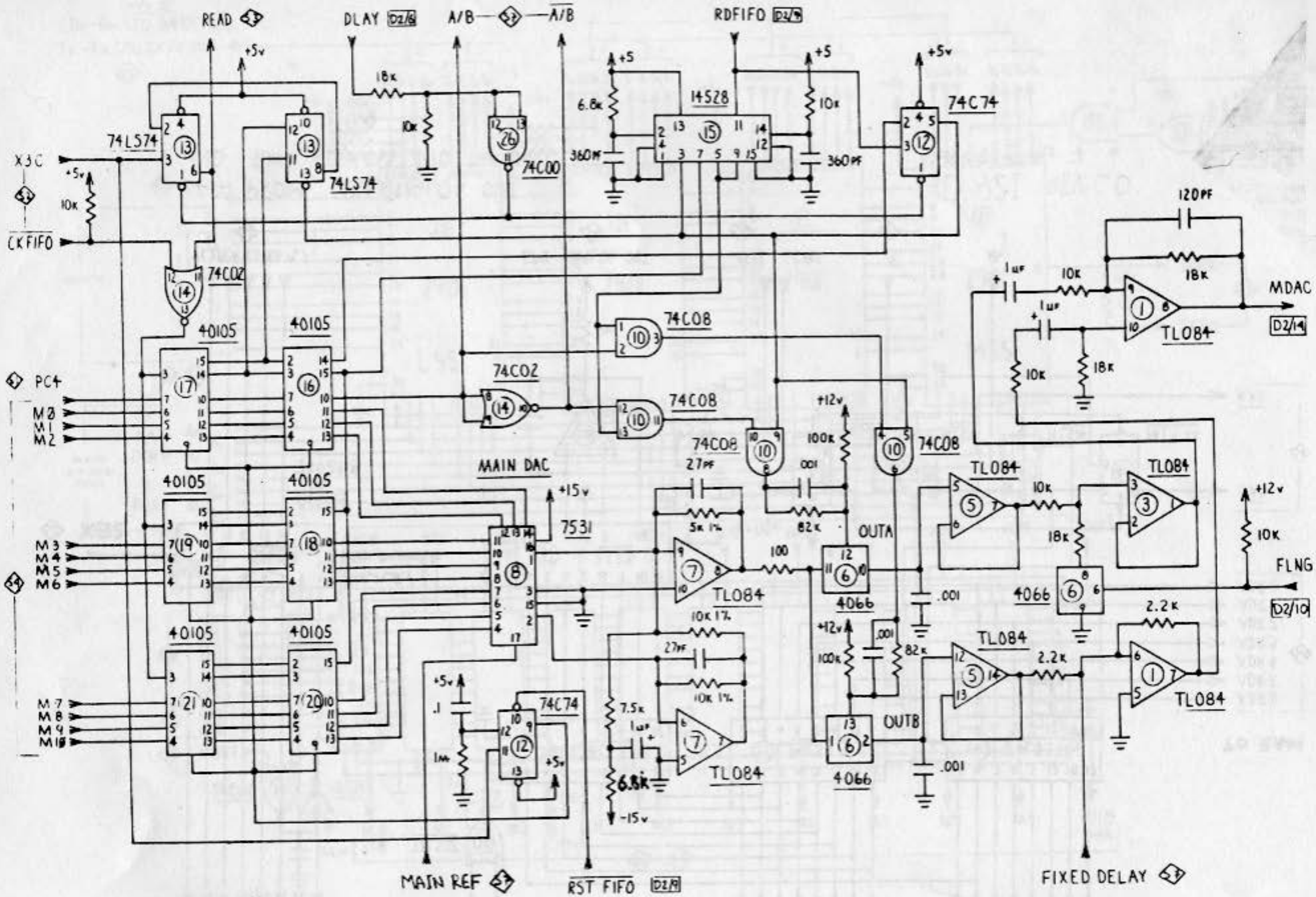
MAC CCPU

$\overline{\emptyset_1}$

$\emptyset_1$

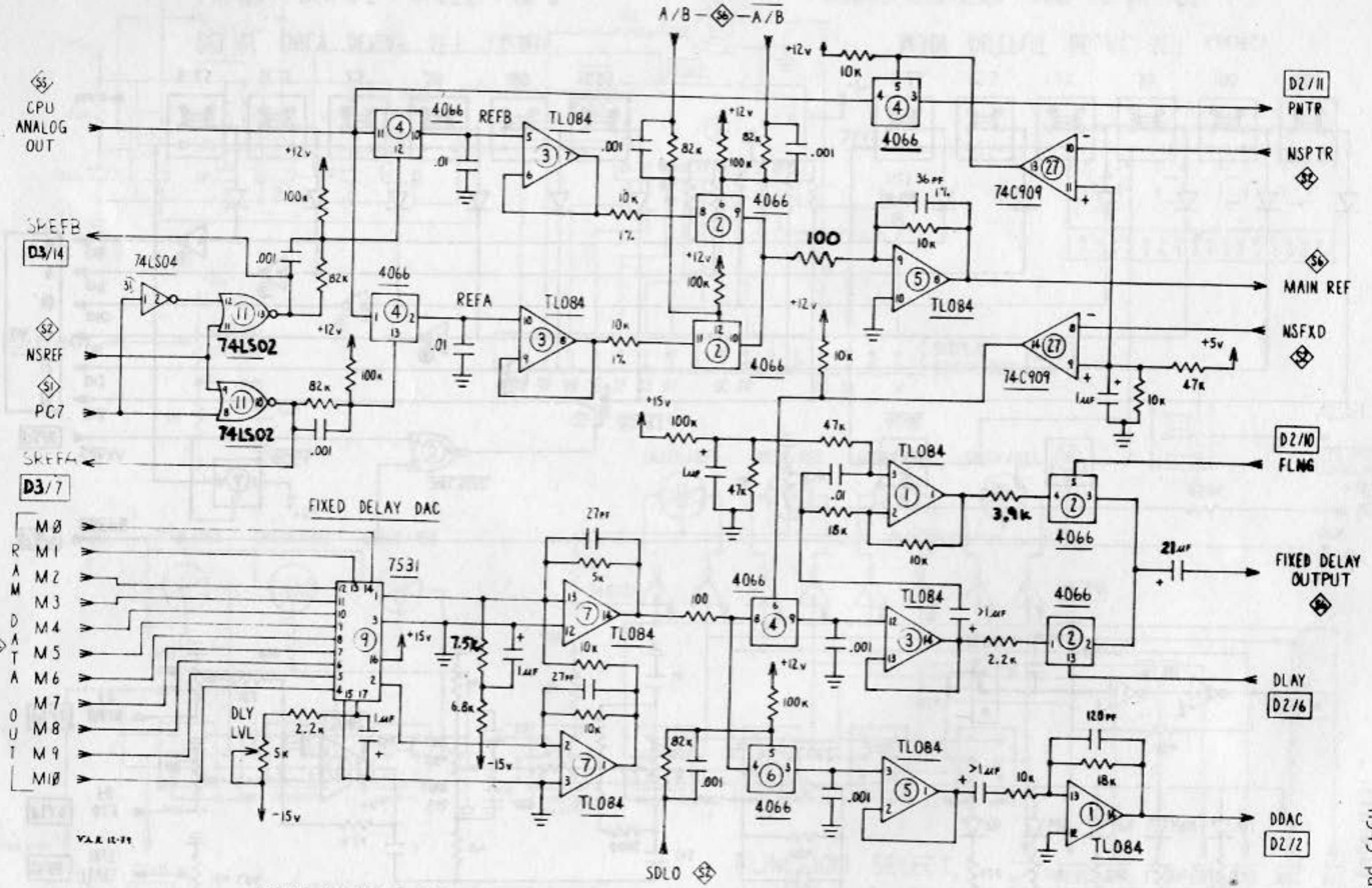
DATA PROM, CPU ANALOG OUT
AND RAM ADDRESS AND TIMING

HD 921 REV. C.D
SHEET 5 OF 7



FIFO ARRAY AND TIMING,
MAIN OUTPUT DAC

HD 921 REV. C,D SHEET 6 OF 7


A/B
-A/B
CPU ANALOG OUT
4066
REFB
TL084
.001
.01
82K
100K
+12V
10K
1%
4066
4066
74C909
36PF
1%
100
D2/11
PNTR
NSPTR
SREFB
D3/14
74LS04
74LS02
74LS02
4066
REFA
TL084
.01
.001
82K
100K
+12V
10K
1%
4066
TL084
MAIN REF
NSFXD
74C909
+5V
47K
1uF
NSREF
PC7
SREFA
D3/7
+15V
100K
47K
TL084
.01
.001
15K
10K
3.9K
4066
D2/10
FLNG
FIXED DELAY DAC
RAM DATA OUT
M0
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
7531
27PF
5K
TL084
100
4066
21uF
FIXED DELAY OUTPUT
7.5K
1uF
+15V
10K
27PF
10K
TL084
4066
>1uF
2.2K
DLY LVL
5K
2.2K
1uF
6.8K
-15V
-15V
+12V
100K
82K
.001
TL084
120PF
18K
>1uF
10K
4066
.001
DDAC
D2/12
DLAY
D2/6
SDLO
MAIN OUTPUT REFERENCE VOLTAGE
AND DELAY ONLY DAC
HD 921 REV. C,D
SHEET 7 OF 7
H949 page S16.

P1/14 LEVEL IN
P1/13 LEVEL OUT
P1/9 DLY FB
P1/1 MAIN FB
10K LOG
10K LIN
4.7K
.1
+15V
-15V
TL082
EQ LOW
680K LOG
.039
.33
10K
1K
.015
EQ HI
100K LOG
.001
P1/8 EQ OUT

LMT NRM3 NRM2 NRM2 PRS
620 270 270 270 270
RD GRN GRN GRN YEL
+5V

+12V
REPEAT
.01
330K
74C901
100K
P2/4 RPT

P3/4 SREFB
SREFA
P3/5
D4
D13 D12 D11 D10 D9 D8
4066
74LS02
80C97
10K
15K
DLY S2
@ 10K (6)
@ IN914 (12)
6.25 12.5 25 50 100 200

DELAY ONLY DELAY SET (μSEC)

MAIN OUTPUT DELAY SET (μSEC)

HP 941 REV. D,E SHEET 1 OF 2

AUDIO CONTROL AND DELAY SET

P2/9 FPR

P2/5 CNT

74LS02

+5v

22k

200m

100k

14528

.01

14528

14528

100k

.01

72LS02

100

RESET

STORE

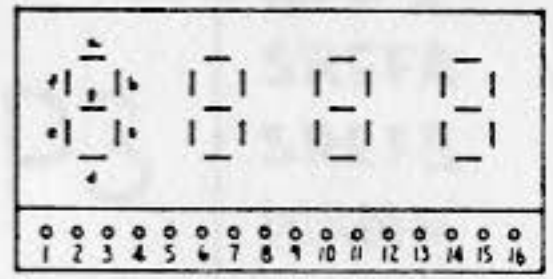
COUNT

7217

+5v

DISPLAY CONNECTOR (FRONT PANEL SIDE)

SG DP DB SE SF SB DI SC D2 D3 SD SA



P3/3 MANV

+12v

MANUAL 10k LIN

1K

1 uF

-15v

+5v

ALG1

P3/7

GREEN / RED GREEN / RED GREEN / RED GREEN / RED

DLY

1k

74C901

74C901

680 680 680

+12v

100

+5v

100

MAN + CV

KEYBOARD

MANUAL

FUNCTION SELECT

DELAY NORM PC

RANDOM EXTEND PC

FLANGE uPC#

REVERSE uPC#

KYBD P3/1

CV+M P3/2

uP3 REVS uP# FLG EXT RND NPC DLY

10 12 11 9 13 8 14

P3

P2/8

HP 941 REV. D,E SHEET 2 OF 2

FUNCTION SELECT, CONTROL, AND DISPLAY

REV	DESCRIPTION		DATE
01	PER ECO#435	PT	8-21-78
02	PER ECO# 450	DT PT	11-10-78

PLAY BACK CONTROL (1)
RECORD CONTROL (4)
SIGNAL INPUT (2)
RECORD PRE-EMPHASIS (3)
DETECTOR INPUT (11)
FILTER OUTPUT (8)
GND (12)
PLAY BACK DE-EMPHASIS (5)
SIGNAL OUTPUT (6)
CONTROL SIGNAL OUTPUT (10)
-15V (7)
+15V (9)

R2 392 1%
R3 392 1%
R4 82K
R5 390
R6 100 1%
R7 50K VCA LOG.
R8 50K PLAY LEVEL MATCH
R9 50K RECORD LEVEL MATCH
R10 30K
R11 100 1%
R12 100 Δ
R13 6.8K
R14 3.9K
R15 100
R16 1.3K
R17 270
R18 2.7K
R19 30.1K 1%
R20 100K 1%
R21 1K
R22 4.7K
R23 50K VCA SYM.
R24 750K
R25 6.8K
R26 100K 1%
R27 30.1K
R28 4.7K
R29 15K
R30 15K
R31 100K
R32 4.7K
R33 *
R34 4.7
R35 RMS SYM. 50K
R36 2.2M
R37 20K 1%
R38 10K 1%
R39 1K
R40 1M
R41 3.01K 1%
R42 30.1K 1%
R43 4.7K
C1 .01 CD 20%
C2 3.3NF PP
C3 68PF CD 10%
C4 10PF CD10%
C5 100PF CD20%
C6 .33 MY. ±5%
C7 68PF CD 10%
C8 3.3NF PP
C9 330PF PP
C10 3.3NF PP
C11 3.3NF PP
C12 .1 MY. ±5%
C13 .012 PC 5%
C14 OPT. .001 CD 20%
C15 * TA
C16 OPT. 10PF CD 10%
C17 1/35 TA.
C18 1/35V TA
C19 OPT. CD 10%
Q1 142081
Q2 142081
Q3 142091
Q4 142081
QA1 □ 142151
QA2 146221
QA3 △ 142161
OA1
OA2
OA3 146251

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE EXPRESSED IN OHMS AND ARE VAW ± 5%.
   B. CAPACITORS ARE EXPRESSED IN MICROFARADS.
   C. OP AMPS ARE #146241.
#2. SELECT C15 + R33 PER SPEC. DWG. A160001.
Δ 3. SELECT QA3 PER. SPEC. DWG. 160002.
□ 4. SELECT QA1 PER. SPEC. DWG. 160016.

dbx INC. WAKEFIELD, MASS.
SCHEMATIC
MODEL 303C TYPE II 15V
340123 02

HA 931 — HP 941

P1 (8 7 / 14 1)

EQOUT	8	7
DLYFB		
-15 v		
LEVEL OUT		
LEVEL IN	14	1

P1 (8 7 / 14 1)

+15v	8	7
GROUND		
GROUND		
MAIN FB	14	1

P2 (8 7 / 14 1)

DLY	8	7
FPR		
RMCV		
+12v		
LMT		
PRS		
+5v	14	1

P2 (8 7 / 14 1)

GROUND	8	7
CNT		
RPT		
NRM3		
NRM2		
NRM1	14	1

P3 (8 7 / 14 1)

$\overline{\text{RND}}$	8	7
$\overline{\text{FLG}}$		
$\overline{\mu\text{PC}}$		
$\overline{\mu\text{PC\#}}$		
$\overline{\text{REVS}}$		
$\overline{\text{EXT}}$		
$\overline{\text{NPC}}$	14	1

P3 (8 7 / 14 1)

ALG1	8	7
RMPR		
SREFA		
SREFB		
MANV		
CV+M		
KYBD	14	1

HD921 — HA931

D1

○	+12v
○	GROUND
○	+5v
○	+5v
○	GROUND
○	+12v

D2 (8 7 / 14 1)

RPT	8	7
$\overline{\text{RSTFIFO}}$		
FLNG		
PNTR		
GROUND		
+15 v		
MDAC	14	1

D2 (8 7 / 14 1)

RDFIFO	8	7
DLAY		
CMP		
SAMP		
GROUND		
DDAC		
−15v	14	1

D3 (8 7 / 14 1)

GROUND	8	7
AD6		
AD7		
AD8		
AD9		
AD10		
SREFB	14	1

D3 (8 7 / 14 1)

SREFA	8	7
PC2		
NWRT		
$\overline{\text{REV}}$		
ALG1		
$\overline{\text{RVF}}$		
EXTD	14	1

HD921-HP941

D4 (8 7 / 14 1)

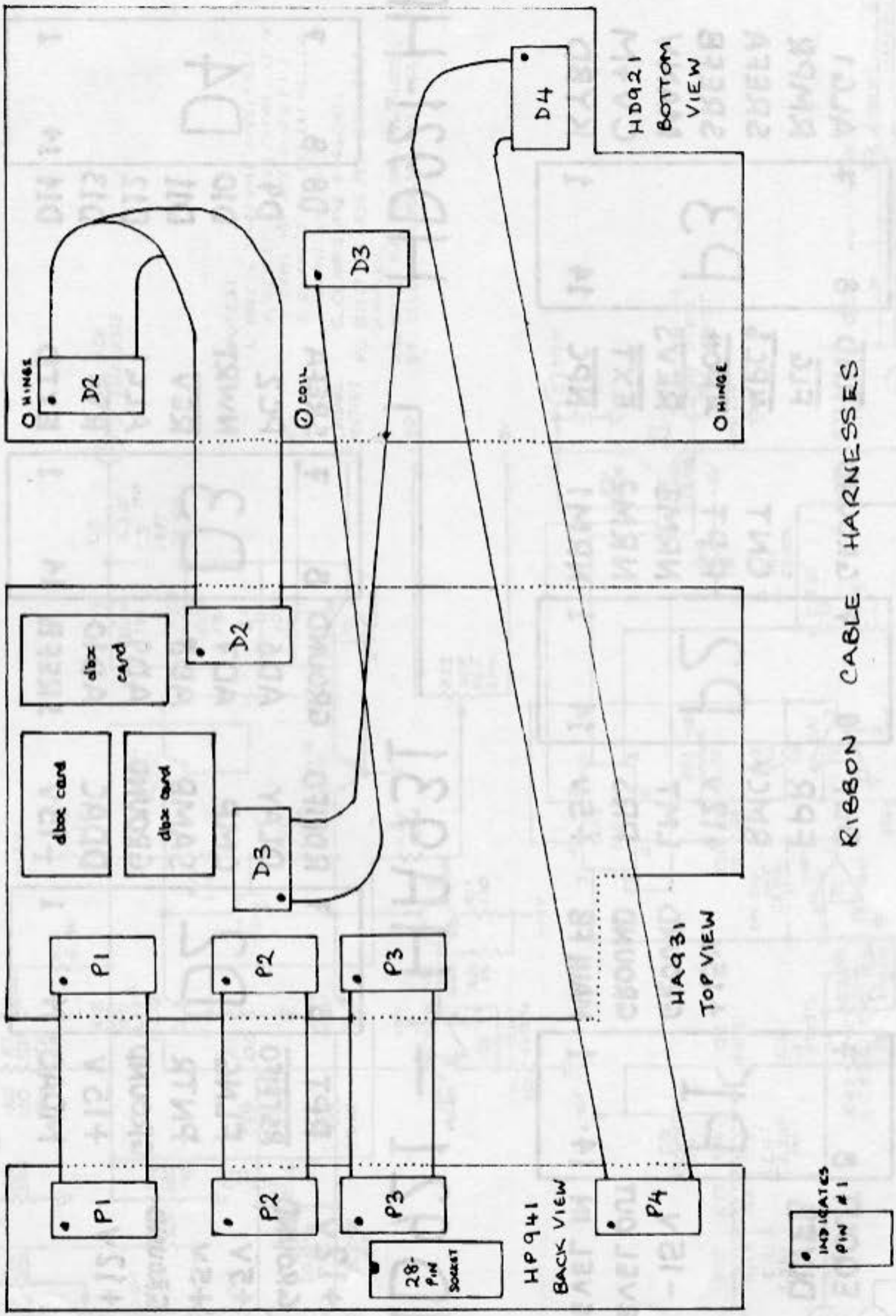
D8	8	7
D9		
D10		
D11		
D12		
D13		
D14	14	1

D4 (8 7 / 14 1)

D7	8	7
D6		
D5		
D4		
D3		
D2		
D1	14	1

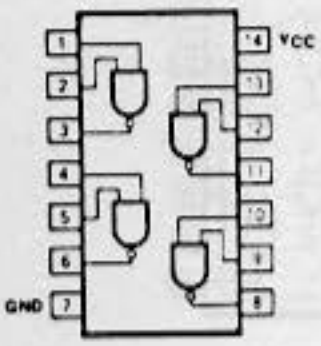
INTER-BOARD CONNECTORS

APPENDIX - Ribbon Cable Harnesses used in H949 Harmonizer

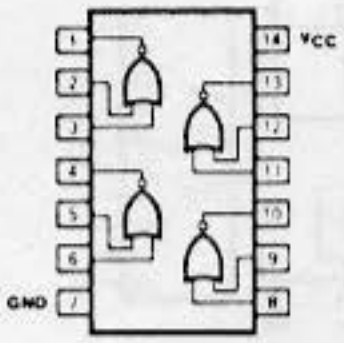


APPENDIX Integrated circuits used in H949 Harmonizer

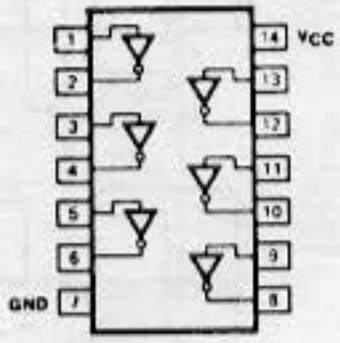
74LS00, 74C00
Quad 2-input
NAND gate



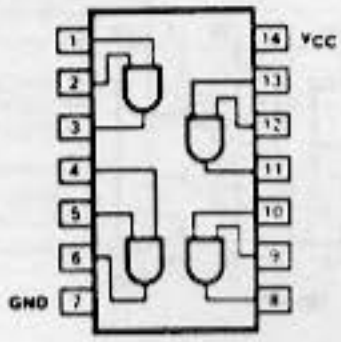
74LS02, 74C02
Quad 2-input
NOR gate



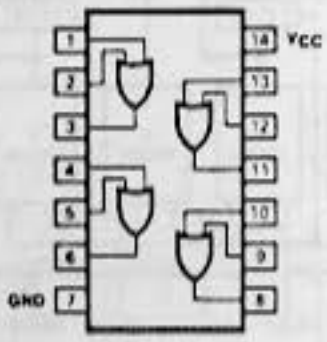
74LS04, 74C04
Hex inverter



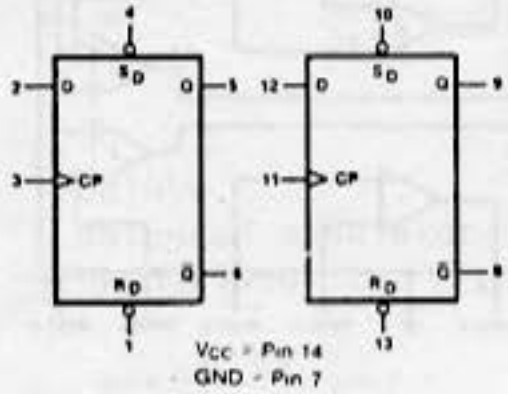
74LS08, 74C08
Quad 2-input
AND gate



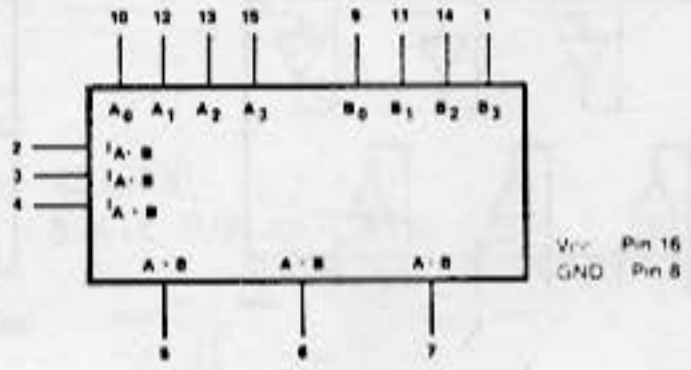
74LS32
Quad 2-input
OR gate



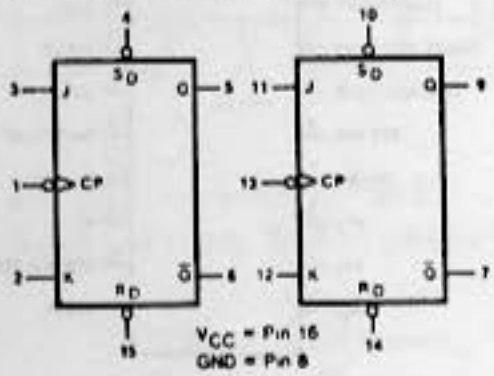
74LS74, 74C74
Dual positive edge-
triggered flip-flop



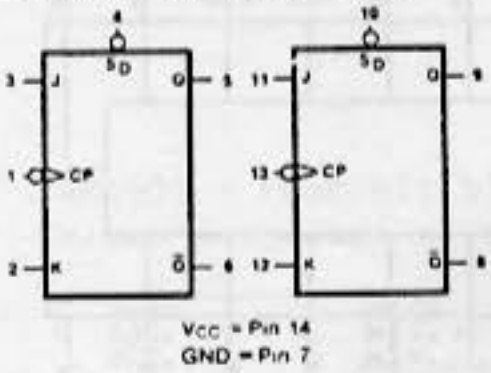
74LS85
4-bit magnitude
comparator



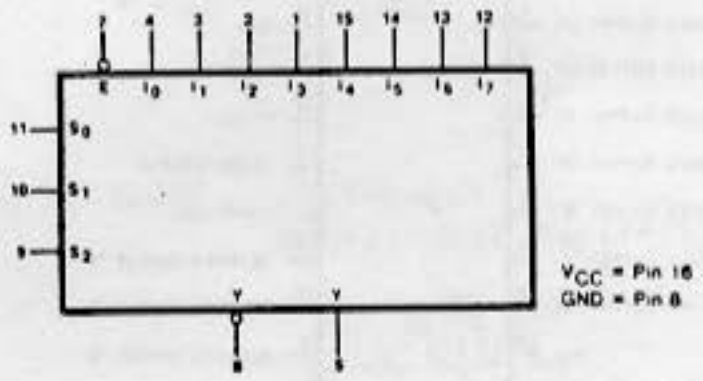
74LS112, 74S112
Dual JK negative edge-
triggered flip-flop



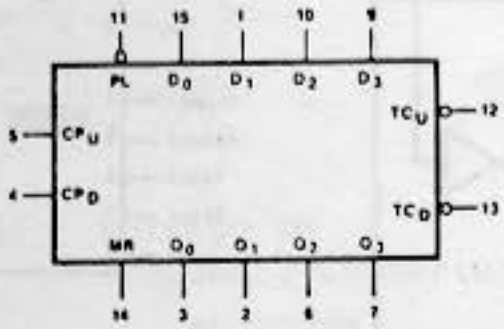
74LS113, 74S113
Dual JK negative edge-
triggered flip-flop



74LS151
8-to-1 multiplexer



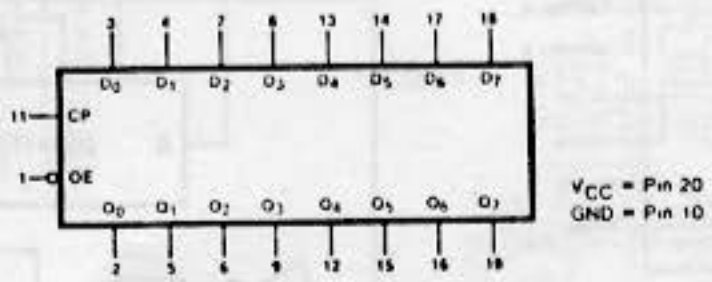
74LS192
BCD decade
up/down counter



74LS193, 74C193
4-bit binary
up/down counter

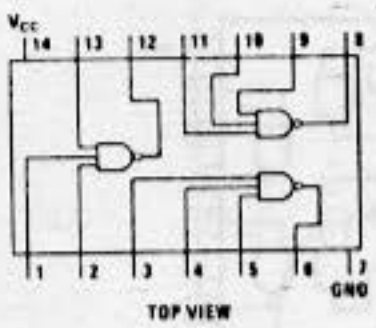
VCC Pin 16
GND Pin 8

74LS374
Octal D flip-flop (3-state)

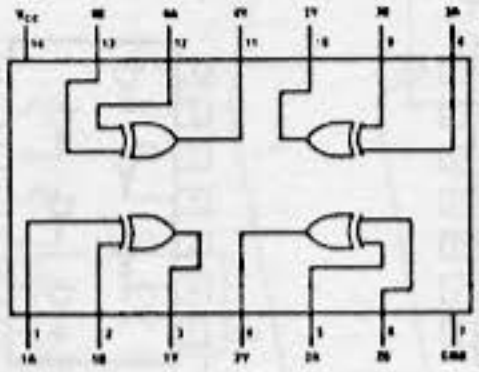


APPENDIX Integrated Circuits used in the H949 Harmonizer

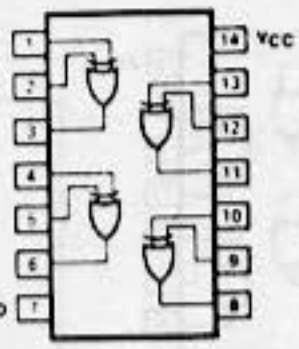
74C10
Triple 3-input
NAND gate



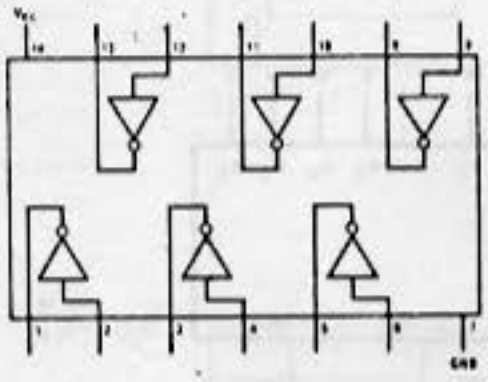
74C86
Quad 2-input
Exclusive-OR gate



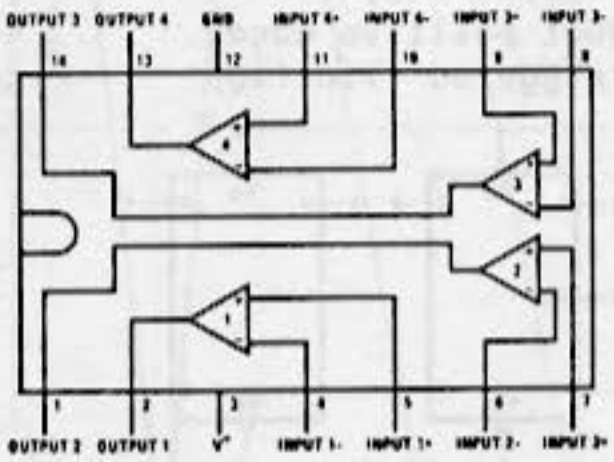
74LS86
Quad 2-input
Exclusive-OR gate



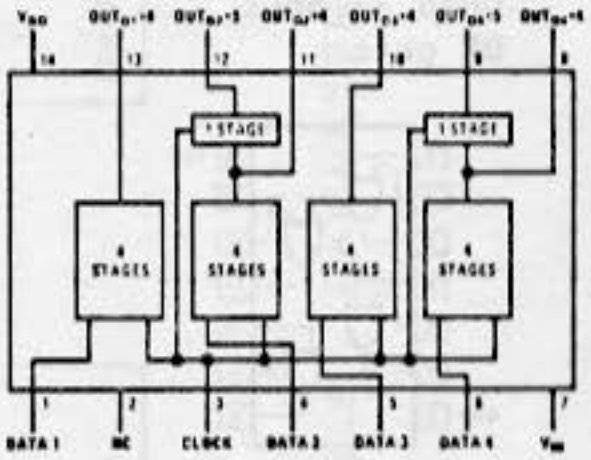
74C901
Hex inverting
TTL buffer



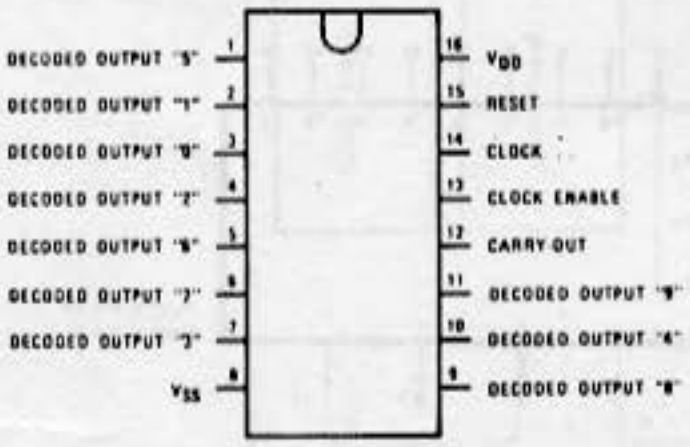
74C909
Quad comparator



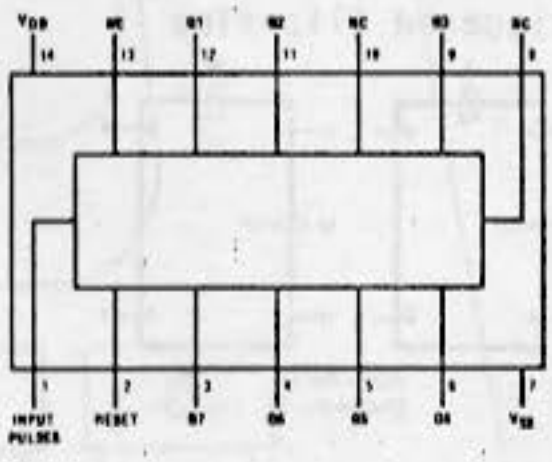
CD4006
18-stage static
shift register



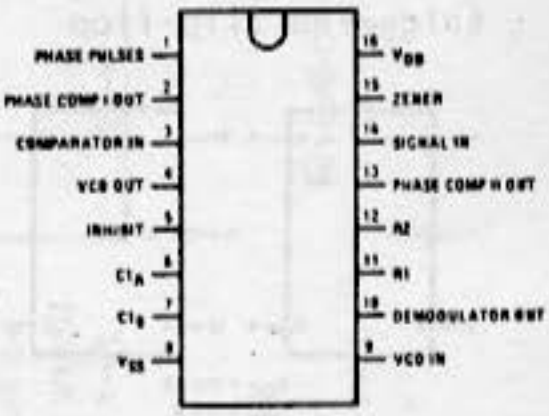
CD4017
Decade counter/divider with
10 decoded outputs



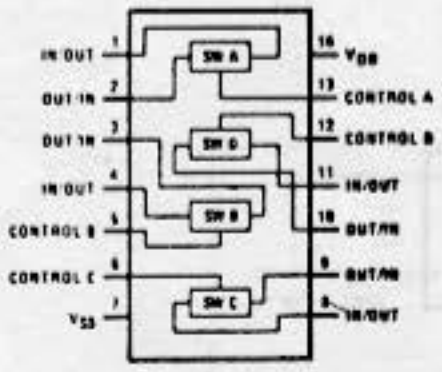
CD4024
7-stage ripple-carry
binary counter/divider



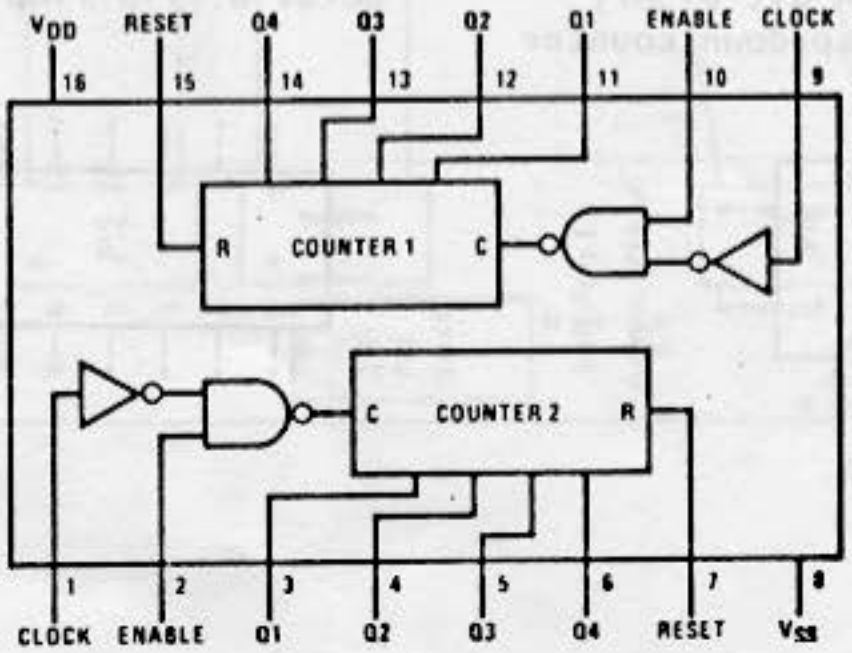
CD4046
Micropower
phase-locked loop



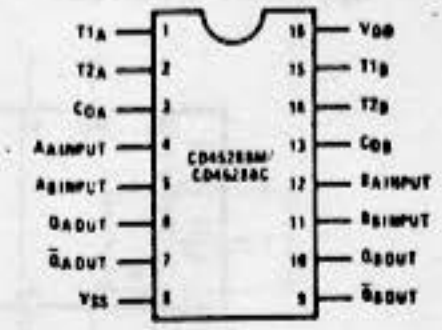
CD4066
Quad bilateral switch



CD4518, MC14518
Dual synchronous up counter



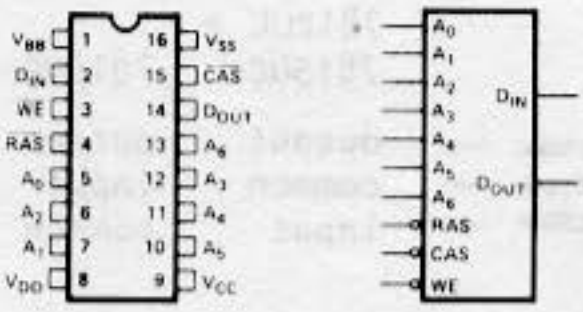
CD4528, MC14528
Dual monostable
multivibrator



Integrated Circuits used in the H949 Harmonizer

16 K Dynamic RAM (various manufacturers and part numbers)

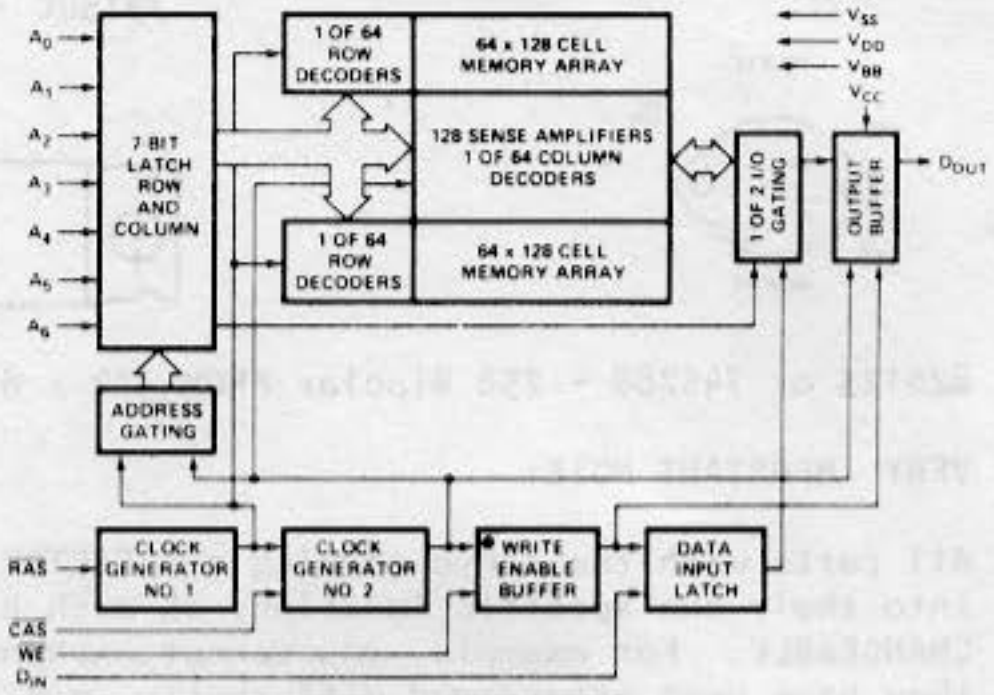
PIN CONFIGURATION **LOGIC SYMBOL**



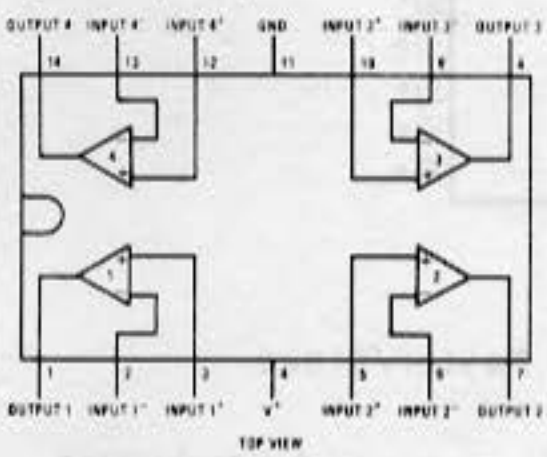
PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

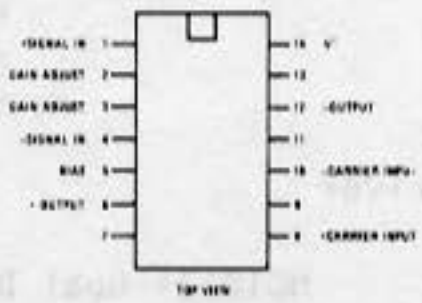
BLOCK DIAGRAM



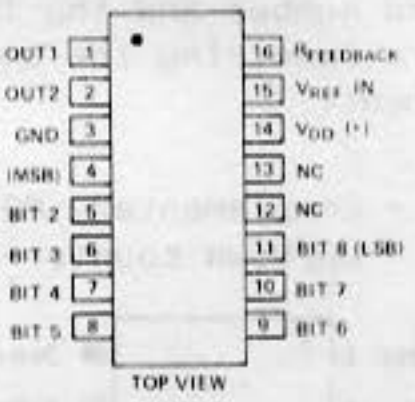
TL064
Quad op amp



LM1496
Balanced modulator-demodulator

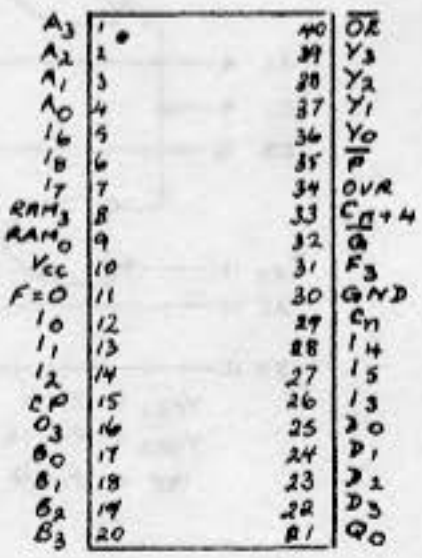


AD7523
8 Bit D/A converter



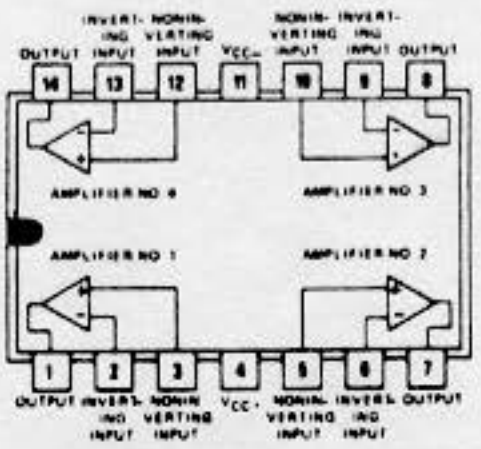
AD7531 - 4-Quadrant Multiplying D/A Converter

AM2901 - Four-bit bipolar micro-processor slice

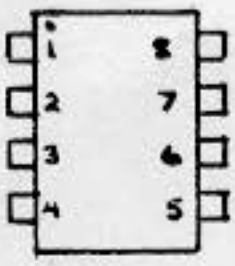


TL081 - JFET-Input Operational Amplifier

TL084 - JFET-Input Quad Operational Amplifier



RC4151 - Voltage to Frequency Converter



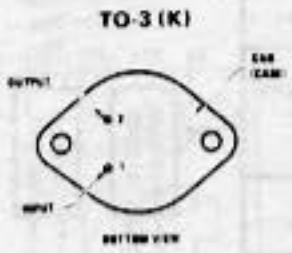
current source
scale factor
logic output
ground

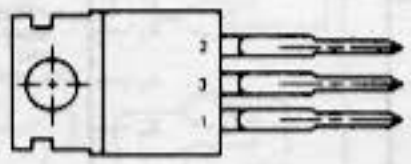
V_{cc}
input voltage
threshold
one shot R,C

Integrated Circuits used in the H949 Harmonizer

LM323 - 3 amp, 5 volt positive regulator

7812UC - 12 volt regulator
7815UC - 15 volt regulator
7915UC - minus 15 volt regulator





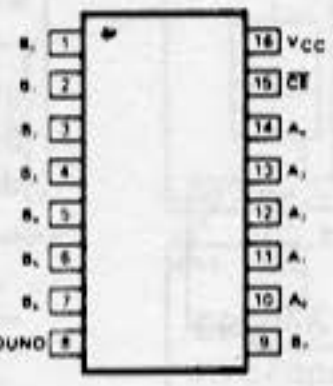
	7812UC + 7815UC	7915UC
2	output	output
3	common	input
1	input	common

82S123 or 74S288 - 256 Bipolar PROM (32 x 8)

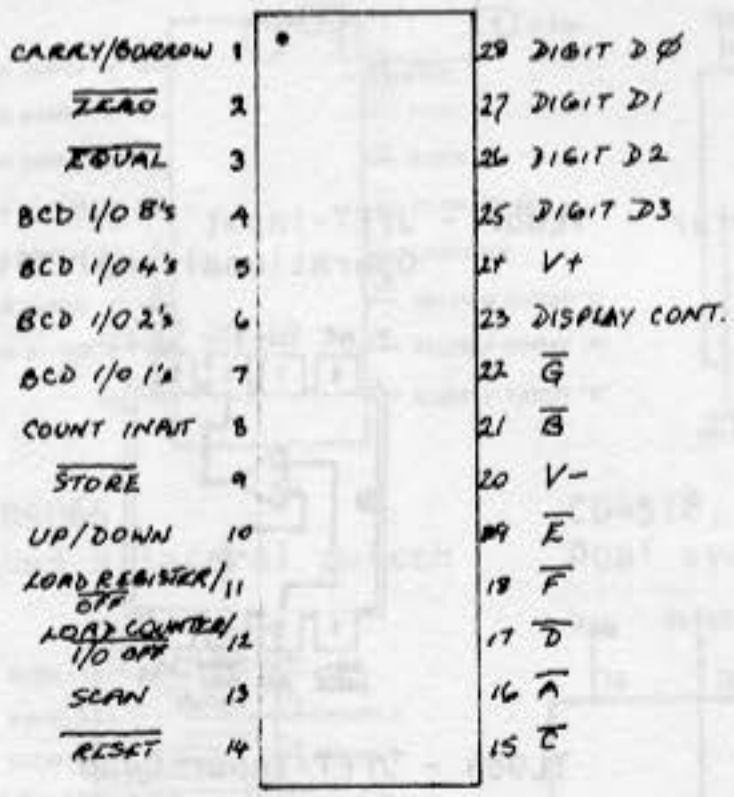
VERY IMPORTANT NOTE:

All parts with the above marking are FACTORY PROGRAMMED, and will fit only into their own specific locations on each circuit board. THEY ARE NOT INTERCHANGEABLE. For example, you cannot exchange IC60 and IC61 on the HD921 board - they have been programmed differently, and their characteristics are completely different.

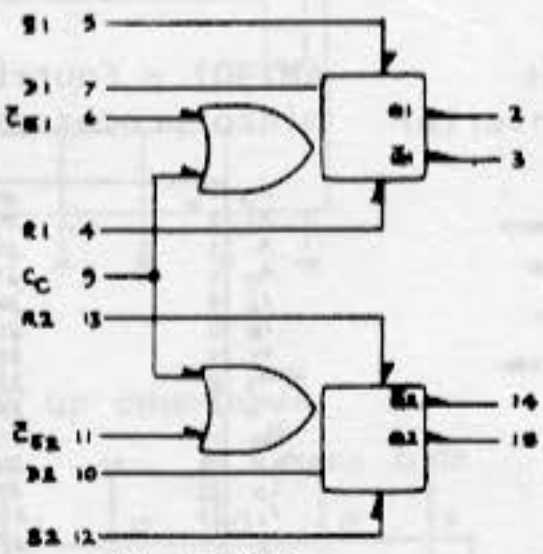
Should you ever need replacements for any of these parts, you must specify the board number and the IC number, to ensure receiving the correct replacement.



ICM7217 - Complementary MOS 4-digit Up/Down counter-decoder-driver



MC10131 Dual D-Type Master/Slave Flip-Flop



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = Don't care
C = $\bar{C}_E + C_C$
A clock H is a clock transition from a low to a high state.