PCM 80

Digital Effects Processor

Service Manual

lexicon

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturer's operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure... voltage that may be sufficient to constitute a risk of shock.

This triangle, which appears on your component, alerts you to important operating and maintenance instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems."

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

Copyright ©1995 Lexicon, Inc.
All Rights Reserved.

Lexicon, Inc.• 100 Beaver Street • Waltham MA • 02154 USA•Tel: 617-736-0300 • Fax: 617- 891-0340

Lexicon Part # 070-10348

Printed in the United States of America

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.

*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when:

the power supply cord or the plug has been damaged,

objects have fallen, or liquid has been spilled into the unit,

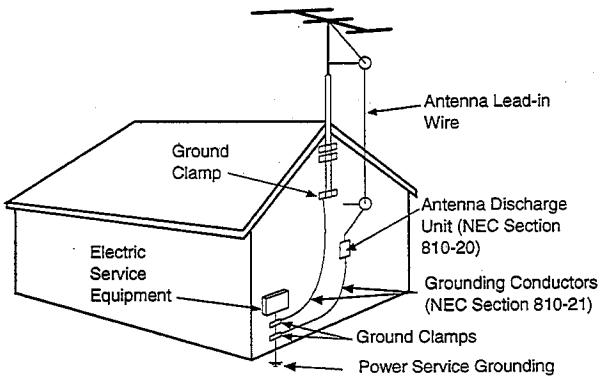
the unit has been exposed to rain,

the unit does not appear to operate normally or exhibits a marked change in performance,

the unit has been dropped, or the enclosure damaged.

Outdoor Antenna Grounding If an outside antenna is connected to the receiver, be sure the antenna system is grounded so as to provide some protection against voltage surges and built-up static charges. Section 810 of the National Electrical Code, ANSI/NFPA No. 70-1984, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna-discharge unit, size of grounding conductors, location of antenna-discharge unit, connection to grounding electrodes, and requirements for the grounding electrode. See figure below.

Power Lines An outside antenna should be located away from power lines.



NEC — National Electrical Code

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

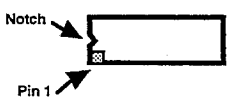
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

Table of Contents

1. Product Overview

Block Diagram 1-1
Front Panel Overview 1-2
Rear Panel Overview 1-3
Installation Notes 1-4
Mounting • Power Requirements • Audio Connections
Control Connections • Setting Audio Levels
Periodic Maintenance 1-7
Ordering parts 1-7
Returning units for service 1-8

2. Specifications

3. Performance Verification

Quick Performance Check 3-1
Analog Audio Performance Check 3-2
Check Signal Levels 3-4
Frequency Response Measurement 3-4
THD+N Measurement 3-5
Signal-to-Noise Ratio 3-5
Digital I/O Test 3-5
Footpedal Functionality 3-6
Footswitch Functionality 3-7
Listening/QC 3-7
Shock Test 3-8
MIDI Functionality 3-9

4. Troubleshooting

Power On Diagnostics 4-1
Error Log and Failure Viewing Mode • Power On Diagnostics
Active Buttons
Power On Diagnostics Test Descriptions 4-7
Troubleshooting 4-16
User Interface Problems• Display Problems • One Bad Channel
Both Channels Bad • No Output
Internal Adjustments and Troubleshooting 4-18
Removing the Top and Bottom Covers • Power Supply
Internal Battery Voltage • System Clocks • Analog Audio
Signal Tracing • Digital Audio Signal Tracing • DAC Adjustment
System Signal Tracing
PCM 80 Extended Memory (SIMM) Installation 4-25
Restoring Factory Settings 4-26

5. Theory of Operation

Architectural Overview 5-1
Block Diagram 5-2
Host Processor Circuitry 5-3
Clocks • Bus Interface • Interrupts
Host Memory 5-6
ROM • Dynamic RAM • Non-Volatile Battery Backed-Up Static
RAM • Battery Backup • PCMCIA Memory Card • Host-to-Slave
Z80/Lexichip Interface • Host-to-DSP56002 Interface
Host I/O 5-11

Contents Cont'd.

Front Panel LEDs 5-12
Switch Status LEDs • Headroom Indicator LEDs • Front Panel Display • Footpedal ADC • Footswitches • MIDI • Analog I/O (Host Control Interface • Digital I/O • System Wordclock Source Selection • Watchdog Timer • System Reset Circuitry +5V Monitor • Reset Delay • Status Bits Summary • Control Bits Summary
DSP Board Circuitry 5-22
Digital I/O 4-22
Digital Audio Transmitter Circuit
Analog Circuitry 5-27
Analog Inputs • Input Amplifier • A/D Conversion • D/A Conversion • Output Filtering • Balanced Output Amplifiers Analog Outputs • Power Supply • Analog Power Distribution Digital Power Distribution
Signal Names 5-31

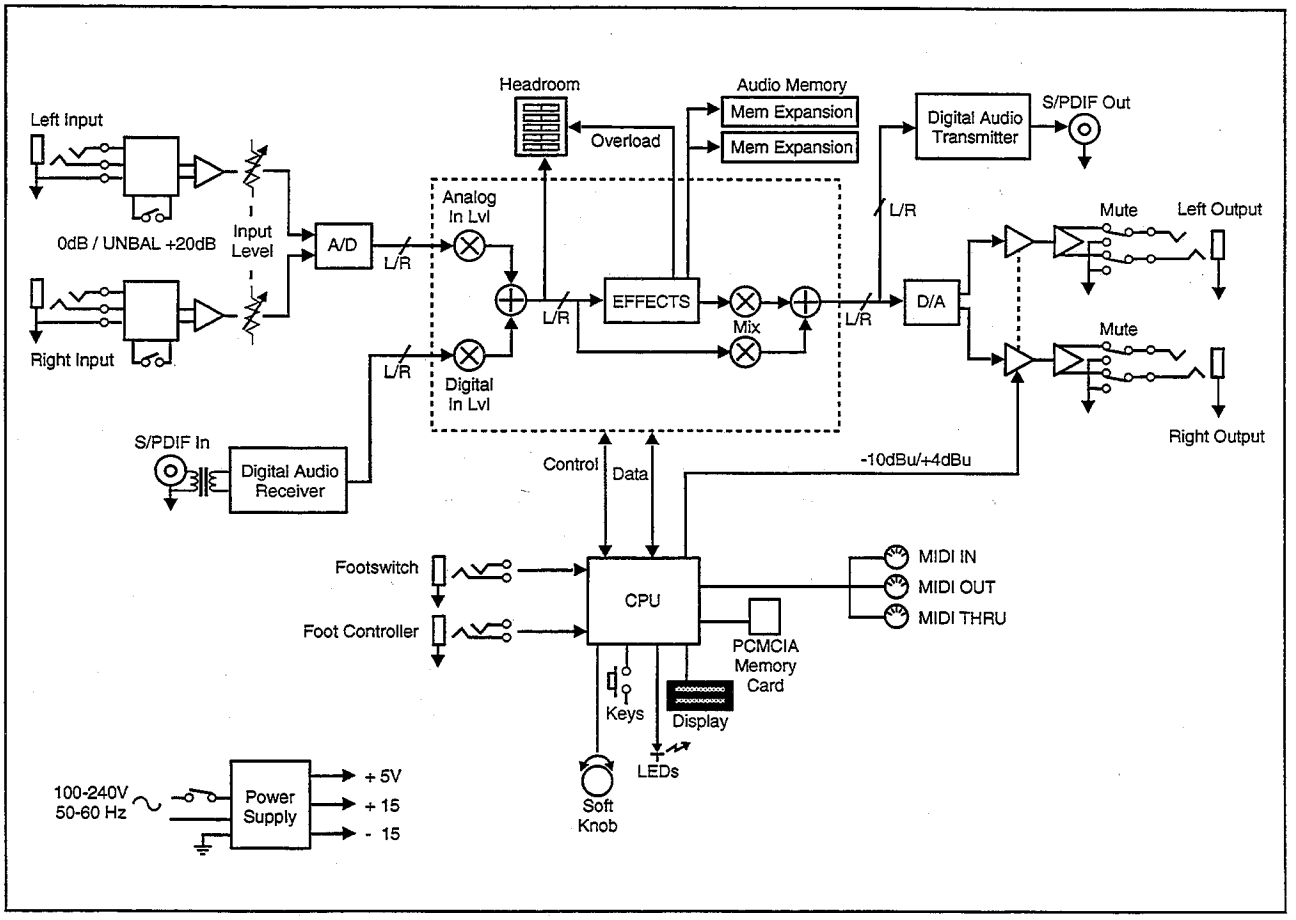
6. Parts List

7. Schematics and Assembly Drawings

1

Product Overview

Block Diagram



The Front Panel

Headroom
5-position indicator for analog and digital signal levels and overload conditions.

INPUT
Adjusts analog input level.

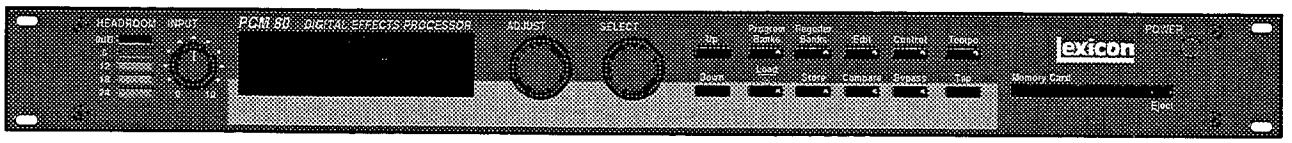
Display
Two rows of 20 alphanumeric characters display effect names and ID numbers, and parameter names and values.

ADJUST
In Edit mode, changes values of parameters chosen with SELECT. With Program Banks or Register Banks selected, behaves as a soft knob for patched parameters.

SELECT
Scrolls through presets, registers or parameters. With Program Bank or Register Bank selected, scrolls through the 50 programs in the selected bank. With Edit selected, scrolls only through the parameters of the active row.

POWER
On/Off.

Memory Card
Slot for optional preset ROM or register RAM cards. Press Eject button to remove card.



Up/Down
Press to move up and down through a program, register, or parameter matrix.

Program Banks
Enables selection of factory presets. Press repeatedly to cycle selection of 4 internal preset banks. Press and hold to display the name of the current bank.

Load/✻
In Program or Register mode, loads the selected program. In Edit mode, scrolls through any multi-field parameter.

Register Banks
Enables selection of user memory. If a RAM card is loaded into the Memory Card slot, each press of this button selects a new register bank. Press and hold to display the name of the current bank.

Store
Initiates register store function.

Edit
Enables parameter selection for editing of values.

Compare
Active in Program, Register, and Edit modes. Press to compare the active version of the current effect with the most recently stored version.

Control
Enables selection of system and global parameters.

Bypass
Bypasses or mutes audio, depending on the setting of each program's bypass parameter.

Tempo
Press to display tempo rate and to initiate tempo functions. LED flashes in time with current tempo rate.

Tap
Sets tempo. Press twice in rhythm to establish tempo rate. Press once to reset LFO.

The Rear Panel

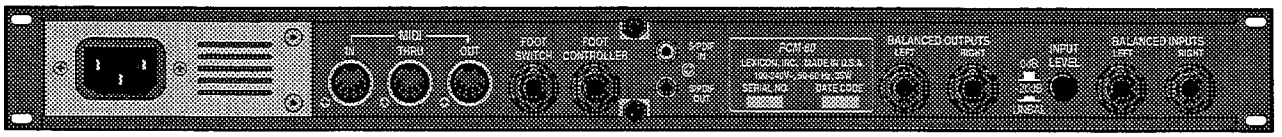
S/PDIF
S/PDIF format digital connectors conform to CP-340 Type II and IEC-958 consumer standards.

Balanced Outputs
Output impedance is 125Ω, each side, balanced, and levels up to +18dBu maximum full scale.

Input Level
2-position (In/Out) switch for matching input gain to the source being used. The In position configures the PCM 80 for unbalanced sources with 20dB of gain. The Out position provides unity (0dB) gain for balanced or unbalanced sources.

Balanced Inputs
1/4" phone connectors, electronically balanced.

Input impedance is 50kΩ unbalanced, and 100kΩ balanced. Inputs accept signal levels from -22dBu to +20dBu.



AC Power
Standard 3-pin IEC power connector. 100-240V, 50-60Hz automatic switching to correct voltage range.

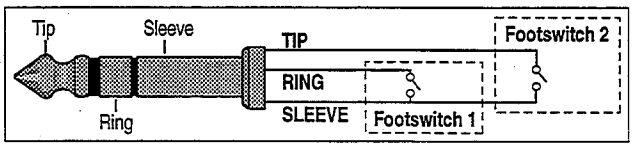
MIDI
IN
Receives MIDI information from other MIDI equipment such as master keyboard controllers, MIDI foot controllers, sequencers and synthesizers.

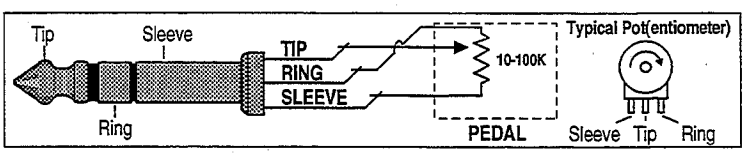
THRU
Passes any MIDI data received without change.

OUT
Transmits MIDI data to other equipment.

Footswitch
1/4" Tip/Ring/Sleeve phone jack for two independent momentary footswitches

Foot Controller
1/4" Tip/Ring/Sleeve phone jack provided for footpedal with 10kΩ to 100kΩ impedance.





Installation Notes

Mounting

The PCM 80 uses one EIA-standard rack space, and can be mounted on any level surface or in a standard 19 inch (483 mm) rack. If the PCM 80 is mounted in a rack or road case, support the rear of the chassis to prevent possible damage from mechanical shock and vibration.

The maximum ambient operating temperature is 104°F (40°C). Provide adequate ventilation if the PCM 80 is mounted in a closed rack with heat-producing equipment such as power amplifiers.

Power Requirements

The PCM 80 is equipped with a 3-pin IEC power connector and detachable cord.

The PCM 80 will operate with power sources from 100 to 240 volts AC, 50-60Hz. Power switching to actual line voltage is automatic.

Audio Connections

Analog Audio

For best performance, maintain balanced connections, and use high-quality, low-capacitance, shielded twisted-pair cable.

When connecting to single-ended, unbalanced devices, connect the low side to signal ground at the unbalanced piece of equipment. Output level does not change when connected to an unbalanced input.

Mono Applications

The PCM 80 senses the number of jacks inserted at the analog inputs and outputs. If a single jack is inserted into either analog input, the input signal is routed equally to left and right effects channels. If one jack is inserted into either analog output, the output signal is automatically summed to mono.

NOTE

Be careful to keep input and output to all channels wired consistently. Out-of-phase wiring can produce audible effects.

Digital Audio

S/PDIF (CP-340 Type II) Consumer Digital Audio I/O. 75Ω coaxial cable, designed for digital audio or video signals is required. Audio grade cable is not necessarily 75Ω and is, therefore, unsuitable. 75Ω video grade cable is generally suitable.

Control Connections

Footswitch/Foot Controller

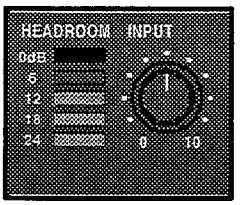
One 1/4 inch T/R/S phone jack is provided for 2 momentary footswitches. Another 1/4 inch T/R/S phone jack is provided for a footpedal (minimum 10kΩ to 100kΩ impedance). Normally open or normally closed momentary switches are suitable. At power on, the PCM 80 assumes the switch is off. Use shielded, twisted-pair cable with shield connected to sleeve. See diagram on previous page.

MIDI

5-pin DIN connectors are provided for MIDI IN, THRU and OUT. Use standard 5-pin DIN MIDI cable assemblies, available from your local dealer.

Setting Audio Levels

The PCM 80, with both analog and digital input and output connections, requires some attention to proper setting of signal level.



Analog inputs are first gain-conditioned by the rear panel input gain switch, and then by the front panel INPUT knob. Proper setting of both the switch and knob are important for best performance of the A/D converter. Audio data from the A/D converter is level adjusted by the Analog Lvl parameter before reaching the effects processors. Digital inputs are also level adjusted before reaching the effects processors via the Digital Lvl parameter.

Analog and digital sources are mixed at the input to the effects processors. For example, setting both Analog Lvl and Digital Lvl to 50% will mix the analog and digital input signals equally and send them to the effects. Creating a mix which exceeds 100% can cause overload.

Proper setting of Input level on the PCM 80 is dependent on:

- Proper setting of the rear panel Input Level switch to avoid signal overload into the analog front end
- Proper adjustment of the signal level into the analog-to-digital converter to optimize noise and avoid overload
- Proper setting of signal level into the digital signal processor to optimize noise.

Headroom Display

The headroom display provides both headroom and overload information from a variety of measurement points. The meters display the sum of both the analog and the digital input data. Examining either the analog or the digital level alone requires that the Level parameter of the subject data stream be set to 100%, while the Level parameter of the other is set to 0%.

The chart below shows the settings of the rear panel Input Level switch. When a choice can be made, it is best to operate at the higher amplitude end of the recommended range to optimize noise performance.

	+20dB Gain	0dB Gain
overload:	> 0dBu	>+20dBu
acceptable:	0dBu to -22dBu	+20dBu to -2dBu
too low (noisy):	<-22dBu	<-2dBu

Overload

The 0db (overload) indicators will light under the following conditions:

- A/D overload
- overload at any point in effects processing

For example, internal peaking of high Q filters, or level buildup from certain reverberation modes can result in overload, even when the input A/D or digital receiver data stream is not at full scale. Such conditions are most often caused by a combination of extreme parameter settings. Adjusting parameter/level settings can eliminate these overload conditions.

Note that incorrect settings of the rear panel Input Level switch can result in analog overload which does not light the overload indicator.

Setting Analog and Digital Input Level

1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.2 Dig In Lvl**, and turn ADJUST to display **0%.**

   NOTE: If you are not running digital audio, controlled by External Clock, into the PCM 80, the digital audio input will be disabled or muted. Until there is valid digital audio input, select **0.0 External** to enable the digital input level control. Until valid digital audio is connected, the **Dig In Lvl** control will remain muted.
4. Turn SELECT to **0.1 Analog In Lvl**, and turn ADJUST to display **100%.**
5. Adjust the front panel INPUT knob so that program material level peaks cause the headroom display to reach the top of the column *without* lighting the overload indicators. An occasional large signal peak causing momentary flashing of the overload indicator is acceptable in most instances, but should be validated by listening to the actual result.
6. If you are running digital audio, turn SELECT back to **0.2 Dig In Lvl**, and turn ADJUST to the desired level. You may want to back off the **Analog In Lvl** setting to prevent the analog/digital mix from overloading the effects processor.

Setting Output Level

While still in Control mode, turn SELECT to **0.6 Output Level**. The Output Level parameter has two range positions. The appropriate position depends on the level handling capability of the device connected to the analog outputs. Devices capable of handling outputs with peak levels of 18dBu require setting **Output Level** to the **+4dBu** setting. Devices which cannot handle peak levels greater than +4dBu require the **-10dBu** setting.

Periodic Maintenance

Under normal conditions the PCM 80 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon, Inc.
100 Beaver Street
Waltham MA 02154
Telephone: 617-736-0300
Fax: 617-788-0499

ATT: Customer Service

Returning units for service

Before returning a unit, for warranty or non-warranty service, consult with Lexicon to determine the extent of the problem, and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return a PCM 80 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, both inside and outside of package

Please enclose a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Service personnel.

2

PCM 80 Specifications

Audio Input	**Connectors:**	1/4 inch T/R/S phone jacks (2)
	Impedance:	0 dB/BAL switch position: 100kΩ, balanced -20 dB/UNBAL switch position: 50kΩ, unbalanced
	Levels:	0 dB/BAL switch position: -2 dBu min for full scale, +20 dBu max -20 dB/UNBAL switch position: -22 dBu min for full scale, 0 dBu max
	CMRR:	0 dB/BAL switch position: 40 dB minimum, 10 Hz to 20 kHz
Audio Output	**Connectors:**	1/4 inch T/R/S phone jacks (2)
	Impedance:	125Ω, each side, balanced
	Levels:	+18 dBm max, full scale (+4 dBu setting) balanced, unbalanced +4 dBm max, full scale (-10 dBu setting)
	Protection:	Relays provided for output muting during power on/off
A/D Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	-65 dB max, 10 Hz to 20 kHz
	S/N Ratio:	100 dB min, 20 kHz bandwidth
	THD:	0.004% max, 10 Hz to 20 kHz
	Dynamic Range:	100 dB min, 20 kHz bandwidth
	Delay:	24 samples (0.54 msec for 44.1 kHz, 0.50 msec for 48 kHz)
D/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	-80 dB max, 10 Hz to 20 kHz
	S/N Ratio:	100 dB min, 20 kHz bandwidth
	THD:	0.006% max, 10 Hz to 20 kHz
	Dynamic Range:	92 dB min (96 dB typ), 20 kHz bandwidth
	Delay:	50 samples (1.13 msec for 44.1 kHz, 1.04 msec for 48 kHz)
A/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	-55 dB max, 10 Hz to 20 kHz
	S/N Ratio:	90 dB min, 20 kHz bandwidth
	THD:	0.008% max, 10 Hz to 20 kHz
	Dynamic Range:	90 dB min, 20 kHz bandwidth

Digital Audio Interface	**Connectors:**	Coaxial, RCA type
	Format:	conforms to S/PDIF CP-340 Type II and IEC-958 consumer standards
	Sample Rates:	44.1 kHz, 48 kHz
Internal Audio Data Paths	**Conversion:**	18 bits
	DSP:	18 to 24 bits
Audio Memory Configuration	**Base memory:**	Two 256k x 18 DRAMs
	User Expansion:	Two SIMM sockets provided for either 1 Meg x 9, 4 Meg x 9 or 16 Meg x 9, 70 nsec DRAM modules
External Memory Card	**Connector:**	Accepts PCMCIA Type I cards, 68 pins
	Standards:	Conforms to PCMCIA 2.0 / JEIDA 4.0
	Card Format:	Supports up to 1MB SRAM (attribute memory not required)
Control Interface	**MIDI:**	5-pin DIN connectors provided for MIDI IN, THRU, & OUT
	Footswitch:	1/4 inch T/R/S phone jack provided for 2 independent momentary footswitches System detects normal-open, or normal-closed on power up
	Foot controller:	1/4 inch T/R/S phone jack provided for footpedal (10kΩ minimum, 100kΩ maximum impedance)
General	**Dimensions:**	19.0"W x 1.75"H x 12.0"D (483 x 45 x 305 mm) 19 inch rack mount standard, 1U high
	Weight:	Net: 6.4 lbs (2.9 kg) Shipping: 9.5 lbs (4.3 kg)
	Power Requirements:	100-240 VAC, 50-60 Hz, 35 W, 3-pin IEC power connector
	RFI/ESD:	Conforms to FCC Class B, EN55022 Class B (CE), IEC 801-2, IEC 801-3
	Environment:	Operating temperature: 32° to 104°F (0° to 40°C) Storage temperature: -22° to 167°F (-30° to 70°C) Humidity: maximum 95% without condensation

Unless otherwise noted, all audio specifications assume rear-panel switch set to BAL, input level control is set for unity gain (0dB), and analog I/O connections wired for balanced configuration.

Specifications subject to change without notice.

3

Performance Verification

Quick Performance Check

This section describes a quick verification of the normal operation of the PCM 80's internal processors and the integrity of the analog and digital audio signal paths. This procedure does not require extensive equipment or removal of the PCM 80 covers.

Diagnostics

When the PCM 80 is powered up, the unit will go through a self-test to verify proper operation of its internal system, and digital signal processors. When proper operation is confirmed, the unit exits the self-test mode and will briefly display the following message:

Lexicon PCM 80
Version n.nn

This message is followed by information on the amount of audio memory installed in the unit, and the final message: **Loading effect...** while the last effect used is loaded to the digital signal processors.

The following series of tests will be run automatically:

Host V40 CPU Test
ROM Checksum Test
Host (V40) SRAM Test
Display Test
Host (V40) Timer/Counter Test
Host (V40) Interrupt Mask Test
56k CPU and DRAM Test
Lexichip DRAM Test
Host (V40) DRAM Test
Battery Test
TACOchip Test

When the unit is powered on, all of the front panel switch LEDs and all of the display pixels are turned on. The display pixels remain on for approximately two seconds, during which time the first three diagnostic tests are run.

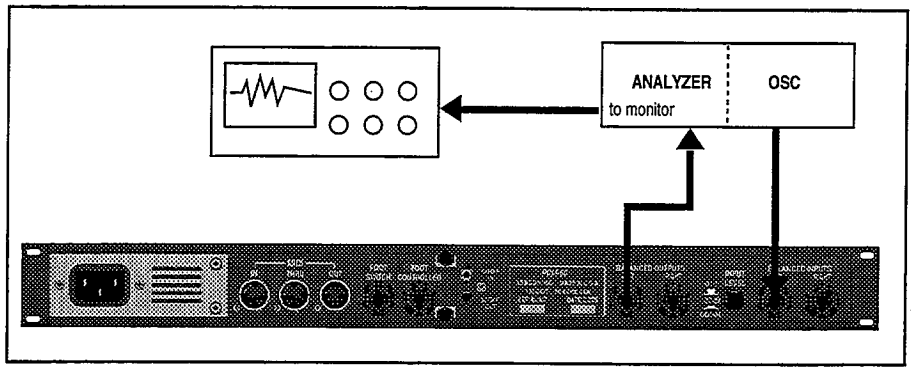
Once the Display Test is complete, and while the rest of the tests are running, the message **Memory Tests** is displayed. If the operator presses the front panel Compare button, or if the 56k DRAM size has been changed, the displayed message will change to **Extended Memory Test** and additional memory tests will be performed. These can take as long as 2 minutes to run when 16M SIMMs are installed. The Extended Memory Test will also be run automatically if the SRAM is cleared.

When all the diagnostics have been executed, all of the headroom LEDs are turned on briefly while the unit is initializing, and **Lexicon PCM 80** appears on the display. Detailed descriptions of the Power On Diagnostics Tests are given in Chapter 4.

Analog Audio Performance Check

Required Equipment

- Low Distortion Oscillator with single-ended or balanced output,<100Ω output impedance, <0,005% THD.
- Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30 kHz high pass filter or audio bandpass (20-20 kHz) filter.
- Oscilloscope
- Audio Input Cable with shield and 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to Low Distortion Oscillator.
- Audio Output Cable with shield and 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to the Distortion Analyzer.
- Two (2) Audio Terminator Plugs, 1/4" with 600Ω-100kΩ resistor between tip and sleeve (single-ended configurations) or tip and ring (balanced configurations). An extra audio cable with a 1/4" connector at one end may be substituted if a termination plug is not available.



Setup

1. **Set Audio Word Clock to 48kHz**
   Turn the unit on and wait for the Power On Diagnostic cycle to finish, and the last used effect to be loaded. Once the effect is loaded, press **Control.** The light on the Control button should be lit, and the display should read:

   Audio *Word Clock
   0.0 Int: 48kHz

   If this display is not shown, simultanously press **Up** and Down to call the display. If the display shows **44.1kHz, turn ADJUST to the left once to select 48kHz**, before running the following tests.

2. **Set Analog In Lvl to 100%.**
   Turn SELECT once to the right to display the Analog Input Level parameter.

   Audio Analog In Lvl
   0.1 100%

   If the percent value is not 100% turn ADJUSTclockwise until 100% is displayed.

3. **Set Output Level to +4dBu.**
   Turn SELECT clockwise to select the Output Level parameter.

   Audio Output Level
   0.6 +4dBu

   If the Output Level is not set to +4dBu, turn ADJUST clockwise until +4dBu is displayed.

4. **Put the PCM 80 into Bypass mode.**
   Press **Down** once. The display should read:

   System Auto Load
   1.6 Off

   Turn SELECT counterclockwise until the following message is displayed:

   System*Bypass Mode
   1.3 InputMute

   Turn ADJUST clockwise until the display reads:

   System*Bypass Mode
   1.3 Bypass

   Press **Bypass on the front panel. T**he LED in the button should light and the display should briefly show the messsage:

   Bypass is on

5. **Connect the audio input cable between the Low Distortion Oscillator and the Left input of the PCM 80 and insert terminator plug.**
   As the PCM 80 automatically routes any audio signal present at either input to both Left and Right inputs, you must insert a terminator plug into the unused input jack to activate only one input channel.

6. **Select balanced or unbalanced input switch.**
   Set the PCM 80 rear panel switch out for input requiring 0dB gain. Push the switch in to test unbalanced input requiring +20dB gain.

7. **Connect the audio output cable between the PCM 80 Left Output and the Distortion Analyzer.**

8. **Insert an audio terminator plug into the PCM 80 Right Output jack.**

Check Signal Levels

1. Apply a 1 kHz sinewave signal to the left input at +20dBu=7.75Vrms for balanced (0dBu=0.775Vrms for unbalanced).

2. Measure the Left output level:
   - Connect the Oscilloscope to the Monitor jack of the Distortion Analyzer.
   - Set the Analyzer to voltmeter mode
   - Turn the PCM 80 front panel Input Level knob up full (completely clockwise). The signal on the oscilloscope will be clipping.
   - Slowly turn the Input Level knob counterclockwise until the signal is just below clipping. Note this setting as you will be reminded to return to it in the following tests.

3. Switch the Distortion Analyzer back to level and read the Left output measurement. Acceptable levels are between +18.5 and +21.5dBu.

4. On the PCM 80, press **Control** then turn SELECT to display **Output Level**. Turn ADJUST to display **-10dBu**.

5. Measure the Left output again on the Distortion Analyzer. The reading should be between 7.5 and 4.5dBu .

6. Swap the I/O and terminator connectors, reset the PCM 80 **Audio Output Level** to **+4dBu** , and repeat steps 2-5 for the right output .

Frequency Response Measurement

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 80. Turn the PCM 80 front panel Input Level to the position established as being just under clipping .

2. Measure the right output and set the Analyzer for 0dBu reference.

3. Turn off all filters on the Analyzer.

4. Sweep the Oscillator from 10Hz to 20kHz.

5. The right output should vary less than ±0.5dB, referenced to the 1kHz output level.

6. Swap the I/O and terminator connectors and repeat steps 1-5 for the left output.

THD+N Measurement

1. Apply a 1kHz +20dBu sinewave signal to the left input of the PCM 80. On the Analyzer the only filter used should be in the range of 20Hz to 20kHz of audio bandpass, or 30kHz low pass filters can be used.Turn the PCM 80 front panel Input Level to the position established as being just before clipping .

2. Set the PCM 80 **Audio Output Level** to **+4dBu.**

3. Measure the Left output THD+Noise level on the Analyzer, for a reading of <0.008 %

4. Swap the I/O and terminator connectors on both inputs and outputs and measure THD+Noise level for the right output <0.008 %

Signal To Noise Ratio

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 80. Turn the PCM 80 front panel Input Level to the position established as being just before clipping .

2. Set Analyzer to dB Ratio and zero it for a reference level. Turn off the oscillator output and measure the right output. The reading should be greater than a 90dB ratio.

3. Swap the I/O and terminator connectors and repeat on the left output.

Digital I/O Test

There are several ways to test the Digital I/O. The first is with the Diagnostic Memory Card which has a built in Digital I/O test. This card is available with complete instructions from Lexicon Customer Service. The second method, described below, requires a second PCM 80.

1. Place the two PCM 80s one on top of the other. Connect power to each, and turn both on.

2. Attach an RCA wire connector between the PCM 80 S/PDIF output of the unit you are testing, and the S/PDIF input of the reference PCM 80.

3. On the PCM 80 under test, Press **Control** and turn SELECT to display:

   Audio*Word Clock
   0.0 Int: 48kHz

   This sets the PCM 80 under test to *send* Word clock.

4. On the reference PCM 80. press **Control** and use SELECT to display the same screen. Turn ADJUST one position to the left. This PCM 80 should automatically lock onto the clock from the PCM 80 under test and display the following:

   Audio*Word Clock
   0.0 Ext: Cns 48kHz

If this test fails, the display will read:

Audio*Word Clock
0.0 Ext: Cns Not Locked

5. Set the reference PCM 80 to send Word clock at **44.1kHz**. The receiving PCM 80 should change to show:

   Error: Lock
   (Press any button)

   Press any button on the front panel. The display will show the last clock value read. To have it read the new 44.1kHz clock, turn ADJUST to the left one position. The unit should automatically lock to the 44.1 kHz rate, and display:

   Audio*Word Clock
   0.0 Ext: Cns 44.1kHz

6. To test the PCM 80 for *receiving*, reverse the RCA cables and repeat steps 2-5, using the reference PCM 80 as the signal source, and the PCM 80 being tested as the receiver.

Footpedal Functionality

Before performing this test, press **Control**. Use **Up** and **Down** and SELECT to locate matrix position **1.0 Edit Mode**. Use ADJUST to set the mode to **Pro**.

1. Connect a footpedal to the PCM 80 rear panel Foot Controller connector.
2. Press **Program Banks** repeatedly to display Program Bank 2 (**P2**).
3. Turn ADJUST to select **4.0 Pedal Swell**.
4. Press **Load/*** to load the program.
5. Press **Edit**, then use **Up** and **Down** and SELECT to locate matrix position **0.2 InLvl L**.
6. Slowly depress the footpedal and verify that the parameter smoothly changes from **Off**, to **-85dB**, up to **–2dB** and, finally, to **0dB**.

Footswitch Functionality

1. Connect a dual footswitch with a 1/4" tip-ring-sleeve plug into the PCM 80 rear panel Foot Switch connector. These tests can also be done with a single footswitch with a mono 1/4" tip-sleeve plug inserted half-way in to test Foot Switch 1, then inserted completely to test Footswitch 2.
2. Press **Control**. Use **Up** and **Down** and SELECT to locate matrix position **1.3 * Bypass Mode**.
3. Press **Load/*** to display the parameter **Bypass Src**.
4. Use ADJUST to select **Foot Sw 1**.
5. Press the first footswitch. The Bypass light should toggle from off to on, or on to off.
6. Use ADJUST to select **Foot Sw 2**.
7. Press the second footswitch. The Bypass light should toggle from off to on, or from on to off.

After finishing this test, use ADJUST to select **Off** (and leave Bypass in its Off default state).

Listening/Q.C.

Required Equipment

- Clean, antistatic, well lighted work area
- Low Distortion sine wave oscillator
- Headphone Amplifier
- (4) 1/4" to 1/4" stereo phone plug cable (3 ft. minimum)
- Two 1/4" female to 1/4" male Y-adapter cables
- Stereo Headphones

Setup

1. Use two audio cables and a Y-adapter to connect the output of a low distortion sine wave oscillator to the left and right audio inputs of the PCM 80.
2. Use 2 cables to connect the headphone amp inputs to the PCM outputs.
3. Set the oscillator to 220Hz at –45dBV.
4. Turn the volume control on the headphone amplifier all the way to minimum (fully counterclockwise) and plug in the headphones.
5. Set the Input Level switch on the rear panel of the PCM 80 to the IN position (-20dB).
6. Power up the PCM 80. Press **Program Banks** repeatedly to select Program Bank 0 (**P0**).
7. Turn the SELECT knob clockwise to display:

   ConcertHallP0 1.9

   ***ADJUpMyEchos**

8. Press **Load/***. (Make sure **Bypass** is OFF.)

Verify Clean Audio

1. Put the headphones on.
2. Set the PCM 80 INPUT control fully clockwise.
3. Slowly increase the volume on the headphone amplifier until it's at a comfortable listening level.
4. Adjust INPUT over its entire range.
5. Verify that no pops, clicks or scratchiness are heard when turning the pot.
6. Adjust PCM 80 INPUT so the peak level just turns on the –6dB (yellow) headroom LED.
7. Adjust the volume on the headphone amplifier to a comfortable listening level.
8. Mute and unmute the signal source at different frequencies. Carefully listen to the outputs for grossly unusual noise, audible distortion or other gross audio irregularities through entire decay time of the reverb.

Shock Test

1. Lift each corner of PCM 80 four inches off of the workbench and drop.
2. Verify that no audio or display intermiitents are caused by this action.

KEEP ONE CORNER OF UNIT TOUCHING THE BENCH AT ALL TIMES TO PREVENT DAMAGE TO THE UNIT

MIDI Functionality

The following is a quick test of MIDI functionality. A more thorough test is included on the Lexicon Memory Diagnostics Card (described in Chapter 4). The following test requires a second PCM 80. You may want to record the parameter values changed during the test so that they can be restored when the test is completed.

1. Power up both PCM 80s and load **P0 0.0 Prime Blue** on each unit. (Press **Programs Banks** repeatedly until **P0** is displayed. Turn SELECT to display **P0**, then press **Load/✱**.)
2. Connect a MIDI cable between MIDI OUT on the reference PCM 80 and MIDI IN on the PCM 80 under test.
3. On each unit:
   a. Press **Control** and use **Up** and **Down** and SELECT to locate matrix position **3.1 MIDI Receive**. Turn ADJUST to select **1**.
   b. Turn SELECT to locate matrix position **3.2 Transmit**. Turn ADJUST to select **1**.
   c. Turn SELECT to locate matrix position **3.4 Pgm Change**. If **MIDI Automation** is not displayed, press **Load/✱** until it appears. Turn ADJUST to select **On**.
   d. Press **Load/✱** to display **MIDI Target ID**. Turn ADJUST to select **All**.
   e. Turn SELECT to locate matrix postion **3.7 SysEx**. If **MIDI SysEx Receive** is not displayed, press **Load/✱** repeatedly until it appears. Turn ADJUST to select **On**.
   f. Press **Load/✱** to display **MIDI SysEx Device ID**. Turn ADJUST to select **0** (the default setting).
   g. Press **Edit** to enter the edit matrix. Use **Up** and **Down** and SELECT to locate matrix position **S.0 Controls Mix**.4.
4. On the reference PCM 80, use ADJUST to slowly increase the parameter from 0-100%. The **Controls Mix** parameter on the PCM 80 under test should track the reference PCM 80 as you turn ADJUST.

This completes testing of MIDI input to the unit under test. Swap the MIDI IN and OUT connections and repeat step 4 to test MIDI output.

MIDI THRU can be tested by verifying the transfer of MIDI data from any device's MIDI OUT to the PCM 80 MIDI THRU, then to any device's MIDI IN. Two MIDI devices with a PCM 80 connected between them, or three PCM 80s can be used for this.

4

Troubleshooting

Power On Diagnostics*

When the PCM 80 is powered up, the unit will go through a self-test to verify proper operation of its internal system, and digital signal processors. When proper operation is confirmed, the unit exits the self-test mode and will briefly display the following message:

Lexicon PCM 80
Version n.nn

This message is followed by information on the amount of audio memory installed in the unit, and the final message: **Loading effect...** while the last effect used is loaded to the digital signal processors.

Following is a list of the Power On Diagnostic Tests in the order in which they are executed. Each test is identified by a code number which is used to identify tests in the failure log.

Test	ID #
Host V40 CPU Test	01
ROM Checksum Test	02
Host (V40) SRAM Test	03
Display Test	04
Host (V40) Timer/Counter Test	05
Host (V40) Interrupt Mask Test	06
56k CPU and DRAM Test	07
Lexichip DRAM Test	08
Host (V40) DRAM Test	09
Battery Test	0AH
TACOchip Test	0BH

An additional test number (FFH), is used to indicate a problem in the link between the Host and the Z80 bus when the Z80 CPU tries to load code from the Slave RAM to the Lexichip.

The 56k DRAM, Lexichip DRAM test, and Host DRAM tests are executed simultaneously by the independent CPUs to shorten the total Power On Tests execution time.

When the unit is powered on, all of the front panel switch LEDs and all of the display pixels are turned on. The display pixels remain on for approximately two seconds, during which time the first three diagnostic tests are run.

Once the Display Test is complete, and while the rest of the tests are running, the message **Memory Tests** is displayed. If the operator presses the front panel

* PCM 80 software contains two types of diagnostics: Power On Diagnostics and Memory Card Diagnostics. This section describes the Power On Diagnostics which are executed automatically each time the PCM 80 is turned on. Memory Card Diagnostics require the PCM-80 Diagnostic Memory Card (Lexicon Part No. 750-10271) which is available from Lexicon Customer Service with complete documentation.

Compare button, or if the 56k DRAM size has been changed, the displayed message will change to **Extended Memory Test** and additional memory tests will be performed. These can take as long as 2 minutes to run when 16M SIMMs are installed. The Extended Memory Test will also be run automatically if the SRAM is cleared.

Before each Diagnostic test is executed, the Test ID# is displayed on the headroom LEDs. This display remains while the test is running, and can be used to identify the failed test in the event that the unit hangs or crashes during the test. See Diagnostic Fa*ilures*.

When all the diagnostics have been executed, all of the headroom LEDs are turned on briefly while the unit is initializing, and **Lexicon PCM-80** appears on the display.

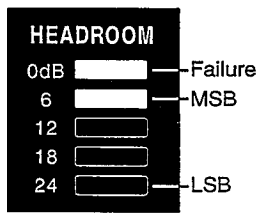
Diagnostic Failures

Errors which occur during the Power On Diagnostic Tests are available in an error log file. When a failure occurs during the test sequence, the red 0dB LED will light and a binary test/error code will be displayed on the LEDs. An **E** and the test ID# will also appear on the front panel display to indicate which test failed. Information about the failure will be stored in an error log file in the SRAM for future analysis. The LED code is a 4-bit binary number displayed on both headroom columns with the -24 dB LED as the LSB, and the yellow -6 dB as the MSB.

The figure below shows an example of the LED binary failure code indicating that the Lexichip Power On DRAM Test failed. In this case, the front panel display would additionally display E8. (Memory Card diagnostic test failures are not reported on the headroom LEDs.)

Failure of any test will stop the Power On Diagnostic Tests sequence. When a failure occurs, the operator has the following options:

1. Power cycle the unit and see if the Power On Diagnostics pass on restart.
2. If the failure occurred during the CPU, ROM and SRAM tests, press **Down** to enter a special diagnostic test loop in which 1's and 0's are walked through



Binary Code 8 (1000)

the Address and Data bus.

3. If any test but the CPU test failed, press **Load** to execute the next test. Although you can step through all of the tests by continuing to press **Load** after each test, the unit will not become operational at the end of the sequence. (Once **Load** is pressed, you can enter a special error log viewing mode — See *Error Log and Failure Viewing Mode*.)
4. If you have a Diagnostic Memory Card, inserting it, power cycling the PCM

80, then pressing **Control** and **Tempo** simultaneously will initiate Functional Diagnostic Tests.

NOTE: If a failure occurs during the CPU test, the failure will not be stored in the error log. Failures that occur during the ROM and SRAM test will not be stored unless **Load** is pressed and the test cycle is allowed to progress beyond the SRAM test. Data may not be stored, or the unit may crash, depending on the seriousness of the problem.

Bypassing Diagnostic Failure Lockup

If problems arise during the power-on cycle, the unit will not boot into the main system. The message **Diagnostic Failure Occurred** will be displayed if Load is pressed when the failure occurs.

There are two options for bypassing system lockup: entering card diagnostics, or simply bypassing the diagnostics and continuing the boot cycle. **Bypassing error messages with either method can result in excessive speaker excursion, and/or lost user register data.** Of the two options, entering card diagnostics involves less risk of loss of user registers than does bypassing diagnostics altogether.

You can enter the card diagnostics by simultaneously pressing **Control** and **Tempo. The message: PCM-80 Diagnostics SELECT Test** will be displayed if a diagnostic card is plugged in to the card slot. If a diagnostic card is not installed, the message: **Insert Diagnostic Card** will appear. Simultaneously press **Control** and **Tempo** when this message appears to enter the Error Log Failure Viewing Mode.

To completely bypass a diagnostic failure, simultaneously press Up and Tempo when the failure occurs. The message: WARNING! Do not continue will be displayed. Simultaneously press **Down** and **Tap** to bypass the failure message and continue the boot sequence.

Error Log and Failure Viewing Mode

All failures that occur are stored in a 20 record ring buffer (First In First Out) called the Error Log File. Each record consists of 5 elements:

1. Test number, which indicates which test failed. For example, the number 09 means that the Host V40 DRAM Test failed. Test number 00 indicates no failure.
2. Tested value. As an example, in the case of a Host DRAM Test failure, this data could be 000000AA — a pattern written by the CPU to the DRAM. A value of 00000000 may indicate that the CPU tried writing all zeros to the DRAM or it could mean that this value is not applicable for the type of failure that occurred (such as timeout failure).
3. Failed value. As an example, in the case of a Host DRAM Test failure this data could be 0000002A, indicating a problem with bit 7 on the Host Data Bus, or perhaps a cold solder connection on the DRAM. A value of 00000000 may indicate that this value is not applicable for the type of failure that occurred (such as timeout failure).
4. Address/location where failure occurred. In case of the Host DRAM Test

failure, the address could be 00000000 which is where the DRAM is located. (00000000 could also mean that this value is not applicable for the type of failure that occurred.)

5. Type of failure. This value indicates which type of failure occurred. For example, in the Host DRAM Test, 01 indicates data failure.

Simultaneously press **Control** and **Tempo** to enter Failure Viewing mode, where as many as 20 failure codes are listed (most recent first). A single failure record is shown below:

Use **Up** or **Down** to display all of the failures. Press **Load** to exit.

Remember that the unit suspends operation when CPU failures occur, and CPU failures are, therefore, never stored. ROM and SRAM failure information is not stored unless the SRAM test has been completed and Load has been pressed in repsonse to the ROM and/or SRAM failure message.

	#	=	Test number (00 indicates cleared error record)
	X	=	Tested value (e.g. data written to RAM)
	Y	=	Failed value (e.g. data read back from RAM)
	A	=	Address where failure occurred
	T	=	Describes failure type:
(0)	00H	=	Unknown / No failure.
(1)	01H	=	Data failure (e.g. failure happened during RAM Data test).
(2)	02H	=	Address failure (e.g. failure happened during RAM Address test).
(3)	03H	=	Timeout failure (Occurs if there is no response from the co-processor or if test is taking to long).
(4)	04H	=	No RAM size information available.
(5)	05H	=	Wrong RAM size.
(6)	06H	=	Data transfer failure to the 56k.
(7)	07H	=	Fatal 56k failure. 56k is not there or there are bus problems.
(8)	08H	=	CPU failure.
(9)	09H	=	Slave Z80 loading the Lexichip WCS failed.
(10)	0AH	=	Data transfer to Slave Z80 SRAM failure.
(11)	0BH	=	56k PLL failure. If the 56k Phase Locked Loop doesn't work the Slave Z80 will not be operational.
(12)	0CH	=	MIDI Test timeout failure, Transmit buffer didn't get emptied.*
(13)	0DH	=	MIDI Test timeout failure, Receive buffer didn't get filled.*
(14)	0EH	=	MIDI Test data transfer error detected by the Serial Control Unit.*
(15)	0FH	=	MIDI Test transmitted data vs. received data mismatched.*
(16)	10H	=	MIDI Test Transmit interrupt failed.*
(17)	11H	=	MIDI Test Receive interrupt failed.*
(18)	12H	=	PCMCIA Card Test, No card installed.*
(19)	13H	=	PCMCIA Card Test, Write Protect is on.*
(20)	14H	=	PCMCIA Card Test, Backup battery voltage is too low.*
(21)	15H	=	PCMCIA Card Test, Bank switching failed.*
(22)	16H	=	PCMCIA Card Test, Attribute register failed.*
(23)	17H	=	PCMCIA Card Test, Transferring code from card to DRAM failed.*
(24)	18H	=	Foot Controller ADC Test failed (Requires special test fixture).*
(25)	19H	=	Watchdog Timer Test failed, timed-out too soon.*
(26)	1AH	=	Watchdog Timer Test failed, failed to time-out.*
(27)	1BH	=	56k Data Window Address Register Test failed.
(28)	1CH	=	Stack failure during Watchdog Timer Test (Software related).

(29)	1DH	=	The Z80 did not initialize the mailbox. It has probably crashed.*
(30)	1EH	=	48 kHz Word Clock frequency is too high.*
(31)	1FH	=	48 kHz Word Clock frequency is too low.*
(32)	20H	=	44.1 kHz Word Clock frequency is too high.*
(33)	21H	=	44.1 kHz Word Clock frequency is too low.*
(34)	22H	=	56k did not boot
(35)	23H	=	DMA data transfer from V40 Host to 56k DSP timed out*
(36)	24H	=	DMA data transfer from 56k DSP to V40 Host timed out*
(37)	25H	=	Data mismatch in data transferred to 56k DSP, then back to V40 Host*
(38)	26H	=	56k did not complete data transfer*
(39)	27H	=	Digital audio receiver is locking to an illegal data stream*
(40)	28H	=	Digital audio receiver is detecting Word Clock frequency outside 48kHz*
(41)	29H	=	Digital audio receiver is detecting Word Clock frequency outside of 44.1kHz*
(42)	2AH	=	Digital audio receiver is detecting Professional instead of Consumer audio*
(64)	40H	=	Digital audio receiver detected some error when ERF signal set high*
(65)	41H	=	Digital audio receiver has detected Validity error*
(66)	42H	=	Digital audio receiver has detected Confidence error*
(67)	43H	=	Digital audio receiver has detected Slip Sample error*
(68)	44H	=	Digital audio receiver has detected CRC error (not applicable to PCM 80)*
(69)	45H	=	Digital audio receiver has detected Parity error*
(70)	46H	=	Digital audio receiver has detected Bi-Phase error*
(71)	47H	=	Digital audio receiver has detected No Lock error*

Failure indications marked with an * are created by tests residing in the Diagnostic card. Note that the failure codes are different for the Host (V40) Timer/Counter Test.

Power On Diagnostics Active Buttons

During the Power On test sequence, the front panel buttons will be scanned. The buttons must be pressed when power is turned on, until all the front panel display pixels are turned off.

Push Button Combination:	**Action Taken**
Up and **Bypass**:	Bypasses some of the diagnostics and speeds up the boot cycle.
Compare	Initiates extensive 56k-, Lexichip- and Host DRAM test. (This test can take up to 2 minutes depending on the size of the installed DRAM). If the 56k DRAM size is changed, the change will be detected and the 56k extensive test will be initiated automatically at the time the unit is first turned on. The message: **Extended DRAM test** is displayed during the test.
Up and **Control**	The unit will loop the Power On Diagnostics until the unit is powered off.
Control and **Tempo**	Will activate the card diagnostics if the diagnostic card is installed. If no diagnostic card is installed and these buttons are pressed again in response to the message: **Insert Diagnostic Card**, a special mode that displays the error log

will be entered. Pressing **Up** or **Down** will scroll through the failure records. Upon entry into this mode, the most recent failure is displayed. Press **Load** to exit.

Pressing these buttons when ROM- or SRAM test failure occurs will activate the card diagnostics if the diagnostic card is installed. WARNING! Depending on the seriousness of the failure, data stored in the registers could be lost if the operator decides to ignore the failure message and continue. In order for the card diagnostics to work, certain parts of the system have to be working. (V40-CPU, ROM, SRAM, Host DRAM, and card interface.)

These buttons can also be pressed when the Diagnostic Failure **Occurred** message is displayed to enter the Diagnostics.

Up and **Tempo** Can be pressed when the **Diagnostic Failure Occurred** message is displayed and the operator wishes to ignore the error message. For more detail, see above description.

WARNING! Bypassing this error message is not recommended. If the operator wishes to enter the diagnostics or look at the failure log, **Control** and **Tempo** can be pressed (see button sequence description above).

Load If diagnostic failure occurs and **Load** is pressed, the failure is ignored and the boot cycle will continue.

Down This button is only active when the V40-CPU, ROM- and/or SRAM tests fail. Pressing it will activate a special test that keeps the Host Data and Address bus active.

Down and **Tap** Initialize PCM-80 to factory settings.

WARNING! This action erases the user setup and the diagnostic failure log by clearing the memory (SRAM). The message: **WARNING! Press STORE to clear the SRAM** is displayed. The memory is cleared by pressing **Store**. The message: **SRAM Cleared press any button to cont.** is displayed. Press any button and the unit reboots. If any button other than **Store** is pressed, **SRAM clear cancelled** is briefly displayed and the boot cycle will continue without clearing the memory.

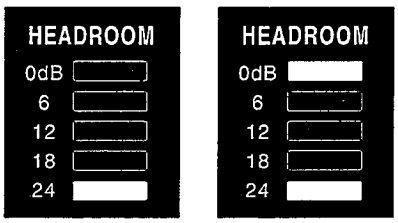
Power On Diagnostics Test Descriptions

Host V40 CPU Test (1)

This test verifies any stuck CPU register bits. The V40 Host processor (U46) tries to pass the value 55AAH through its internal registers. In second pass, the data is inverted to AA55H and passed through the registers. If an error is detected, an attempt is made to write an error code to the front panel headroom LEDs and the boot cycle will be halted.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code.

If a CPU error occurs, the operator has the option of pressing **Down** to enter the test loop. Besides reading data from the ROM, the V40 writes a walking "1" value to location "0000H" in the SRAM. (Mapped to B0000H.) By using an oscilloscope and triggering on the HMWR/ pulse, you can verify that all the data lines are



Host V40 CPU Test Host V40 CPU Test Failure

connected to all the devices and that there are no shorts. If there is a problem with the data bus and/or the address bus between the V40 CPU and the ROM, the unit will not boot at all. An additional walking "1" test on the address bus is performed by rotating a "1" through the 20-bit address bus by reading data from the entire address space If the CPU registers used by this test are broken, the test will not work as intended.

A CPU error is a serious problem. The program will not be able to proceed from here to the diagnostic system and may not even reach the test loop. The only way to exit the test loop is by power cycling the unit.

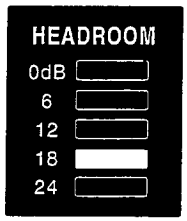
No failure log is generated.

ROM Checksum Test (2)
The ROM checksum, which is a byte size value, is located as the last byte in the ROM (U39). The test adds up the entire ROM including the Checksum byte. The result should be zero (8 bit value.)

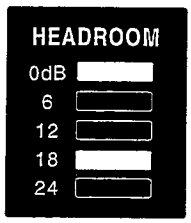
Before the test is executed, the following binary code will be put out on the

Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code, and an attempt is made to write E2 to the front panel display.

If a ROM checksum error occurs, you can press **Load**, simultaneously press **Control** and **Tempo**, or to press **Down**. If **Load** is pressed, the failure is ignored and the next test will be executed. The failure will not be stored until just before



ROM Checksum Test



ROM Checksum Test Failure

the Display Test is executed.

Pressing **Control** and **Tempo** invokes the Card Diagnostics.

Note: There is a risk in doing this if there is a ROM problem, as the diagnostic system may not function and the user registers may be destroyed.

If a diagnostic card is not inserted pressing **Control** and **Tempo** again invokes the Failure Viewing Mode.

Pressing **Down** causes the CPU to start executing the same test loop as described in the CPU test. The unit has to be power cycled to exit the test loop.

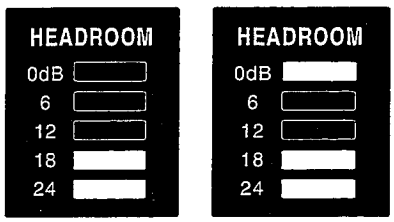
Failure log	
Test number	: 2
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: N/A

Host (V40) SRAM Test (3)
This SRAM test does not touch the volatile SRAM area (where register and other system information is stored). It does nondestructive testing in the first 4k of the SRAM (U38). The nondestructive test reads one location and stores it in a CPU register. Then, it performs a marching "1" test on that location followed by a marching "0" test on the same location. The test location is incremented by one

until the end of the diagnostic SRAM area is reached. Since the SRAM is used as a temporary stack until the DRAM has been tested, a destructive counting test is done on the area where the temporary stack is located (approx. the first 200H bytes). This will ensure address independence in the temporary stack area.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and an attempt is made to write E3 to the front panel display.

If a Host SRAM failure occurs, you can press **Load**, simultaneously press **Control** and **Tempo** or press **Down**.



Host V40 SRAM Test | Host V40 SRAM Test Failure

If **Load** is pressed the failure is ignored and the next test will be executed. The failure will not be stored until just before the Display Test is executed.

Pressing **Control** and **Tempo** invokes the Card Diagnostics.

Note: There is a risk in doing so if there is a SRAM problem. The program stack may not be (and probably will not be) operational. Therefore, the program is likely to crash and destroy all the user register setups. The diagnostic system may not function.

If a diagnostic card is not inserted pressing **Control** and **Tempo** again invokes the Failure Viewing Mode. No data is stored in the failure log.

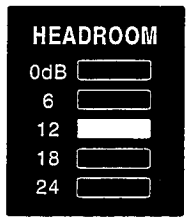
Pressing **Down** will cause the CPU to start executing the same test loop as described in the CPU test. The unit has to be power cycled to exit the test loop.

Failure log

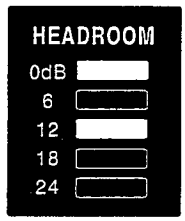
Test number	: 3
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: address or data

Display Test (4)
This test checks the display busy bit (U24 pin 9) by writing a "reset" display command to the display. The test verifies if the display busy signal is activated and then deactivated again. If not, a failure is reported. Maximum busy time is specified as 45µs.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and an attempt is made to write E4 to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. pressing **Load** will execute the next test.



Display Test



Display Test Failure

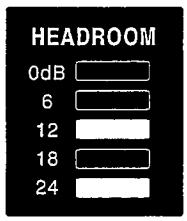
Failure log

Test number	: 4
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: N/A

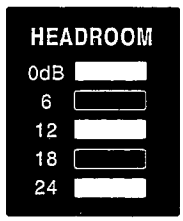
Host (V40) Timer/Counter Test (5)
The timer/counter test checks the 3 V40 (U46) internal counters. The test verifies that the status registers and the count registers don't have any stuck bits.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E5 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.

NOTE: The failure codes do not apply to this test.



Host Timer/ Counter Test



Host Timer/ Counter Test Failure

Failure log

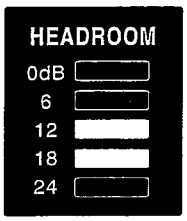
Test number	: 5
Tested value	: N/A
Failed value	: N/A

Address/location : N/A
Type of failure : Bit 0 = Timer 0 Status test failed if 1
Bit 1 = Timer 1 Status test failed if 1
Bit 2 = Timer 2 Status test failed if 1
Bit 4 = Timer 0 Counter test failed if 1
Bit 5 = Timer 1 Counter test failed if 1
Bit 6 = Timer 2 Counter test failed if 1

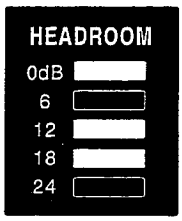
Host (V40) Interrupt Mask Test (6)

This test is limited to the internal V40 (U46) interrupt controller mask register. The register will be tested by a marching "1" and a marching "0" test.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E6 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.



Host V40 Interrupt Mask Test



Host V40 Interrupt Mask Test Failure

Failure log
Test number : 6
Tested value : Expected written data
Failed value : Actual read back value
Address/location : N/A
Type of failure : N/A

56k CPU and DRAM Test (7)

This test is executed by the 56k and consists of the 56k (U13 DSP) doing a CPU test and a DRAM test. The 56k does not have enough code space to be able to do both the CPU and DRAM test in the same sequence. The Host V40 (U46) therefore loads and executes the CPU and the DRAM tests separately. The

CPU test is executed first. A DRAM sizing test is a part of the DRAM test.

When the 56k finishes the test, it will send a done message to the Host. If it found an error, it will send an error message. If the Host gets the error message, it will log the error and report it to the display. The Host is also running a timer to keep track of the execution time and report error if the test is not completed in time.

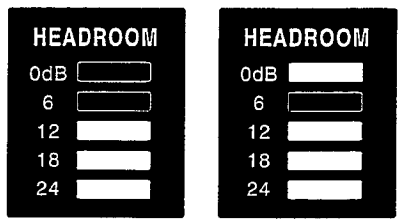
As this test can take quite some time, the Host doesn't wait for the test results. The Host goes and boots the Lexichip DRAM test and completes the Host V40 DRAM test before getting the test results from the 56k.

There are two versions of the 56k DRAM test. The first version tests only the standard 256k of memory, not the 56k Data Window Address Register. This is done to shorten the test time and therefore shorten the boot cycle time. The other version tests all of the installed DRAM: 256k, 1M, 4M, or 16M. This extended version also tests the 56k Data Window Address Register, accessing all of the memory. When 16 M of memory is installed, this test can take up to two minutes.

The extended version is invoked when:

- **Compare is pressed during power-on.**
- 56k DRAM size has been changed. DRAM size changes are automatically detected when the unit is turned on.
- SRAM has been cleared.

Before the test is executed, the following binary code will be put out on theHeadroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E7 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing Load will execute the next test. If the 56k- CPU or DRAM test fail, the TACOchip test will not be executed.



CPU and DRAM Test | CPU and DRAM Test Failure

Failure log

Test number	: 7
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

Lexichip DRAM Test (8)

Like the 56k DRAM Test, the Lexichip DRAM (U14 DSP) Test is not controlled by the Host V40. The Hosts role is to load a test code to the Slave Z80 SRAM (U33 DSP) and to communicate with the Z80 (U34 DSP) regarding test results. The Host V40 CPU ensures that the 56k Phase Locked Loop (PLL) is running

before loading code to the Z80 SRAM (The 56k has to be able to run the 56k DRAM code for the PLL to work). The Host - Z80 interface will not work properly unless the 56k PLL is working. The Z80 controls the Lexichip (U19 DSP) which actually performs the DRAM test. When the Z80 and the Lexichip finish the test, the Z80 will send a done message to the Host. If it found an error it will send an error message. If the Host gets the error message it will log the error and report it to the display. The Host is also running a timer to keep track of the execution time and report error if the test is not completed in time.

As this test can take quite some time, the Host doesn't wait for the test results. The Host goes and completes the Host V40 DRAM test and the 56k DRAM test before getting the test results from the Z80.

The Host V40 can instruct the Z80 to initiate two different versions of the Lexichip DRAM test. A simpler version, which shortens boot time is usually executed. A longer version is executed when the Compare button is pressed during power-on, or when the SRAM is cleared.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E8 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing Load will execute the next test. If the Lexichip DRAM test fails the TACOchip test will not be executed.

DRAM Test DRAM Test Failure

Failure log

Test number	: 8
Tested value	: Expected written data
Failed value	Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

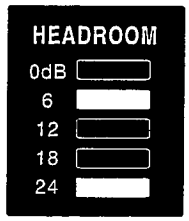
Host (V40) DRAM test (9)

The Host DRAM test is executed by the V40 CPU while it is waiting for the other CPUs to complete their respective DRAM tests. As with other DRAM tests, there are two versions, one executed under normal conditions, the other initiated by:

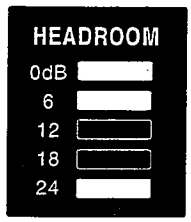
- pressing Compare during power-on

- clearing SRAM

Before the test is executed, the following binary code will be put out on the Headroom LEDs:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E9 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test. If the Host DRAM test fails, execution of Card Diagnostics is not recommended, as the DRAM is used by the Diagnostics. Execution may result in speaker



Host V40 DRAM Test



Host V40 DRAM Test Failure

damage and/or lost user registers.

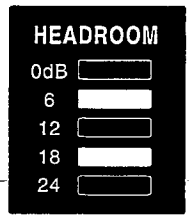
Failure log

Test number	: 9
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

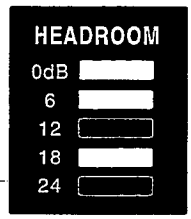
Battery test (0AH)
The Host CPU reads the battery low indicator and passes low/good battery information to the main operating system. The boot cycle is not discontinued if there is a low battery condition. When the battery voltage is close to the trigger level of the comparator, the comparator could start oscillating.

Before the test is executed, a binary code will be put out on the Headroom LEDs. The code is:
No failure log is generated, but a warning message will be displayed.

TACOchip Test (0BH)
The TACOchip test utilizes all CPUs. The 56k processor (U13 DSP) is in charge and sends data through the various slots of the TACOchip (U12 DSP). The Lexichip receives data, stores it in its DRAM, reads it back, and transfers it to the various slots in the TACOchip. Then the 56k fetches the data from the TACOchip



Battery Test



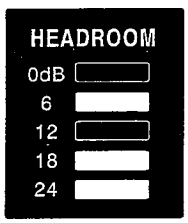
Battery Test Failure

and makes sure that data received matches data sent. When the 56k finishes the

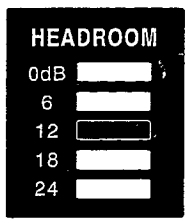
test, it will send a done message to the Host. If it found an error, it will send an error message. The Host logs the error and reports it to the display. The Host also runs a timer to track execution time, and reports an error if the test is not completed in time. The Z80's duty in this test is to transfer the Lexichip code that the Host V40 loads into the Slave Z80 SRAM (U33 DSP)to the Lexichip. The Z80 (U34 DSP) takes no part in determining failures. This test will not be executed if either the 56k or the Lexichip DRAM test fails.

Before the test is executed, a binary code will be put out on the Headroom LEDs. The code is:
If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E11 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.

Failure log



TACOchip Test



TACOchip Test Failure

Test number	: 0BH
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: TACOchip Address of first bad location
Type of failure	: Various

Troubleshooting

Problems with the PCM 80 can usually be classified as user interface problems or audio problems. User interface problems can range from one non-functioning front panel control to no display. Audio problems affect the signal quality from the analog or digital audio inputs and outputs. Some failures can be traced directly to one particular subsystem within the PCM 80, while others are caused by multiple sub-system failures.

When a problem is encountered, it is good practice to verify overall operation of the PCM 80 by running both the Power-On Diagnostics and the supplemental Memory Card Diagnostics. Refer to the Diagnostic functional instructions and troubleshooting hints given earlier in this chapter.

User Interface Problems

Display problems

Verify that all cable connections from the Host/Motherboard (J7-J9 and J16) to the various Front Panel boards are secure.

Vibration can eventually break the strands of cables making them intermittent or possibly open. Connections can become oxidized, corroded or otherwise contaminated causing them to be intermittent, open or resistive. For all of these reasons, caution should be used in troubleshooting. Before any cables are removed, they should be carefully inspected for proper seating and checked for continuity at all points between the Host/Motherboard and the Front Panel boards.

Verify that the +5VD supply is operational and within specification. Check the distribution of the supply to ensure that power is reaching the appropriate front panel display buffer and the register ICs.

If only one control on the Front Panel is failing, then the problem is probably a bad switch, encoder or potentiometer. If more than one control is failing, the problem may be with the Host Processor. Refer to the Diagnostic Descriptions and Theory of Operation.

Audio Problems

The first step when troubleshooting audio problems is to collect as much information as possible. The following lists some basic questions which should be answered before any repairs are attempted.

Is the problem:

1. on one output only?
2. at certain signal frequencies only?
3. at certain signal levels only?
4. in certain programs only?
5. at certain sample frequencies only?
6. with input only?
7. only without input?
8. temperature sensitive?
9. shock sensitive?

In general, it is best to verify overall audio performance and to further isolate the problem by running all of the audio proof-of-performance tests. This can be vital when troubleshooting subtle problems. Some system failures may cause a variety of tests to fail but troubleshooting based on one symptom type may be much easier than another. For example, a bad capacitor may produce a high level of distortion and a frequency response problem. The frequency response problem is easier to trace because the signal level can be monitored throughout the signal path on an ordinary oscilloscope.

One Bad Channel

One of the most useful pieces of information is determining whether a problem occurs on only one or on both channels. If the problem occurs at only one output, the following assumptions can generally be made with some level of confidence:

1. The power supplies are OK.
2. The system timing (clocks) is OK.
3. The digital circuitry (except for A/D and D/A conversion) is OK.

This type of problem can be fairly easy to troubleshoot, as the working channel can be used as a reference. With the same signal applied to both inputs, compare the signals on both channels at various points along the analog signal path. This may localize the problem fairly quickly.

The system diagnostics may be helpful in isolating RAM or DSP processor failures that might cause bad audio. Refer to the Diagnostics Descriptions for more information.

Both Channels Bad

As the likelihood of two separate components failing in the same way at the same time is remote, problems which occur in both channels can usually be traced to a component or components that are common to both channels, or to a system problem such as a power supply or timing problem. Verify that the power supplies are operational and within specification. If there is no output, refer to the next section.

No Output

First, determine whether the problem occurs on one or both channels.

When the machine has no output from only one channel, apply the same signal to both inputs, then compare the signals on both channels at various points along the analog signal path.

When the machine has no output from either channel, verify that the ±15V and the ±5V analog power supplies are operational and within specification. If the power supplies are OK, determine whether the problem lies within the A/D or the D/A conversion, then troubleshoot the corresponding circuitry.

Internal Adjustments and Troubleshooting

The following information allows testing of a non-functioning unit: no display, pegged input meters, load noises, popping crashes and /or no output. Test procedures are provided for checking power supplies, system clocks , battery voltage, and both analog and digital signal paths.

WARNING **CAUTION**

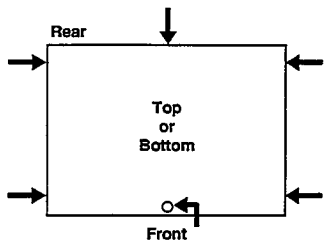
As these tests require removal of the PCM 80 cover, it is imperative that these tests be performed with regard to all safety and ESD precautions.

Required Equipment

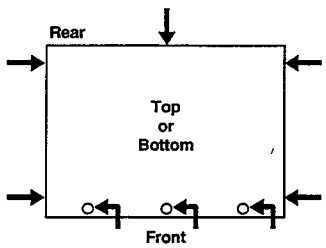
- DMM (Digital Mulitimeter)
- Frequency Counter
- 100 MHz oscilloscope (with 1X ,10X probes)
- Bench power supply providing a variac voltage adjustment and transformer isolation

Removing the Top and Bottom Covers

Remove the eight (or six in early models) screws which attach the top cover.



Older models have six (6) screws attaching the top and bottom covers, one on the top, one at the rear, and two on each side.



Newer models have an additional two screws on the top and bottom, making a total of eight (8) screws per cover.

Repeat for the bottom cover.

WARNING

THE POWER SUPPLY IN THIS UNIT HAS A LIVE HEAT SINK. DO NOT TOUCH WHILE THE UNIT IS PLUGGED IN AND POWERED ON.

Power Supply

1. Plug in the PCM 80 and set the variac for nominal line voltage. A clicking noise from the relays should occur 30 seconds after you have powered up the PCM 80.

2. Set DMM to measure VDC, and check the regulated voltages for the proper levels. Use the chassis (away from the power supply) as a ground reference.

Supplies	Location	Range
+5.1 VD	U17 pin 14	(4.85-5.25)
+15 V	J3 pin 1 (orange wire)	(14.25-15.75)
-15 V	J3 pin 3 (blue wire)	(14.25-15.75)
+5 VP	* Cathode side of D14	(4.75-5.25)
+5 VA	C50 (side closest to U7)	(4.75-5.25)
-5 VA	C49 (side closest to U7)	(4.75-5.25)

* The cathode side has the stripe.

Internal Battery Voltage

1. Turn PCM 80 power off and detach the power cord.
2. Set the DMM for a DC voltage reading on the 20 volts DC scale.
3. Place the positive probe (red) of the DMM on top of the Battery. Place the negative probe (black) on U29 pin 11 (just to the right of the Battery).
4. The reading on the DMM should be >2.75 volts. Replace the battery if the voltage is at 2.75 volts or lower.

System Clocks

These procedures test the major crystals and other clocks that are important to the operation of the unit. A frequency counter and an oscilloscope are required for these tests. The oscilloscope's ground lead should be connected to the PCM 80 chassis (away from the power supply).

1. Looking down on the unit with the top cover off, locate the DSP board which is screwed on to standoffs just to the right of the power supply area. Near the center of this board is Y1, a crystal that runs the Lexichip. Measure either side of this with the frequency counter. The reading should be 25.8MHz.

2. Turn PCM 80 power off and detach the power cord. Remove the screws that hold the DSP board in place. Remove the board and turn the power on. The message: Error E7 will be displayed.

3. Measure Y1, Y2, and Y3. Y1, the 16MHz clock that runs the microprocessor, is located to the left of the microprocessor (U46). Place the probe at U49 pin 1.

   Crystals Y2 (the 12.28MHz crystal) and Y3 (the 11.28MHz crystal) are located toward the rear of the unit. To measure Y2, which is used to generate the 48kHz Sample Rate Clock, place the probe at U45 pin 10.

   To measure Y3, which is used to generate the 44.1 kHz Sample Rate, place the probe at U56 pin 10.

Analog Audio Signal Tracing

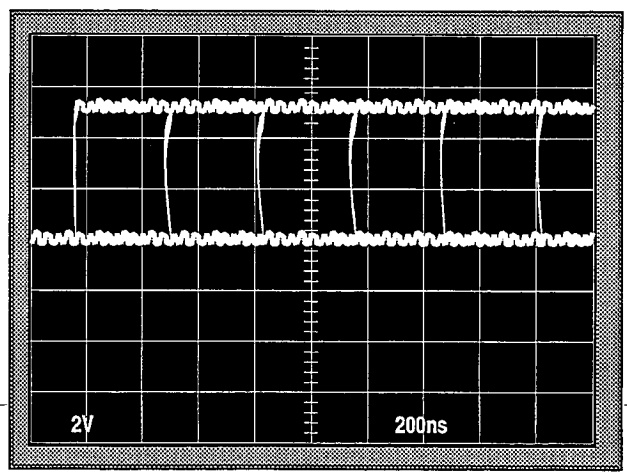
Required Equipment

- Level meter with oscillator
- Oscilloscope (to confirm audio signals for any visible problems)

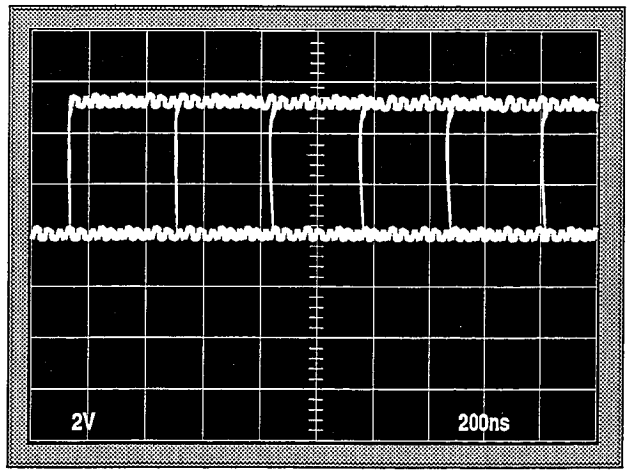
Setup

1. Place the PCM 80 in Bypass, Analog InLvl=100%, OutLvl=+40dBu, Sample Rate=Internal 44.1 or 48kHz. (See Analog Audio Performance Check: Setup).
2. Apply a 1kHz signal @ -20dBu (77.5 mVrms)
3. Turn input pot fully clockwise.

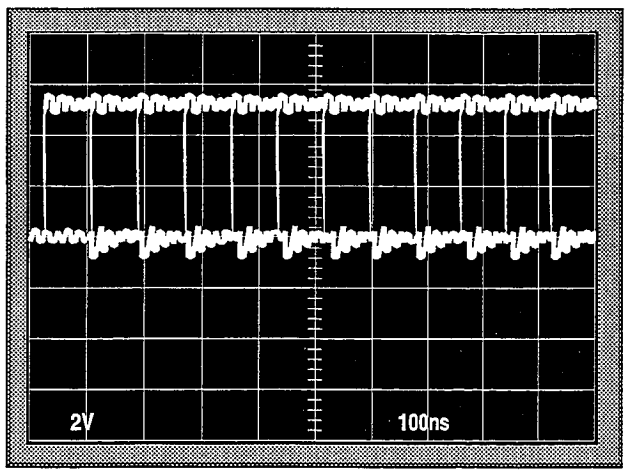
Name	Measurement Point	Levels
Input Stage	U1 Pin 1 Left signal U1 Pin 7 Right signal	-20dBu – Input Switch IN (BAL) or 0dBu – Input Switch OUT (UNBAL)
Input Level Pot	R29 Left Signal R30 Right Signal	-20dBu Bal or 0dBu Unbal (77.5mVrms-0.775 Vrms)
Left ADC Buffer	U6, Pins 1,7	-8dBu Bal or +12dBu Unbal (0.308 mVrms–3.08 Vrms)
Right ADC Buffer	U5, Pins 1,7	-8dBu Bal or +12dBu Unbal (0.308mVrms - 3.08 Vrms)
ADC Inputs	U7 Pins 3+4 Left U7 Pins 25+26 Right	-8dBu Bal or +12dBu Unbal (0.308mVrms 3.08 Vrms)
ADC Outputs	U7 Pin15 or R32	This is a Digital audio signal +5volt CMOS Characteristics If there is no output at this pin check for information at 256FSA at pin 19, 64FSA at pin 14, WCA/ at pin 13) WCA/ = Sample Rate (44.1 or 48kHz) 64FSA = 64xSample Rate (2.82 or 3.07MHz) 256FSA = 256xSample Rate (11.28 or 12.28MHz)



Digital Filter Input	U12, Pin1	Digital audio signal



DAC Inputs	U11, Pin 10 Right Side Pin 15 Left side	Digital audio signal



DAC Outputs Audio signal	U11 Pin 17 Left out U11 Pin 8 Right out	-8dBu Bal or +12dBu Unbal (0.308 Vrms - 3.08 Vrms)
Lowpass Filter	U10 Pin 7 Left out U10 Pin 1 Right out	-2dBu Bal or +18dBu Unbal (0.616 Vrms - 6.16 Vrms)
		With output level set at +4dBu:
Output Drivers	U9 Pin 4 Left in U9 Pins 8,1 Left out	-2dBu Bal or +18dBu Unbal (0.616 Vrms - 6.16 Vrms)
		With output level set at -10dBu:
	U8 Pin 4 Right in U8 Pin 4 Right Out -16dBu Bal or+4dBu	-16dBu Bal or +4dBu Unbal (0.123 Vrms - 1.23 Vrms)

Digital Audio Signal Tracing

This procedure verifies the Digital Audio Path of the PCM 80.

1. The input for the Digital signal is RCA J10 (white, marked S/PDIF) on the back of the PCM 80. Typical input level is 0.5 Vpp. The signal level is stepped up to 2.5Vpp (typical) by a 1:5 transformer (TX2) and goes to the input of the Digital Audio Receiver (U19, Pin 9). U19 outputs a serial audio data stream at 5Vpp (typical) via Pin 26.
2. The signal travels to pin A8 of J17, then goes to the DSP board for processing.
3. After the signal is processed, it comes back down onto the Host board via pin B10 of J17, and then passes through a gate (U47, Pins 1 and 3). The 5Vpp signal goes to the input of the Digital Audio Transmitter (U22, Pin 8).
4. The Digital Audio Transmitter generates the S/PDIF formatted signal. This 5Vpp signal exits U22 at Pin 20 and goes through a resister divider network (R98-99) to bring the signal level down to 1Vpp. When properly terminated by 75Ω, the signal level will drop further to 0.5Vpp.

DAC Adjustment

1. Place the PCM 80 in Bypass, Analog InLvl=100%, OutLvl=+4dBu, Sample Rate=44.1 or 48kHz Internal. (See Analog Audio Performance Check: Setup).
2. Input a -20dBu (77.5mVrms) "Bal" or -40dBu (7.75mVrms) "Unbal" 1kHz signal into the PCM 80, and set the Distortion Analyzer to its THD+Noise setting. The PCM 80 front panel Input Level control should be set at 12:00, or the unit should be set for unity gain.
3. While observing the Left output, adjust R54 to a distortion reading between 0.2 to 0.3 % on the analyzer.
4. Switch to the Right output and adjust R52 to a distortion reading of 0.2 to 0.3%.

System Signal Tracing

This procedure tests basic digital control signals in the PCM 80. For each of the following signals, load **P0 0.0 Prime Blue**, probe at the indicated place, and check for the expected results.

DSP Board Clocks

FCLK — DSP board: Probe on circuit-side at either side of R32
DSP56002 Clock: Should be a 40MHz square wave.

SLVCLK, SLVCLK/ — DSP board: Probe on circuit-side at either side of R34 and R33, respectively
Slave Clocks: Should be a 10 MHz square wave.

Misc Signals

HWAIT/ — DSP board connector: Probe on circuit-side of DSP board J4 pin B26) Host Wait Signal. Double low-going pulse spaced at about 10 µS apart. These two pulses should repeat every 20mS. More activity can be seen when adjusting the size parameter in the Edit menu (matrix position **2.0**).

MUTE/ — (U25 pin 15) Master Mute Line: Normally high, low on power-up.

Reset Signals

MRST/ — (U55 pin 1) Master Reset: Normally high, low on power-up.

SLVRST/ — DSP board connector: Probe on circuit-side of DSP board J4 pin A22.
Slave Reset: Normally high, low on power-up.

LEXRST/ — DSP board connector: Probe on circuit-side of DSP board J4 pin A20
Lexichip Reset: Normally high, low on power-up.

56KRST/ — DSP board connector: Probe on circuit-side of DSP board J4 pin B10)
DSP56002 Reset: Normally high, low on power-up.

Interrupt Signals (See Theory of Operation: Interrupt Timing)

HNMI — (U34 pin 3) V40's NMI line: Normally low. When DIOIMSK/ is high, it is ulsed high on digital I/O errors such as as loss-of-lock

PROGINT5 — (U26 pin 2) V40's INTP5 line: Periodic high-going pulse
Pulse width=10 =mS (approx.)
Period=20ms

PROGINT7	(U26 pin 6) V40's INTP7 line: Periodic high-going pulse Pulse width=11ms (approx.) Period=40 ms
WDKICK/	(U14 pin 5) Watch Dog Timer Kick Pulse: Pulsewidth=150nS Period=1mS

Encoder Signals

ASNB, ASNA	(U43 pins 3 and 2 respectively) Adjust Soft Knob Lines B and A: As ADJUST is rotated clockwise, the following patterns should rotate in relative order: High, High High, Low Low, Low Low, High
SSNB, SSNA	(U43 pins 5 and 4 respectively) Select Soft Knob Lines B and A: As ADJUST is rotated clockwise, the patterns described above should rotate in relative order.

LED/Switch Scanning Signals

LHRCOL/, RHRCOL/	(U29 pins 14 and 13 respectively) Left and Right Headroom LED Column Strobes: Square Wave with a 4mS period.
SWC0/, SWC1/, SWC2/	(U42 pins 19, 18, 17 respectively) Switch & LED Column Strobes: Low-going pulse, Pulse width=2 mS, Period=6mS
LDRW0/, LDRW1/, LDRW2/	U42 pins 16, 15, 14 respectively) LED Row Strobes: Reload P0.0 Prime Blue. Observe the following on U42 pin 16: Low-going pulse, Pulse width=2mS, Period =6mS Press "Edit" Button. Observe the following on U42 pin 15: Low-going pulse, Pulse-width=2mS, Period=6mS Press "Register" Button. Observe the following on U42 pin 14: Low-going pulse Pulse width=2mS, occasionally 4mS when tempo light blinks Period=6mS

PCM80 Extended Memory (SIMM) Installation

The addition of SIMMs (memory modules) allows several PCM 80 algorithms (Glide>Hall, M-Band+Rvb and the Resonant Chords algorithms) to address up to 4 Meg of delay memory, providing as much as 42 seconds of stereo delay. PCM 80 memory can be expanded with SIMM memory modules of the following type:

30-pin SIMM Memory Module	
Usable densities:	1 Meg x 9 (true parity) 4 Meg x 9 (true parity) 16 Meg x 9 (See Physical Requirements. Note also that only 4 Meg will be addressed by the PCM 80.) 8-bit SIMMs are **not** usable 9-bit SIMMs (logic parity) are **not** usable
Access Time:	70 nsec or faster
Physical Requirements:	Either 3-chip or 9-chip modules may be used, with the following size restrictions: Maximum size: .208" (5.28mm) total module thickness 1.30" (33mm) total module height 3.50" (88.9mm) total module length

Required Equipment

- 2 SIMMs modules
- #1 Phillips Head screwdriver
- Anti-static workstation

WARNING **CAUTION**

Modification should be performed only by qualified technical personnel. Damage caused by performing this modification may void the manufacturer's warranty.

1. Turn PCM 80 power off and detach power cord.
2. Remove the screws (6 on early models, 8 on later models) from the PCM80 top cover.
3. Remove the top cover.
4. Locate the Digital Board (on top of the Main Board) and remove the four (4) screws at the corners of the Digital Board.
5. Hold the Digital Board at the two righthand corners and lift the board off of the Main Board.
6. Install the SIMMs by sliding the board, component side up, into the socket so that the gold "fingers" of the board slide into the socket.
7. Lift the jumper block from W1 pins 2 and 3 and reposition it at W1 pins 1 and 2.
8. Reinstall the board and reassemble the machine.

When the machine is turned on it should go through an EXTENDED MEMORY TEST and tell you how much memory is installed.

Restoring Factory Settings

The following procedure restores the PCM 80 factory default settings. This may be necessary due to memory problems, or following internal battery replacement.

This procedure will destroy any user settings or registers. Save setups and registers on a Memory Card to reload after this proceudre is completed.

1. Set the INPUT GAIN switch on the rear panel of the PCM 80 to the OUT position.
2. Set the front panel INPUT control fully counterclockwise.
3. Press **Down** until the display reads: **System Edit Mode/1.0/Go**
4. Turn SELECT until the display reads: **System/Initialize/1.8 (Press STORE)**
5. Press **Store** and verify that the display flashes the following message: **Are you sure? (Press STORE)**
6. Press **Store** and verify that the display flashes the following message for about 1/2 second: **Restoring Original Factory Settings...** then the message: **Loading Effect ...** then the display: **Chorus+Rvb/P0 0.0/Prime Blue**
7. Turn off the PCM 80 and detach the power cord.
8. Remove the 4 phone plug cables from the PCM 80.

5

Theory of Operation

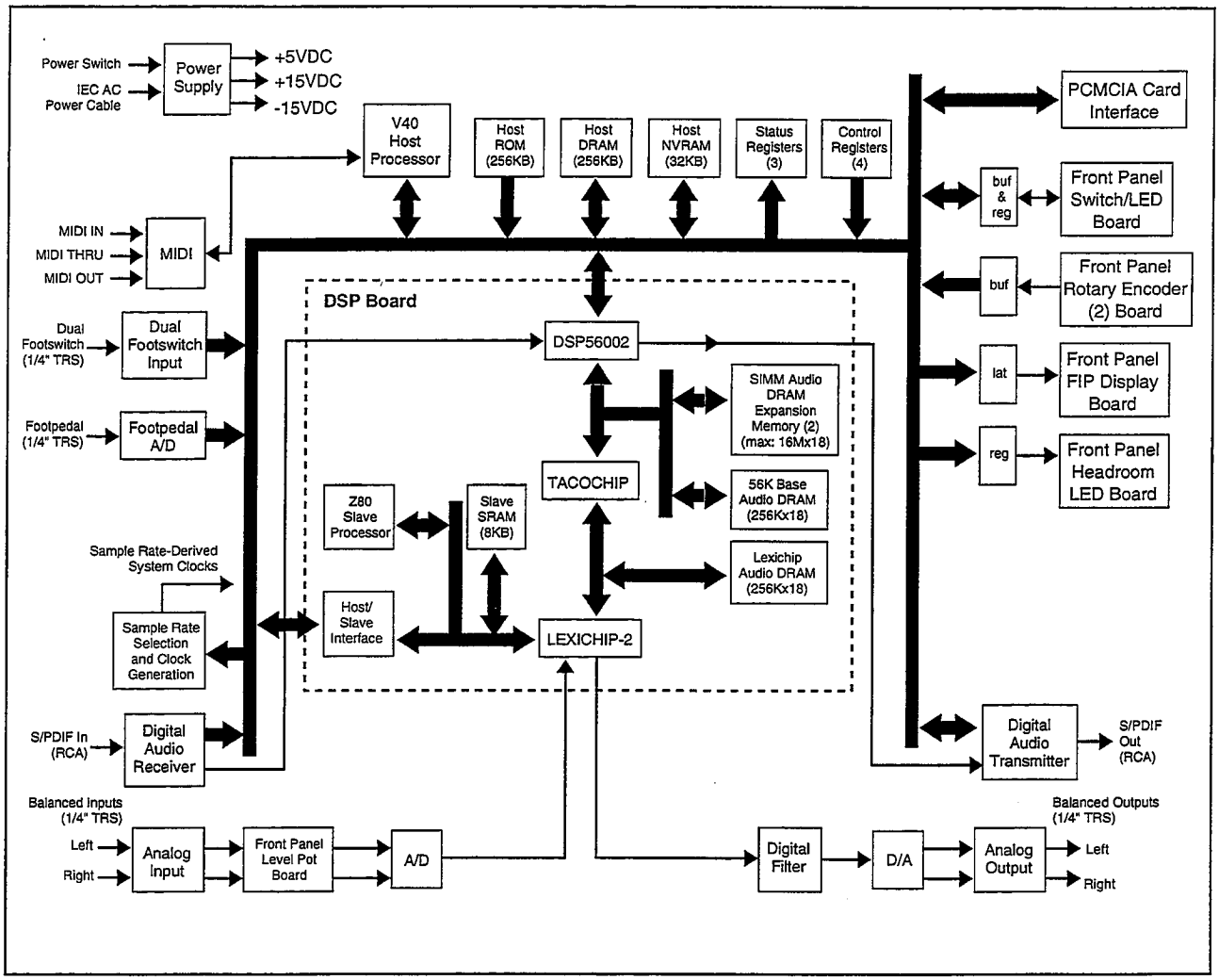
Architectural Overview

The PCM 80 digital hardware utilizes multiple microprocessors and digital signal processors to perform digital audio effects which are controlled via the front-panel interface, and the MIDI serial interface.

The PCM 80 features five major circuit sections: Host, DSP (Digital Signal Processing), Digital I/O, Analog Conversion, and Power Supply sections. A 10 MHz NEC uPD70208, also known as the V40, provides host microprocessor functions. The host processor circuit manages the user interface including the FIP display, softknobs, switchboard, status and headroom LEDs, MIDI, the footswitch and footpedal, and digital I/O circuitry. It is also responsible for program-load and parameter-passing to the DSP circuitry on the DSP board. The DSP board is responsible for the digital effects processing of the PCM 80. It has a unique tightly-coupled multi-DSP engine featuring three ASICs (Application Specific Integrated Circuits): Lexicon's proprietary Lexichip-2 and Tacochip, and a Motorola DSP56002. A slave microprocessor, the Zilog Z-80, provides independent housekeeping functions for the Lexichip-2. The analog conversion circuitry handles A-to-D conversion and D-to-A conversion as well as a high performance analog interface to the balanced-line jacks on the rear-panel. The digital I/O circuitry implements S/PDIF digital audio I/O.

The PCM 80 is physically sectioned into two major circuit boards, five minor circuit boards and a power supply module. The two major circuit boards are the Host Board and the DSP Board. The host processor, digital I/O and analog conversion circuitry reside on the Host Board while the DSP circuitry resides on the DSP Board which connects to the Host Board directly via a 72-pin connector. Smaller boards which are connected to the Host Board include the Front-Panel Switch Board, Front-Panel Encoder Board, Front-Panel Headroom Indicator LED Board, Front-Panel Input Level Pot Board, and the Intelligent FIP Display Module. The Power Supply Module supplies +5VDC, +15VDC, and -15VDC.

Block Diagram



Host Processor Circuitry

The Host Circuit is responsible for management of front-panel controls and displays, MIDI interface, Tap/Tempo/LFO functions, and download and real-time control of DSP code. There are 256K bytes of ROM, 256K bytes of DRAM, and 32K bytes of battery backed-up SRAM. The 32K bytes of SRAM are for non-volatile system parameter and user register storage.

The main processor of the host circuit is the NEC V40 (uPD70208) (U46). The V40 CPU has several on-chip peripherals including an 8-level priority interrupt controller, DMA controller, timers, and a serial port. The 8-level interrupt controller allows for management of several time-critical periodic tasks in order to meet the real-time requirements of the PCM 80. The DMA controller allows DSP-code download to happen in the background without significant impact on system performance. The timers provide MIDI UART clock generation, and timing references for tempo and LFO functions. The serial port is used to implement the MIDI interface.

In summary, the main host responsibilities are:

- Management of the user-interface:
  Intelligent front panel display FIP
  Front-panel switches
  Switch status LEDs
  Headroom LEDs
  Foot controller pedal jack via 8-bit A/D
  Footswitch jack
- Processing data and instructions to and from the MIDI UART (internal)
- Maintenance of non-volatile SRAM for storage of user registers
- Transparent refresh of Host DRAM.
- Providing download/upload to/from PCMCIA card interface
- Loading of slave Z80/Lexichip program code and data
- Controlling slave Z80/Lexichip reset and interrupt functions.
- Loading of DSP56002 program code and data
- Controlling DSP56002 reset, interrupt, and DMA functions
- Selecting sampling rate to be 44.1 kHz, 48 kHz or PLL frequency
- Management of channel status and reset functions for digital I/O interface
- Controlling audio muting hardware
- Management of user-defined control patching and LFO functions
- Management of Tap key and Tempo functions

Clocks

A 16 MHz crystal (Y1) is used to generate an 8 MHz clock used as the internal processor clock. This clock is also sourced from the V40 (HCLK) to clock external control logic: a hex flip-flop (74AC174) at U48 and a GAL20V8 at U49. HCLK is also inverted by a 74AC00 (U61) to source HCLK/. HCLK/ clocks a hex flip-flop (74HC174) at U62 and a GAL16V8 on the DSP board.

Bus Interface

The V40's 8-bit data bus is bidirectionally buffered by a 74HC245 (U59). Since twelve of the twenty V40 address lines are multiplexed with data and processor status, two 74HC573s (U50, U60) are used to latch and buffer sixteen of them (HA<19:0> less HA<11:8>). HA<11:8> are sourced directly from the V40.

Host Bus Status lines (HBS<2:0>), Host Memory Read Line (HMRD/), Host Memory Write Line (HMWRB/), and the Host Refresh Request Lines (HREFREQ/) are sourced to the GAL20V8 for memory interface logic.

Interrupts

The host processor has nine interrupts: one non-maskable interrupt (NMI) and eight maskable priority interrupts (INTPx). The priority ordering of the eight priority interrupts is preset as follows: INTP0 (highest) to INTP7 (lowest).

	Non-Maskable Interrupt
NMI	Digital Audio Receiver Error Condition
	Maskable Interrupts
INTP0	Timer 0 (LFO Interrupt) (Periodic: 1 msec) (Internal) (Highest Priority)
INTP1	MIDI Port Transmit/Receive (Internal)
INTP2	Timer 2 (Front Panel Display Interrupt)
INTP3	DSP56002 DMA Transaction Complete
INTP4	DSP Interrupt (Z80 or DSP56002)
INTP5	Programmable Interrupt P5 (Patch Calculations Process)
INTP6	Programmable Interrupt P6 (reserved for future enhancement)
INTP7	Programmable Interrupt P7 (Front Panel Interface Process) (Lowest Priority)

INTP0 and INTP1 are sourced internal to the V40. INTP2 is sourced from the V40's Timer 2. INTP3 is sourced by the V40's DMA controller Transaction Complete Flag ("TC/"). INTP4 is sourced externally by an interrupt sourced either by the Z80 or the DSP56002 on the DSP board. The interrupt can be identified by reading 56KINT and SHINT in Status Register 1. (U24 pins 3 and 2.) 56KOVRL/, a parallel control bit toggled by the DSP56002, is the source of the interrupt. It is gated by a 74HC08 AND gate with FINTMSK/ to generate 56KINT. (56KINT is enabled when FINTMSK/ is high, and disabled when it is low.) Note that, as the interrupt 56KOVRL/ is the inverted PC4 bit of the DSP56002, the default state of PC4 should be high. For the DSP56002 to interrupt the host, PC4 should be set low until the host sends a interrupt-acknowledge message via the host port to reset the bit high. INTP5, INTP6 and INTP7 are sourced by software-programmable bits in Control Register 1 (U26 pins 2, 5 and 6). The interrupts are rising-edge triggered.

When probing with an oscilloscope, the following should be observed on each of the V40's interrupt pins, while running the program **P0 0.0 Prime Blue:**

NMI	(U46 pin 66)	Normally low. (When DIOIMSK/ is high, it is pulsed high on digital I/O error such as loss-of-lock)
INTP0		Not accessible (Internal to V40)
INTP1	(U46 pin 37)	Not accessible (Internal to V40) (Externally grounded)
INTP2	(U46 pin 38)	Periodic low-going pulse (Pulse-width=250ns, Period=2ms)
INTP3	(U46 pin 39)	Periodic low-going pulse (Pulse-width=125ns, Period=3.6ms (approx.)
INTP4	(U46 pin 40)	Non-periodic
INTP5	(U46 pin 41)	Periodic high-going pulse (Pulse-width=10ms (approx.), Period 20ms)
INTP6	(U46 pin 42)	Reserved for future enhancement
INTP7	(U46 pin 43)	Periodic high-going pulse (Pulse-width=11ms (approx.), Period 40ms)

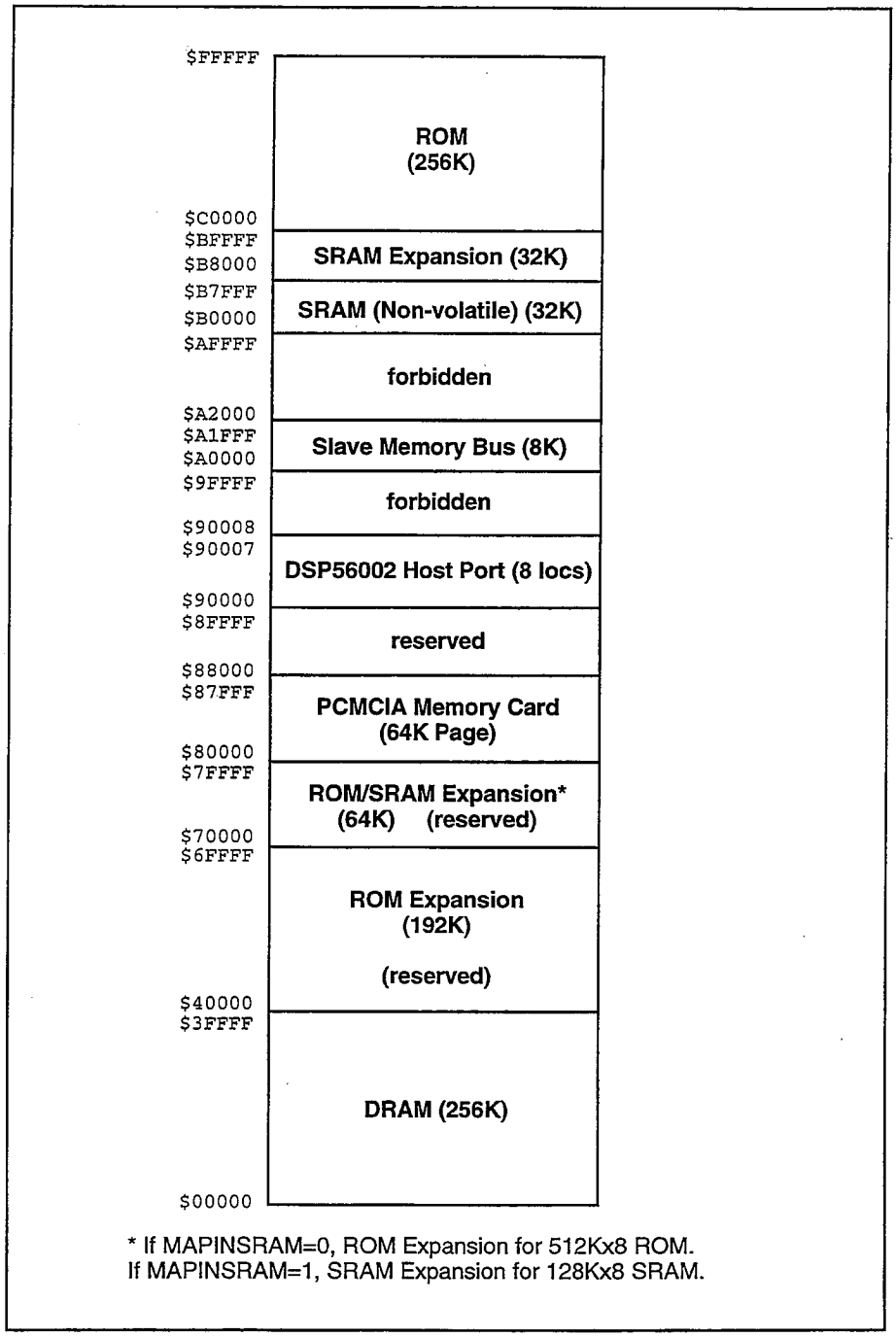
On-Chip Peripherals

V40 on-chip peripherals include:

- Clock generator
- Bus interface
- Bus arbitration
- Programmable wait-state generator
- DRAM refresh controller
- 3 16-bit timer/counters:1 for MIDI UART clock, 1 for 2ms display interrupt tick, 1 for 1ms interrupt tick
- Asynchronous serial I/O controller (for MIDI)
- 8-input interrupt controller
- 4-channel DMA controller (Only one used – for DSP56002 host port transactions)

Host Memory

A GAL20V8 (U49) provides memory decoding for ROM, SRAM, DSP56002 Host port, Slave Z80 RAM Access, and DRAM. Following is the Host V40 memory map:



Memory Address Map

ROM

A 27C020/27C2001 (U39) which is a 2-megabit EPROM in a 256Kx8 configuration is installed.

The ROM enable signal (HROMEN/) is sourced by the GAL20V8 (U49) to enable the ROM when the memory address range is $C0000 to $FFFFF. (If a 512Kx8 ROM is used, the lower 256KB is mapped to $40000 to $7FFFF, and the higher 256KB is mapped to $C0000 to $FFFFF. Note that the upper 64K of the lower 256KB is displaced by SRAM if a 128KB SRAM is used and the control bit MAPINSRAM is asserted.)

Dynamic RAM (DRAM)

256Kx8 Dynamic RAM is provided. Two 44256 (256Kx4) parts at locations U52 and U51 in 20-pin ZIP packages are used to implement high and low nibble. U51 implements the low nibble. Refresh is taken care of by the V40 automatic refresh cycle which needs to be set up by software. Host address bits 17-0 are multiplexed to provide 9 row and 9 column address bits.

DRAM control is implemented by a GAL20V8 (U40) and a 74AC174 (U62). The GAL generates two signals DMEMOP/ and SELCA. DMEMOP/ is asserted for both read and write accesses to the DRAM. This signal is clock-delayed by U62 to generate HRAS/, the row address strobe. PTHRAS/ (pre-terminated version of HRAS/) is clock-delayed once again to generate HCAS/, the column address strobe. SELCA goes to 74AC157 multiplexers (U53, U54, U63) to source row and column address lines. When SELCA is asserted high, address lines HA<19:10> are selected to source the column address to HDRA<9:0>. When SELCA is not asserted (low), address lines HA<9:0> are selected to source the row address to HDRA<9:0>. During DRAM access, HMRD/ distinguishes between reads and writes. When HMRD/ is asserted low, it is a read operation. Otherwise it is a write operation.

The timing of the Host DRAM interface is shown in detail in later in this chapter.

Non-Volatile Battery Backed-Up Static RAM

A battery backed-up 32Kx8 Static RAM (U38) is provided to implement non-volatile storage. It is primarily used for system control parameter and user register storage. The 32-pin SRAM socket is factory shipped with a 28-pin 32Kx8 SRAM, installed with pin 1 of the IC aligned to pin 3 of the 32-pin socket.

The following table outlines the memory mapping for various configurations. The signal NVRAMEN is asserted by the GAL20V8 depending of the address lines and the control signal MAPINSRAM. MAPINSRAM, when asserted, allows the full use of 128Kx8 SRAMs. However, the lower 64KB of SRAM displaces the upper 64K portion of the reserved ROM expansion space. As current software only supports the 32Kx8 SRAM, MAPINSRAM should never be asserted.

RAM Type	MAPINSRAM	Memory Size	Address Range
32K x 8	0	32KB	$B0000-$B7FFF
128K x 8	0	64KB	$B0000-$BFFFF (upper 64KB only)
128K x 8	1	128KB	$70000-$7FFFF (lower 64KB) $B0000-$BFFFF (upper 64KB)

NVRAMEN is inverted by a 74AC00 (U15) NAND gate to yield QNVRAMEN/ which is an asserted-low signal going to the chip enable of the SRAM. QNVRAMEN/ is also qualified by PWR_OK which is source from the +5V Monitor (MC34164-U16). When power is going down, PWR_OK gets asserted and QNVRAMEN/ is gated off. The 74AC00 is powered by VRAM which is the battery backup voltage. This ensures that as power goes down, that the CE1/ pin of the RAM tracks Vcc as required by the SRAM manufacturer for reliable data retention. When the unit is on, VRAM should be at 5V. When the unit is on, VRAM follows the voltage from the backup lithium battery (3V) (BAT1).

Battery Backup

The Battery Backup circuitryis designed to protect data in the non-volatile SRAM. It is triggered (controlled) by the +5V Monitor, U16. To ensure the lowest possible leakage current during power on, two transistors (Q5 and Q6) are used to switch between backup operating modes.

A buffer (HC08), guaranteed to operate down to 2V is used to drive Q5. R76 ensures that the transistor stays off while the HC08 Vcc is less than 2V.

D28 is a Schottky diode to minimize the forward voltage drop while power is off. R82 protects the battery in case the diode should fail.

The battery low indicator is set to trigger at approximately 2.1-2.5V. If the battery is low, the status line BATLOW is asserted.

PCMCIA Memory Card

A PCMCIA memory card slot (J19) provides removable user register storage, and capability for algorithm and host software updates. Up to 1 MB of memory on a PCMCIA card is accessable. The host has a 64K window into the card memory space. The PCMCIA card enable signal CARDEN/ is asserted by the HOST GAL20V8 (U49) whenever the address accessed is the range $80000-$8FFFF. The PCMCIA interface in the PCM 80 is designed to handle all cards with an access time of 250nS or faster. The selected 64KB page within the 1MB of card space is set by 4 bits in Control Register 3. This allows up to 16 pages (16x64KB=1MB). The location within the page is selected by the 16 LSBs when the card is selected. The 4-bit page register CA<19:0>, set by Control Register 3 <3:0>, extends the card addressing capability to 1MByte. When the CREG/ control bit (Control Register 3 bit 7) is asserted low, the card's configuration register is selected instead of normal memory access.

Three 71HC541 octal buffers provide address line buffering (U67, U68) and control line buffering (U66). All three are enabled by software when doing card operations, and are disabled otherwise. They are enabled by de-asserting (setting high) DISCARD/ (Control Register bit 6.)

When DISCARD is asserted high:

- Address lines are pulled-down to ground via RP6 and RP7.
- CCE1/, COE/, and CWE/ are pulled-up to CVCC via RP5.
- CARDENB/ is pulled to a high by R176, disabling the bidirectional data buffer (U65).

A bidirectional data buffer 74HCT245 (U65) is used to isolate the card data lines from the host data bus HD<7:0>. The signal HMRD/ determines the direction. When low, data is enabled from the card data bus CD<7:0> to HD<7:0>. When high, data is enabled from HD<7:0> to CD<7:0>.

Software detects whether or not there is a card installed by reading CARDDET/ (Status Register 0 bit 4). This signal is asserted low when both ends of the PCMCIA card are plugged in, ensuring that the card is not powered-up or accessed until fully plugged in. The end-pin signals: CDET1/ and CDET2/ are pulled high when their respective pins are not inserted. These pins are grounded and, when they are inserted into J4, the corresponding lines are pulled low. A 74AC32 (U64) provides this logic by ANDing CDET1/ and CDET2/ to assert CARDDET/ (low).

Software reads the PCMCIA card write protection switch by reading CWRPROT (Status register 0 bit 5). CWRPROT is a buffered version of CWP via U66. Both CWRPROT and CWP are pulled-up to CVCC. When no card is inserted, CVCC will dischage to ground. Therefore, CWRPROT is not valid unless the card is fully inserted and enabled by setting DISCARD/ high.

The three remaining sections of the 74AC32 (U64) are used to produce a gated version of HMWR/ called PREBCWE/ . This signal gives an earlier rising edge to give the PCMCIA card the proper data setup time. PREBCWE/ is buffered by U66 to source CWE/ (the write enable that goes directly to the card).

The timing of the PCMCIA Card interface is shown in detail later in this chapter. Note that one wait state (generated by the V40 preset by software) is inserted for all card access.

Two status lines (CARDBVD<2:1>) from an inserted SRAM PCMCIA card indicate the condition of its battery. These are read by the host from Status Register 0 bits 3:2 respectively. Both signals are kept asserted when the battery is in good condition. A replacement warning condition is signaled by CARDBVD1 asserted and CARDBVD2 not asserted. In that case, data integrity on the card is still assured. If CARDBVD1 is not asserted, with CARDBVD2 either asserted or not asserted, the battery is no longer servicable and data is lost.

The following summarizes PCMCIA card control bits via Control Register 3:

Control Register 3 (I/O location=$0006)

7	6	5	4	3	2	1	0
CREG/	**DISCARD/**	FLASHVEN	MPINSRAM	**CA19**	**CA18**	**CA17**	**CA16**

The following outlines the PCMCIA card status via Status Register 0

Status Register 0 (I/O location=$0000 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	SINGOUT/	**CWRPROT**	**CARDDET/**	**CARDBVD2**	**CARDBVD1**	spare	FOOTSWR

Host-to-Slave Z80/Lexichip Interface

The host has direct access to the DSP board's Slave Z80 8K SRAM. The Z80, in turn, is responsible for loading and modifying Lexichip program code internal to the chip. The address range for host access to the Slave Z80 SRAM is $A0000-$A1FFF. This memory address range is decoded by the HOST GAL20V8 (U49) to assert SBUSEN/ (low). (This corresponds to the Z80's local address range of $0000-$1FFF.)

Host-to-DSP56002 Interface

There are two methods of Host to DSP56002 communication: Register access using the HA<2:0> address lines, and DMA (direct memory access).

Register access is mapped to host memory addresses $90000-90007. (These locations are duplicated in the whole range between $90008 and $97FFF.) This memory address range is decoded by the HOST GAL20V8 (U49) to assert DSPHEN/ (low). This signal goes directly to the DSP56002 (U13) on the DSP board.

The signals HREQ, HACK/, and HMRD3Q synchronize DMA transfers. The signal HREQ from the DSP56002 (on the DSP board) to the host board is clock-delayed by a 74AC164 (U62) to source HREQQ to the DMA request 0 input on the V40 (U46-28). The V40 in turn sources the DMA acknowledge signal HACK/ back to the DSP56002. The signal HMRD3Q gates off HACK/ to source the actual acknowledge line that goes to the DSP56002 (QHACK/) to provide adequate data hold time. This gating is done on the DSP board by a 74AC32 (U18). The signal host V40 signal HTC/ is pulsed upon the DMA-cycle's full completion.

Host I/O

I/O Address Map

Two 74HC138s (U27 and U28) provide I/O decoding for writeable and readable registers. The 74AC00 (U61) provides decode for the 8-bit ADC used to read the foot controller jack. The 74HC174 (U48) provides various HCLK delayed signals for I/O interface control. Host I/O address mapping is summarized as follows:

READS:

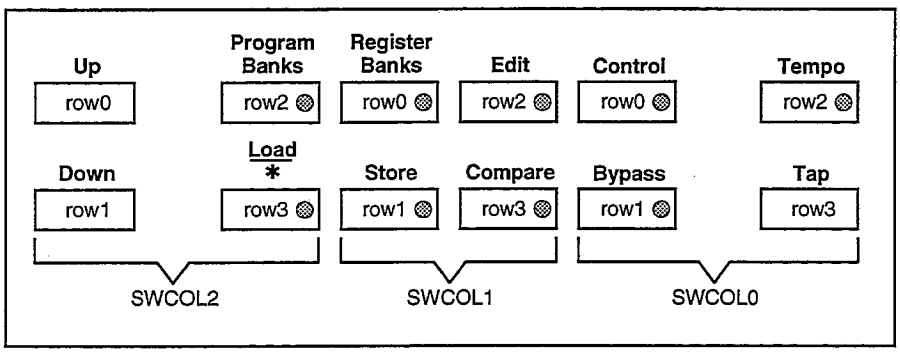
Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0010 (H)	Footcontroller A/D Conversion Data
xxxx xxxx xxx0 111x (B)	$000E (H)	Watchdog Timer Kick
xxxx xxxx xxx0 110x (B)	$000C (H)	Switch Matrix Row and Soft Knobs
xxxx xxxx xxx0 101x (B)	$000A (H)	Clear Slave-to-Host Interrupt
xxxx xxxx xxx0 100x (B)	$0008 (H)	Clear Lexichip Overload Flag
xxxx xxxx xxx0 011x (B)	$0006 (H)	(unused)
xxxx xxxx xxx0 010x (B)	$0004 (H)	Status Register 2
xxxx xxxx xxx0 001x (B)	$0002 (H)	Status Register 1
xxxx xxxx xxx0 000x (B)	$0000 (H)	Status Register 0

WRITES:

Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0010 (H)	Foot Controller A/D Conversion Start
xxxx xxxx xxx0 111x (B)	$000E (H)	Front Panel Display FIP
xxxx xxxx xxx0 110x (B)	$000C (H)	Switch/Status LED Matrix Cols/Rows
xxxx xxxx xxx0 101x (B)	$000A (H)	Set Host-to-Slave Interrupt
xxxx xxxx xxx0 100x (B)	$0008 (H)	Headroom LED rows
xxxx xxxx xxx0 011x (B)	$0006 (H)	Control Register 3
xxxx xxxx xxx0 010x (B)	$0004 (H)	Control Register 2
xxxx xxxx xxx0 001x (B)	$0002 (H)	Control Register 1
xxxx xxxx xxx0 000x (B)	$0000 (H)	Control Register 0

Front Panel Switches

The front-panel switches are arranged on the front-panel board as shown below.



Switches are arranged in a 4 row x 3 column matrix in which each column of 4 rows are read by:

1. Asserting one bit of the Switch Column (SWCOL<2:0>/) field of the SWITCH/ LEDs MATRIX REGISTER (74HC574,U42).
2. Then reading the Switch Row (SWROW<3:0>) field of the the Switch Matrix Input Buffer (74HC541, U43).

The control register and the Switch Column Matrix Buffer are outlined follows:

Switch/LED Matrix Register (I/O location=$000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	LDRW2	LDRW1	**LDRW0/**	**SWC2/**	**SWC1/**	**SWC0/**

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

7	6	5	4	3	2	1	0
SWROW3	**SWROW2**	**SWROW1**	**SWROW0**	SSNB	SSNA	ASNB	ASNA

Soft Knobs

Two 36-position 2-bit gray-code encoded knobs with detents are used to implement the SELECT and ADJUST Soft Knobs. The 2-bits of each (available by reading the Switch Matrix/Soft Knobs Input Buffer) are assigned as follows:

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

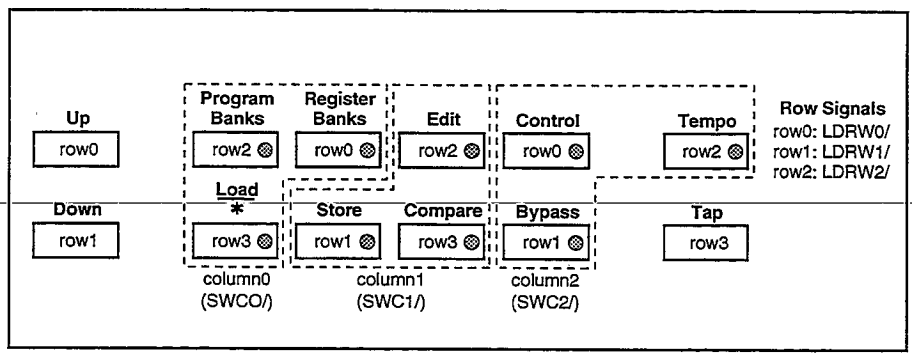
7	6	5	4	3	2	1	0
SWROW3	SWROW2	SWROW1	SWROW0	**SSNB**	**SSNA**	**ASNB**	**ASNA**

The encoded bits for the SELECTSoft Knob are SSNB and SSNA. The encoded bits for the ADJUST Soft Knob are ASNB and ASNA. As each knob is rotated clockwise, the sequence for each pair (SSNB:SSNA, and ASNB:ASNA) should be: LL, LH, HH, and HL, etc. in a rotating sequence. This can be observed at the inputs of the Soft Knobs Input Buffer (U43) pins 5 & 4, and 3 & 2 respectively.

Front Panel LEDs

Switch-Status LEDs

On the front-panel board, green LEDs are physically embedded in each of 9 switch button-caps. These LEDs are matrix-driven determined by 6 register bits consisting of 3 columns and 3 rows. The columns are the same as those that drive the switch columns (SWCOL<2:0>/). The LED matrix columns and rows are determined by 6 bits of a 74HC574 Octal Register (U42). During operation, each column should individually be asserted for 2ms of a 6ms period. Transistors Q9, Q10, and Q11 source the needed current for each column. R147, R149 and R151 pull down each column when any respective transistor is off. Any LED within a column can be lit by asserting the corresponding rows (LEDROW<2:0>/) (asserted-low). When LED(s) are on, peak current through R153, R154, and R155 should be about 20 mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The front panel switches and LEDs are arranged as shown below.



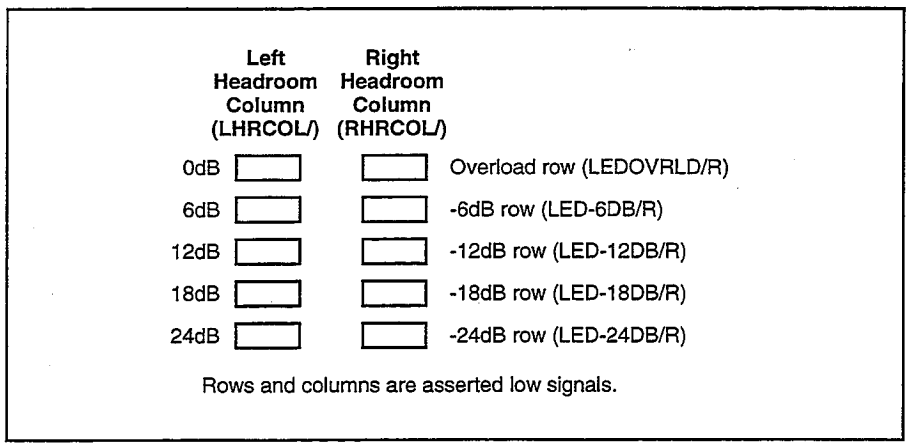
Status LED Column Grouping and Row Assignments

Switch/LEDs Matrix Register (I/O location = $000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	**LDRW2/**	**LDRW1/**	**LDRW0/**	**SWC2/**	**SWC1/**	**SWC0/**

Headroom Indicator LEDs

The Headroom LEDs are matrix-driven determined by 2 columns of 5 rows. The columns and rows are determined by 7 bits of a 74HC574 Octal Register (U29). During operation, each column should individually be asserted for 2ms of a 4ms period. The two columns are LHRCOL/ for the left input level, and RHRCOL/ for the right input level. Transistors Q7 and Q8 provide the necessary current to drive each column's LEDs. R84 and R86 pull down each column when its respective transistor is off. LEDs within a column can be lit by asserting the corresponding rows (LED-24DB/R, LED-18DB/R, LED-12DB/R, LED-6DB/R, LEDOVRL/R). When LED(s) are on, peak current through R87-91 should be about 10.4mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The headroom indicator LEDs are arranged as shown below.



Headroom Indicator LEDs

Column and row control bits are in the headroom LED register. They are summarized as follows:

HeadroomLED Register (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HIOUTLVL	**RHRCOL/**	**LHRCOL/**	**LEDOVRLD/**	**LED-6DDB/**	**LED-12DB**	**LED-18DB**	**LED-24DB**

Front Panel Display

The front panel alphanumeric display is a Futaba M202SD01HA, an intelligent vacuum fluorescent display module with 2 rows of 20 characters each. The module has its own display controller and is connected to the host system bus via an 8-bit data latch (U40). The display data write signal, DISPDWR/, is sourced from the I/O write decoder (74HC138 (U27)). It is inverted by a 74HC04 (U37) to be the latch signal DISPDWR for the 74HC573 (U40) which is the display data latch. When the signal is asserted,. data from the host (HD<7:0>) flows through to source the display connector, then the display. When the signal is de-asserted, the latch is closed, and data should be held. This provides proper hold time for the display. DISPDWR/ goes to the display directly. DISPBSY is a handshake signal that, when asserted high, indicates that the display is busy. When the signal is low, it indicates that the display is ready to accept the next character or command. DISPBSY is monitored by the host via Status Register 1 bit 7 (U24 pin 9).

Display Data Buffer Latch (I/O location = $000E Write-Only)

7	6	5	4	3	2	1	0
DISPD7	DISPD6	DISPD5	DISPD4	DISPD3	DISPD2	DISPD1	DISPD0

For more information, including the character set codes and cursor commands, see the Futaba Dot Matrix VFD Module M202SD01HA Instruction Manual.

Footpedal ADC

An Analog Devices ADC0804 (U23) performs 8-bit A-to-D conversion for the footpedal input. Note that this input (J11) can also be used as a footswitch input in addition to the dual footswitch input jack (J12).

Conversion is started by an I/O write to location $0090. Conversion data is ready after the ADCDONE/ is asserted low (Status Register 0 bit 7) (U20). Conversion data is read by an I/O read from location $0090. ADCEN/, the enable for both reads and writes, is sourced by a 74AC00 (U61) via a 91Ω series-terminating resistor.

Footswitches

The stereo 1/4" jack at J12 provides input for two footswitches. The primary switch should be wired from the tip to the sleeve. (This is the circuit that is used on a mono-plug footswitch.) The secondary switch should be wired from the ring to the sleeve. Each one can be normally-open or normally-closed. The two inputs can also accept a 0-5V voltage level. FB15, C143, FB17 and C167 provide RFI isolation of the footswitches to prevent any high frequency signals from entering or exit the box. R125 ,R163, D31, D32, D34, D33 provide current limiting and overvoltage protection. R124 and R161 pull the inputs high when the circuit is open. FOOTSWT and FOOTSWR and the respective signals that go to Status Register 0 bits 7 and 0 for host processor monitoring.

MIDI

The MIDI interface in the PCM 80 complies with the MIDI specification. MIDI is implemented using the on-chip serial port of the V40 with buffering between it and the rear-panel 5-pin DIN jacks (J13-J15).

MIDI IN is accepted from J15. A 6N138/139 provides opto-isolation to source the buffered MIDI signal MIDIIN. This buffered signal goes to the RxD input of the V40 (U46 pin 34).

The unbuffered MIDIOUT signal is sourced from the TxD output of the V40 (U46 pin 35). It is then buffered by a 74HC14 schmitt trigger inverter (U58) and a 2N3904 transistor (Q12) before going to the MIDI OUT jack (J13).

MIDI THRU is sourced by a 74HC14 (U58) and a 2N3904 transistor (Q13) which is a buffered version of the MIDI input (MIDIIN). The MIDI THRU output is provided at the rear panel via J14. W5 provides selection between normal MIDI THRU operation of J14, and a special test mode. For normal operation, W5 should have a jumper shunt on pins 1 and 2. For testing, the jumper may be put on 2 and 3 to have the MIDI THRU jack duplicate the function of the MIDI OUT jack.

Analog I/O (Host Control Interface)

The following describes analog I/O control signals from the host. For further information, see Analog Circuitry.

The signals ADCAL and DACRST/ are host control signals going to the A-to-D converter and to the digital filter of the D-to-A converter circuit respectively. ADCAL must be asserted during power-up to calibrate A/D. Likewise, ADCAL must be deasserted for normal A-to-D operation. Note that DACRST/ must be released low for proper operation of the digital filter chip of the D-to-A converter circuit. (When DACRST/ is asserted low, it will still pass audio, but not to specification.)

Control Register 1 (I/O location = $0001 Write-Only)

7	6	5	4	3	2	1	0
FIMTMSK/	DIOMSK/	LEDSEN	**ADCAL**	**DACRST/**	PRGINTP7	PRGINTP6	PRGINTP5

The MUTE/ signal when asserted (low) opens the analog output relays to prevent any audio glitches from reaching the analog outputs during power-up and power-down. Also, the MUTE/ signal, when asserted-low gates off analog input, analog output, and digital input serial streams. This gating is done by three sections of a 74HC08 AND gate (U47). When the MUTE/ signal is de-asserted (high), the analog output relay is closed, and the serial audio streams are enabled, allowing audio to pass through.

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	**MUTE/**	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

When the control signal HIOUTLVL is asserted (high), the +4 dBu setting for analog output level is selected. When HIOUTLVL is not asserted (low), the -10 dBu setting for analog output level is selected.

Headroom LED Register 1 (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HOOUTLVLRHRCOL/		LHRCOL/	LEDOVRLD/	LED-6DB	LED-12DB	LED-18DB	LED-24DB

Digital I/O

The host is responsible for managing the channel status of the Crystal Semiconductor CS8412 digital audio receiver, and the Crystal Semiconductor CS8402 digital audio transmitter. Status Register 2 and Control Register 2 contain bits to monitor and set channel status bits received and transmitted respectively. More details on Digital I/O are given later in this chapter.

System WordClock Source Selection

The user can select from among three different wordclocks (sample-rates): 44.1kHz, 48kHz and External. An 11.2896 MHz crystal (Y3) is used to derive the 44.1kHz wordclock, and a 12.2880 MHz crystal (Y2) is used to derive the 48.0kHz wordclock. (Both crystal circuits use a 74HCU04 (U56,U45) as crystal drivers operating the crystal in its parallel resonance mode.) An on-chip PLL on the CS8412 (U19) digital audio receiver is used to derive External wordclock.

The following table outlines the options for the wordclock source under host control. Note that appropriate digital I/O bits need to be set accordingly.

CTRL2<7> SRSSEL1	CTRL2<6> SRSSEL0	Wordclock Source
0	0	Internal 44.1kHz
0	1	Internal 48kHz
1	0	External Sync from Digital Input
1	1	Disabled (DC tied low)

A 74HC253 (U44) multiplexer controls selection of sources. The multiplexer's output is 256FS. A 74HC74 dual flip-flop (U31), two 74HC161 counters (U32,U33), and a 74HC175 quad flip-flop divide down 256FS to other various wordclock-dependent clock signals. The following is a summary of these clock signals and their functions:

256FS
Other Variations: PT256FS, 256FSA
Frequency: 256 x selected wordclock frequency (50% duty cycle) @44.1 KHz = 11.2896MHz; @48.0kHz = 12.2880MHz
Function: a. Goes to 74HC74 (U31) to divide clock down further.
b. Goes to CS5389 A/D (U7)as its master input clock.
c. Goes to DSP board connector (J17) for future functions.

128FS
Other Variations: PT128FS
Frequency: 128 x selected wordclock frequency (50% duty cycle) @44.1kHz: 5.6448MHz; @48.0kHz: 6.1440MHz

	Function:	a. Goes to 74HC74 (U31) to divide clock down further.
		b. Goes to CS8402 digital audio transmitter (U22) as its master clock.
64FS	Other Variations:	PT64FS, 64FSB, 64FS/, 64FSA (inverted)
	Frequency:	64 times the selected wordclock frequency (50% duty-cycle)
		@44.1kHz: 2.8224MHz; @48.0kHz: 3.0720MHz
	Function:	a. Goes to two 74HC161s (U33) and a 74HC175 (U30) to divide the clock down further.
		b. Goes to CS5389 A/D (U7), SM5813 digital filter (U12), and the Lexichip-2 (U19) on the DSP board via connector J17 for analog I/O audio data bit clocking.
		c. Goes to CS8412 digital audio receiver (U19) and CS8402 digital audio transmitter (U22) and the DSP56002 (U13) on the DSP board via connector J17 for digitial I/O audio data bit clocking.
AIOFRAME	Frequency:	2 times the selected wordclock frequency (High going pulse once every 32 64FS bit clocks.)
	Function:	Goes to the Lexichip-2 (U19) and DSP56002 (U13) on the DSP board to mark the start of a sample frame. (2 frames/Wordclock period.)
WC/	Other variations:	WCA/, CHSEL (inverted)
	Frequency:	User-selected Wordclock frequency of 44.1kHz, 48kHz, or External.
	Function:	a. The falling edge of WC/ (or the rising edge of CHSEL) denotes the beginning of a sample period.
		b. Goes to Lexichip-2 (U19) and DSP56002 (U13) on the DSP board via connector J17 to interrupt or reset the processors to the first instruction of the sample-period's instruction sequence.
		c. WC/ goes to the CS5389 A/D to indicate, when low, that the serial audio data frame corresponds to the right channel. Otherwise it corresponds to the left channel.
		d. CHSEL goes to the SM5813 digital filter to indicate, when high, that the serial audio data frame corresponds to the right channel. Otherwise it corresponds to the left channel.
TACOSWAP	Frequency:	1/2 that of the selected wordclock frequency.
	Function:	Swaps memory banks in the TACOCHIP (U12 on the DSP board) to swap data betwen the Lexichip and the DSP56002 buffers at the beginning of every wordclock period.

System Reset Circuitry

PCM 80 reset circuitry consists of four functional blocks, three of which join together and generate the Master Reset (MRST/) signal. The Watchdog Timer, the +5V Monitor, the reset delay circuitry and the Reset Register. The reset circuitry has no provision for early detection of power failure. Therefore, if the +5V Monitor detects less than 4.3V, the hardware will immediately force reset.

After a successful power on and a delay of approximately 0.75 sec., the Host CPU reset, the Reset Register reset, and the UART reset are released. The outputs of the Reset Register, except the Host Master Reset (HMRST), are left in an active state. It is, therefore, the responsibility of the software to release reset for other devices after the reset cycle. The Host can assert Host Master Reset, causing the Watchdog Timer circuitry to create a reset pulse to prevent reset latchup.

Watchdog Timer

The main component of the Watchdog timer circuitry is a Monostable Multivibrator, U14 (74HC4538). The HC4538 has a very well defined trigger input. They are all edge sensitive and have hysteresis. This design takes advantage of that and the retrigger capability of the multivibrator. Kicks from the Host ensure that the Q output of the first device stays high, provided that the kicks occur in shorter intervals than the pulse width. If a kick does not happen within the required time period, the first device will time out and its output will change state from high to low, triggering the second device, which will generate a pulse which will cause C104 to discharge, resetting the system. After the reset pulse disappears, C104 will start charging, as during the power on cycle. The output or the +5V Monitor is also connected to the second MMV, through an AND gate, to ensure an instant reset pulse when power is interrupted. The HMRST signal is connected to the second device's positive edge input, thereby triggering a reset pulse when HMRST is asserted.

As the Watchdog timer circuitry is inactive after power on until it is kicked, the software has to deliver the first kick to activate the timer.

+5V Monitor: The +5V monitor U16 (Motorola MC34164) is a Micropower Undervoltage Sensing Circuit which triggers at +4.33V (+5V increasing) and +4.27V (+5V decreasing). It has an Open Collector output. This device is used to control the Battery Backup and Reset circuitry. The combination of R71 and R72 is selected to ensure minimum U17 VIH when C104 is fully discharged and the +5V monitor's output transistor is turned off.

All control registers are initialized with their outputs in a low state. Control Register 0 contains all other sub-system resets including resets for the digitial I/O circuitry (DIORST/), and for the DSP56002 (56KRST/), Z80 (SLVRST/), and LEXICHIP-2 (LEXRST/) on the DSP board. HMRST is a control register bit which will, when set, reset the entire unit. When the unit is reset via HMRST, the control register itself will be cleared after a delay.

Other initialization related control bits include FRCMOD and MUTE/. FRCMOD must be set when the 56KRST/ line is released high to put the DSP56002 into its proper mode of operation (Mode 5). FRCMOD must be released after reset to allow proper interrupt operation to the DSP56002. MUTE/, like the other control bits, powers up in the low state. This enables all muting circuitry, including holding the audio output relays in an open state. The MUTE/ signal, when asserted, isolates the outputs (both digital and analog) from any power-on/power-off glitches.

The following summarizes the bits involved reset and initialization in Control Register 0:

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	MUTE/	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

Status Bits Summary

Host Status Register 0 (I/O location = $0008 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	SINGOUT/	CWRPROT	CARDDET/	CARDBVD2	CARDBVD1	spare	FOOSWR

FOOTSWT	Footswitch Jack Tip Input Level.
SINGOUT/	Single Analog Output Jack Status.
CWRPROT	PCMCIA Card Write Protect.
CARDDET/	PCMCIA Card Detect (Asserted-Low).
CARDBVD2	PCMCIA Card Battery Voltage Detect Bit 2
CARDBVD1	PCMCIA Card Battery Voltage Detect Bit 1
FOOTSWR	Footswitch Jack Ring Input Level

Host Status Register 1 (I/O location = $0002 Read-Only)

7	6	5	4	3	2	1	0
DISPBSY	HTC/	BATLOW	LEXOVRL/	LEXOVRL/	FPLOCK/	56KINT	SHINT

DISPBSY	Front-Panel Display Busy Flag.
HTC/	DMA Transaction Complete Signal. [This status bit is non-functional]
BATLOW	Battery-Low Condition for Non-Volatile SRAM.
LEXOVRL/	Lexichip Overload Bit (Asserted-Low)
56KOVRL/	DSP56002 Overload Bit (Asserted-Low)
FPLOCK/	DSP56002 PLL Lock Condition (Asserted-Low)
56KINT	DSP56002 Interrupt.
SHINT	Slave (Z80) to Host Interrupt.

Host Status Register 2 (I/O location = $0006 Read-Only)

7	6	5	4	3	2	1	0
ADCDONE/	ERF	F2/IGC	FI/ORG	F0/C3/	E2/C2/	E1/C1/	E0/C0/

ADCDONE/	Footpedal ADC done. (Asserted-low)

The following bits are explained in more detail in the Digital I/O Receiver section.

ERF	Digital I/O Receiver Error Flag.
F2/IGC	Digital I/O Receiver Frequency Reporting Bit 2/ Ignorant Category Bit.
F1/ORG	Digital I/O Receiver Frequency Reporting Bit 1/ Original Bit
F0/C3/	Digital I/O Receiver Frequecy Reporting Bit 0 / CS3/
E2/C2/	Digital I/O Receiver Error Condition Bit 2 (asserted high)/ CS2/ (asserted low)
E1/C1/	Digital I/O Receiver Error Condition Bit 1 (asserted high)/ CS2/ (asserted low)
E0/C0/	Digital I/O Receiver Error Condition Bit 0 (asserted high / CS2/ (asserted low)

Control Bits Summary

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	MUTE/	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

HMRST	Host Master Reset.
OUTVLD	Digital Output Valid Bit.
MUTE/	Mute Analog I/O (asserted low)
DIORST/	Digital I/O Circuitry Reset (asserted low)
FRCMOD	Force DSP56002 Mode (during 56KRST/ release) (asserted high)
56KRST/	DSP56002 Reset (asserted low)
LEXRST/	Lexichip-2 Reset (asserted low)
SLVRST/	Slave Z80 Reset (asserted low)

Control Register 1 (I/O location = $0002 Write-Only)

7	6	5	4	3	2	1	0
FINTMSK/	DIOIMSK/	LEDSEN	ADCAL	DACRST/	PRGINTP7	PRGINTP6	PRTGINTP5

FINTMSK/	DSP56002 Interrupt Mask (Asserted-Low)
DIOIMSK/	Digitial Input Interrupt Mask
LEDSEN	Front-Panel LEDs enable
ADCAL	A-to-D Converter Calibrate
DACRST/	D-to-A Converter Reset (asserted low)
PRGINTP7	Programmable Interrupt Priority 7
PRGINTP6	Programmable Interrupt Priority 6
PRGINTP5	Programmable Interrupt Priority 5

Control Register 2 (I/O location = $0004 Write-Only)

7	6	5	4	3	2	1	0
SRSSEL1	SRSSEL0	DIOCSSEL	OUTCS15/	OUTCS3/	OUTCS2/	FC1	FC0

The following bits are explained in more detail later in this section.

SRSSEL1:0	Wordclock Source Selection Bits 1:0
DIOCSSEL	Digital I/O Receiver Channel Status Select.
OUTCS15/	Digital I/O Transmitter Channel Status Bit 15 Output (asserted low)
OUTCS3/	Digital I/O Transmitter Channel Status Bit 3 Output (asserted low)
OUTCS2/	Digital I/O Transmitter Channel Status Bit 2 Output (asserted low)
FC1:0	Digital I/O Transmitter Frequency Control Bits 1:0.

Control Register 3 (I/O location = $0006 Write-Only)

7	6	5	4	3	2	1	0
CREG/	DISCARD/	FLASHVEN	spare	CA19	CA18	CA17	CA16

CREG/	PCMCIA Register Select (Asserted-Low)
DISCARD/	Disable PCMCIA Card Drivers (Asserted-Low)
FLASHVEN	Flash ROM VPP Enable
CA<19:16>	PCMCIA Card Address <19:16> (Page Address)

DSP Board Circuitry

The PCM 80's DSP board is Lexicon's proprietary digital signal processing module. With the exception of the SIMM expansion memory, it does not contain any servicable parts. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair.

DSP56002 Audio DRAM

In addition to the DSP56002's internal RAM, SIMM sockets are provided for expansion audio. The default, on-board 256Kx18-bits DRAM (HM5143280/ uPD42480, U2) may be used, or installable SIMM memory modules (J1, J2) may be used to boost the audio memory to 1MBx18, 4MBx18, or 16MBx18. Upgrading DRAM size may be desirable for applications such as sampling. Note that, when enabled, expansion memory does not add to, but replaces on-board memory.

To select the on-board memory, W1 must have its jumper shunt between pins 2 and 3 (only). To enable SIMM memory instead, W1 must have its jumper shunt between pins 1 and 2 (only). W1 selects to which memory the RAS/ DRAM control line goes. When one line is not connected, R2 and R1 provide pull-up to disable the respective RAS/ line.

Expansion Memory Requirements: 1MBx9, 4MBx9, or 16MBx9 30-pin SIMMs. Modules must be "true parity" (9-bit) type, *not* logical parity (8-bit +parity generator).

Digital I/O

The digital I/O circuit implements the S/PDIF digital audio I/O interface via rear panel RCA jacks. One jack provides S/PDIF Digital Input (J10-White), and the other S/PDIF Digital Output (J10-Red). The circuit features two Crystal Semiconductor ASICs: the CS8412 digital audio receiver (U19), and the CS8402 digital audio transmitter (U22).

Digital Audio Receiver Circuit

A Crystal Semiconductor CS8412 (U19) is used to implement the digital audio receiver. It is a monolithic CMOS circuit that receives and decodes digtal audio data which has been encoded according to AES/EBU/EIAJ CP-340 consumer format interface standards. It contains a RS422 differential line receiver, data recovery logic, and a clock recovery circuit that utilizes an on-chip phase-locked loop.

S/PDIF input is accepted by J10 and is RFI isolated by C130. A 1:5 transformer (TX2) is used for DC isolation and also to boost the input signal by a factor of five. R110 is used to provide the proper input impedance of 75Ω (374/5=75) to the input. It also provides the differential voltage to the CS8412 RS422 inputs via C127 and C128. Decode of S/PDIF input format, which is biphase encoded, is provided by the CS8412. The resulting audio data is output by the SDATA pin in a synchronous serial format. 64FSB is the serial bit clock with WCA/ that provides the audio channel framing.

The CS8412 locks onto the frequency of the incoming S/PDIF signal with its internal PLL. R93 and C112 provide the external glue for the PLL Filter. C110, C111, and R92 provide power supply isolation and bypass capacitance for the CS8412's PLL circuitry and other analog circuitry. The output of the PLL, the MCK pin, sources the signal 256FSPLL. When external lock is selected by the 74HC253 Multiplexer (U44), this serves as a master clock for all digital audio clocking. This clock has 256 pulses per wordclock period.

The CS8412 has individual output pins for the more popular channel status bits. The function of Host Status Register 2 bits 5:0 is determined by DIOCSSEL (Control Register 2 bit 5). If DIOCSSEL is high, Status Register 2 bits 5:0 are channel status bits. When DIOCSSEL is high DIOCSSEL/ should be low clearing the output of the 74HC74 (U35) that sources the CS12 pin of the CS8412. This ensures that the channel status corresponds to sub-frame 1 (as opposed to sub-frame 2). If DIOCSSEL is low, those bits become Error Condition and Frequency Reporting bits. In either case, Status Register 2 bit 6 indicates an digital audio receiver error condition detected by the CS8412. This is outlined in the following table:

Host Status Bit	DICSSEL		Function
STAT2<0>	0	E0	Error Condition bit 0
STAT2<1>	0	E1	Error Condition bit 1
STAT2<2>	0	E2	Error Condition bit 2
STAT2<3>	0	F0	Frequency Reporting bit 0
STAT2<4>	0	F1	Frequency Reporting bit 1
STAT2<5>	0	F2	Frequency Reporting bit 2
STAT2<6>	X	Error Flag	
STAT2<0>	1	C0/	Professional Flag (asserted low) (should be high)
STAT2<1>	1	C1/	Non Audio (asserted low)
STAT2<2>	1	C2/	Copy Inhibit (asserted low)
STAT2<3>	1	C3	Emphasis (asserted low)
STAT2<4>	1	ORIG	Channel Status Encoding indicating Original
STAT2<5>	1	IGCAT	Ignorant Category Channel Status Encoding

DIOCSSEL/, when asserted low, gates GTREFCLK low to the CS12 pin of the CS8412 so that sub-frame 1's channel status is output from the channel status pins.

The Error Flag signal is gated by the Digital I/O Interrupt Mask (DIOIMSK/) with a 74HC08 AND gate (U47). The signal, after being buffered by a 74HC32 OR gate (U34), sources the V40's Non-Maskable Interrupt (HNMI). (The other input to U34 should always be low.) When DIOIMSK/ is high, ERF can trigger the V40's NMI. At that time, the type of error condition can be determined by reading the Error Decode bits. (When doing so, DIOCSSEL, Control Register 2 bit 5, must be set low.) When an error occurs, the corresponding error decode is latched. Since only one error can be indicated at any given time, there is a priority associated with each error code. Validity has the lowest priority while No-Lock has the highest priority. The error code is cleared by bringing the SEL pin of the CS8412 (U19) high for more than eight MCK cycles. From the V40's perspective, this is done by keeping DICSSEL high for 12 T-states or 3 instructions cycles. The following table describes the error conditions:

E2	E1	E0	Error	Comments
0	0	0	No Error	
0	0	1	Validity Bit High	Validity bit for a previous sample was high since the last clearing of the error codes
0	1	0	Confidence Flag	The received data eye opening is less than half a bit period, indicating a poor transmission link
0	1	1	Slipped Sample	A stereo sample has been dropped or re-read due to differences in internal vs. external sample rates
1	0	0	CRC Error (Pro only)	N/A
1	0	1	Parity Error	Incoming sub-frame does not have even parity as specified by digital audio interface standards
1	1	0	Biphase Coding Error	Biphase coding violation occurred
1	1	1	No Lock	PLL is not locked on incoming data stream. Lock is lost after not receiving 4 consecutive frame preambles

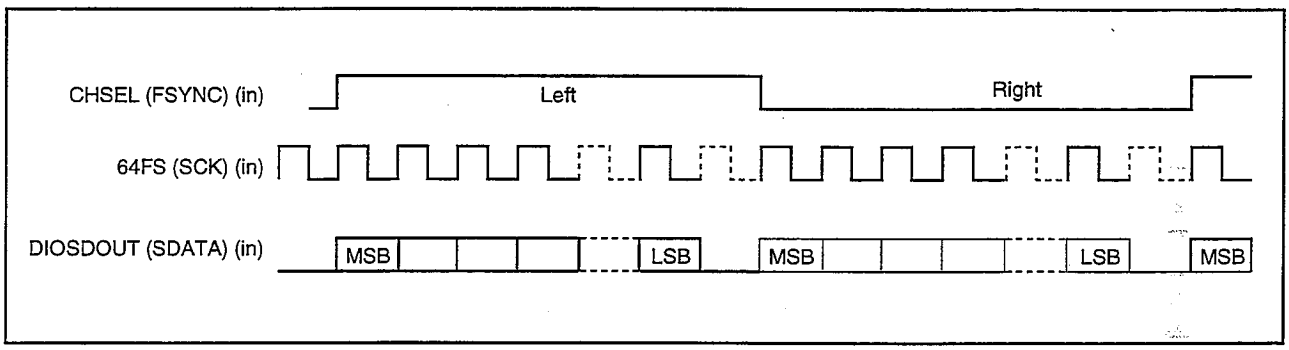
The frequency reporting bits are status bits from the CS8412 (U19) that indicate the sample rate of the incoming digital input. When digital input is selected, the system sample-rate should lock to the sample-rate of the incoming signal. In this case, one of three sample-rates is supported: 44.056kHz, 44.1kHz and 48kHz. (32kHz is accepted and will be locked to, but none of the DSP algorithms support it.) The frequency reporting bits' status is the result of a measurement by an internal circuit that uses a 6.144MHz clock as a reference. This reference is supplied by a 74HC74 (U35) that divides down the output of the 12.288 MHz crystal oscillator circuit. If all three frequency reporting bits are zero, it indicates that the incoming sample-rate is out-of-range. Note that the No-Lock condition, indicated by the Error Decoding bits, is a separate condition from being out-of-range. In either case, audio is muted. The CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition. To meet the Level 2 (Normal Accuracy Mode) specification, of the EIAJ CP-340 standard, only the 400 ppm tolerance is acceptable. Otherwise, the PCM 80 should be considered out-of-lock or going-out-of-lock. The decoding of the frequency reporting bits are summarized in the following table:

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz +4%
0	1	0	44.1kHz +4%
0	1	1	32kHz +-4%
1	0	0	48kHz +-400ppm
1	0	1	44.1kHz +-400ppm
1	1	0	44.056kHz +-400ppm
1	1	1	32kHz +-400ppm

Digital Audio Transmitter Circuit

A Crystal Semiconductor CS8402 (U22) is used to implement the digital audio transmitter. The CS8402 accepts 24-bit serial audio data (DIOSDOUT) from the DSP56002 on the DSP board. The audio data is then encoded with parity into a biphase-mark bit stream which is driven out through an RS422 line driver. At the output, R89 and R99 provide the proper output impedance of 75Ω. There is provision for an optional 1:1 output transformer at location TX1. Terminals DO+ and DO- are provided to feed a floating jack if transformer isolation is desired. (In which case, the DO- connection to ground should be cut.) The serial input to the CS8402 is hard-wired to Format 1. Format 1 is outlined as follows:

1. Has a sync signal FSYNC input which is high for the entire left frame, and low for the entire right frame.
2. Serial data is MSB first
3. Data is sampled on the falling edge of the serial bit clock pin SCK. (Which is 64FS.)



CS8402 Audio Serial Port Format

The CS8402 outputs the appropriate channel status depending on the host V40's setting of Control Register 2 bits 4:0. DICSSEL (Control Register 2 bit 5) determines the function of the Status Register 2 bits 5:0.

Digital Audio Transmitter Control Bits

Host Control Bit	Function	
CTRL2<0>	FC0	Frequency Control bit 0
CTRL2<1>	FC1	Frequency Control bit 1
CTRL2<2>	CS2/	Copy Inhibit Out (asserted low)
CTRL2<3>	CS3/	Emphasis Out (asserted low)
CTRL2<4>	C15	Generation Status (asserted low)
CTRL2<5>	DICSSEL	Digital Input Channel Status Multiplexer Select

There are two sets of control bits that specify sample-rate: the Frequency Control bits (FC<1:0>), and the Wordclock Select Bits (SRCSEL<1:0>). The Frequency Control bits set the appropriate channel status corresponding to the system sample-rate to be output from the digital output. Note that these bits are only to set channel status, *not* the actual sample-rate. Selecting the system sample-rate is done with the wordclock source select bits: SRCSEL<1:0> (Control Register 2 bits 7:6). The two sets of bits, however, should be consistent. Software sets the appropriate bits depending on whether an internal sample-rate or an external sample-rate reference is used, and depending also on which sample-rate is selected or detected. The following two tables outline the function of the Frequency Control Bits, and the Wordclock Source Select Bits.

Digital Output Sample Frequency Encoding

FC1	FC0	Function	CS24	CS25
0	0	44.1kHz Encoding for Channel Status Output	0	0
0	1	48kHz Encoding for Channel Status Output	0	1
1	0	32kHz Encoding for Channel Status Output*	1	1
1	1	44.1kHz Encoding for CS Output, CD Mode*	0	0

*Not supported

System Wordclock Source Selection

CTRL2<7> SRSSEL1	CTRL2<6> SRSSEL0	Wordclock Source
0	0	Internal 44.1kHz
0	1	Internal 48kHz
1	0	External Sync from Digital Input
1	1	Disabled (DC tied low)

CS8402 is reset by the host control bit DIORST/. This signal is asserted low on power-up and, therefore, will not pass through audio until the host releases this signal after DSP code is loaded. In that case, the CS8402's internal transmit timing counters are not enabled until eight and one-half 64FS clocks after the first active edge of FSYNC after DIORST/ is released. On a power-fail condition (which happens on power-down and brown-out conditions), DIORST/ should be asserted. When DIORST/ is asserted, the differential line drivers of the CS8402 are set to ground. Though this cuts off the digital output mid-stream, it should not send speaker-damaging signals to the box receiving the PCM 80's digital output. It is up to the receiving box to handle a lost digital input gracefully. (In the PCM 80, the CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition.)

Analog Circuitry

Analog Inputs

Two 1/4 inch tip/ring/sleeve phone jacks (J1,2) are provided for balanced or unbalanced sources. A balanced signal may be applied across the tip and ring, whereas an unbalanced source will ground the ring automatically when using a tip/sleeve plug. The jacks are wired to insure a balanced or an unbalanced mono signal will be applied to both left and right channels from either input. 150 pF ceramic disk caps and ferrite beads are included for RFI suppression.

Input Amplifier

A dual op amp (U1) provides the required gain and buffering for each analog source. A 4-pole double-throw switch (SW1), located on the rear panel, reconfigures the input stage from a balanced input with 0dB gain to an unbalanced non-inverting stage with 20dB of gain. 49.9 kΩ, 1% resistors are used to insure 100 kΩ input impedance and 40 dB of common mode rejection in balanced mode. Nonpolar 10 uF capacitors block any DC bias on the incoming signals from affecting the performance of the input stage. Overvoltage protection for the op amp is provided by the series 100 ohm resistors and 1N4148 diodes.

The outputs of the input amplifiers go through another set of DC blocking caps before going to the input level pot (R201) on a separate PC board. The caps serve to prevent any DC offset due to the op amps' bias currents from affecting the quietness of the level pot or introducing bias in the A to D conversion.

A/D Conversion

After the input level pot, the left and right signals return to the main board and encounter series 470Ω resistors. These resistors, in conjuction with 1N4148 diodes, limit the signal amplitude to ±5 volts. Two dual op amps (U5,6) perform the signal preconditioning and provide the low output impedance required by the A/D converter. These op amps operate off ±5 volt rails to insure signal levels do not exceed the maximum specified for the converter.

Each signal passes through non-inverting amplifiers with 12dB of gain. In addition, unity gain inverting amplifiers help create the balanced signal required by the A/D converter. Each op amp stage is bandwidth limited to 320kHz. These outputs drive a one-pole low pass filter to limit aliasing during conversion.

Conversion is performed by a stereo monolithic 18-bit Delta-Sigma CS5389 A/D converter (U7). This device uses a single-bit sampler operating at 64x the sample rate (oversampling) and a 5th-order noise shaping filter. This filter pushes the granularity noise beyond the audio spectrum. A digital decimation filter removes this high frequency noise and reduces the word rate to 18 bits. A differential architecture on the converter's front-end improves noise rejection.

The CS5389 has a serial data interface which requires a master clock (256FSA), bit clock (64FSA), and left/right framing signal (WCA/). Data (AIOSDIN) is MSB first, and is located at the beginning of each frame. Sample rates of 44.1kHz and 48kHz are supported. An active-high, calibration signal (ADCAL) is asserted during power up and whenever the sample rate is changed. This initializes the converter's calibration cycle. Data from the converter is discarded for the first 100ms after ADCAL goes low due to the calibration process

D/A Conversion

Digital-to-analog conversion tasks are shared by an 8x oversampling digital filter (U12) and 18-bit AD1865 stereo DAC (U11). The digital filter performs noise shaping and linear interpolation on the incoming audio data by incorporating three FIR filters. The 8x upsampled data for the left and right audio channels is passed to the DAC simultaneously to eliminate phase skew.

The digital filter accepts 16-bit data in a serial format and requires a master clock (256FSA), bit clock (64FSA), and left/right framing signal (CHSEL). Data (AIOSDOUT) is MSB first, and, unlike the A/D converter, is located at the end of each frame. Note that the framing signals, CHSEL and WCA/, are out of phase for the D/A and A/D conversions, respectively, in order to maintain the proper phase relationships with either analog or digital audio sources. Reset (DACRST/) is asserted low during power cycling.

The digital filter outputs two 18-bit words via the DAC's serial port. A bit block (BCKO), framing signal (WCKO) and left (DOL) and right (DOR) audio data are provided by the digital filter's serial interface. Here the data is MSB first and shifted out at the beginning of each frame.

Two trimpots (R52, R54) are provided for adjusting the MSB which permits optimization of low level THD performance. A description on how to perform this adjustment is given in the Performance Verification section of this manual. Low order high pass filtering is provided by the 100 pF capacitors in the DAC's internal op amps' feedback loop. The 10 uF series capacitors block any DC offsets created by any DSP algorithms.

Output Filtering

The DAC output signals pass through low pass filters, composed of a dual op amp (U10) and its associated components. A 3rd-order, non-inverting Butterworth filter topology with 6dB of gain and -3dB point at 50kHz is used to maintain a flat response in the audio bandwidth. This circuitry attenuates the image found at 8x above the sampling frequency.

Output Level Switching

Two J108 FETs (Q15 and Q17) provide the ability to attenuate the output signals by 14dB. The FETs act like switches which activate voltage dividers (R191, R193, R186 and R185) by shorting R193 and R185 to ground. The impedance of these resistors, combined with the FETs on-resistance, determine the amount of attenuation.

The FETs are controlled by a 2N3906 transistor (Q16). When HIOUTLVL is high, Q16 turns off. A negative voltage is applied to the gates of the FETs through R188, which turns the FETs off. A high impedance develops across each FET, which, when applied in series with R193 and R185, does not decrease the analog signal levels. However, with HIOUTLVL low, Q16 turns on. A small positive voltage is applied to each gate by the voltage divider R197 and R188, thereby turning the FETs on. This action shorts R193 and R185 to ground, which attenuates the analog signals prior to each output stage.

Balanced Output Amplifiers

Two SSM2142 balanced line drivers are employed as output amplifiers (U8,9). These devices have an internal gain of 6dB, which is maintained when driving single-ended loads, as long as the unused output is shorted to ground. 10Ω resistors and 4.7 uF tantalum capacitors reduce noise induced by ripple in the supply rails. 150 pF and 47 uF non-polar capacitors help eliminate DC offsets and increase AC noise rejection. 1N4148 diodes and series 75Ω resistors provide overvoltage protection.

Analog Outputs

Two 1/4 inch tip/ring/sleeve phone jacks (J5,6) can accommodate balanced and unbalanced configurations. Ferrite beads and 150 pF ceramic disk caps are included for RFI suppression.

The left and right analog output signals are mono-summed in the DSP domain when the SINGOUT/ signal is enabled (active low). SINGOUT/ is disabled only when phone plugs are inserted into both analog output jacks. Because the jacks are wired for AND logic, inserting a single plug into either jack automatically changes the output signal to mono.

Output muting is accomplished by miniature relays (RY1,2) controlled by MUTE/. When MUTE/ is low, Q1 turns off, breaking the current path to the relay coils, thereby shorting the analog outputs to ground. Likewise, when MUTE/ is high, Q1 turns on, activating the relays and connecting the stereo output signals to the output jacks.

Power Supply

A universal input switching power supply supplies all needed voltages. It operates over an input range of 85 to 265 VAC, 50-60Hz and produces three output voltages: +5 VDC @ 5 Amps, +15 VDC @ 2 Amps and -15 VDC @ 0.5 Amps. The +5 volt supply is used for all the digital circuitry while the ±15 volt supplies are required for the analog circuitry and converters.

The AC voltage is connected by a 2-pin connector located toward the rear of the unit. A 6-pin connector at the opposite end of the supply accommodates the DC output voltages and returns. A cable assembly brings the supply voltages over to the main board. +5 VDC and digital ground connections to the main board are made near the power supply, while the ±15 VDC and analog ground connect near the analog I/O jacks.

The power supply is not field serviceable. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair. A 1.5 Amp Slo Blo fuse is incorporated on the module's AC input side. Always replace with a fuse of identical rating.

Analog Power Distribution

The ±15 VDC rails pass through a π filter to reduce high frequency noise before they are distributed to any analog circuitry. After this filter, the ±15VA rails go to the appropriate components, including three voltage regulators. Two voltage regulators (U2,3) are used to produce ±5VA for the op amps that drive the A/D converter's analog inputs as well as the analog supplies required by the A/D and D/A converters. A third regulator (U4) generates +5VP, which is needed for the A/D and D/A converters' digital supply.

Digital Power Distribution

+5VDC is supplied pre-regulated to all digital circuitry on the host board (including the DSP board connector) via J18. C180 and C184 serve as low-frequency bypass capacitors, and C181 serves as a high-frequency bypass capacitor local to the power-supply connection. A few dozen other high-frequency bypass capacitors (.01 uF and .1 uF) are scattered through the digital circuitry.

Signal Names

2FS	Digital Audio Clock (2x Wordclock)
16FS	Digital Audio Clock (16x Wordclock).
64FS	Digital Audio Clock (64x Wordclock)
64FSA	Analog Clock (64x Wordclock)
128FS	Digital Audio Clock (128x Wordclock)
256FS	Digital Audio Clock (256x Wordclock)
256FSA	Analog Clock (256x Wordclock)
256FS48	Wordclock Oscillator Ouput for 48 kHz sampling rate
256FS441	Wordclock Oscillator Output for 44.1 kHz sampling rate
56KINT	Interrupt from DSP56002
56KOVRL/	DSP56002 Interrupt from DSP to host
56KRST/	DSP56002 Reset Line
-15VA	-15 Volts Analog
-5VA	-5 Volts Analog
+5VA	+5 Volts Analog
+5VD	+5 Volts Digital
+5VP	+5 Volts Post-regulated
+15VA	+15 Volts Analog
+15VDU	+15 Volts Digital Unfiltered
ADCAL	ADC Calibration Enable
ADCDONE/	Footpedal ADC Conversion Done Signal
ADCEN/	Foot Controller ADC Enable
AIOFRAME	Analog I/O Framing Signal
AIOSDIN	Analog I/O Serial Data Input
AIOSDOUT	Analog I/O Serial Data Output
ASNA	Adjust Soft Knob A
ASNB	Adjust Soft Knob B
BATLOW	Battery Low Signal
BFREGEN/	I/O Buffer/Register Enable
BVD<2:1>	PCMCIA Battery Voltage Status
CA<19:0>	PCMCIA Card Address
CARDBUS	PCMCIA Card Bus
CARDDET/	Card Detection
CARDEN/	PCMCIA Card Slot Enable
CARDENB/	Buffered Card Enable
CD<7:0>	PCMCIA Card Data
CDET1/	PCMCIA Card Detect 1
CDET2/	PCMCIA Card Detect 2
CE1/	PCMCIA Card Enable 1
CE2/	PCMCIA Card Enable 2
CLOVRL/	Clear Lexichip Overload Line
CHSEL	Channel Select (1x Wordclock)
COE/	PCMCIA Card Output Enable
CSHINT/	Clear Slave-to-Host Interrupt
CTRL3..0WR/	Control Register 3 thru 0 Write Enable
CVCC	PCMCIA Card Vcc
CVCCVPP	PCMCIA Card Vcc / Vpp
CWE/	PCMCIA Card Write Enable
CWP	PCMCIA Card Write Protect
CWRPROT	PCMCIA Card Write Protect
DACRST/	DAC Reset
DIOCSSEL/	Digital I/O Channel Status Select
DIOIMSK/	Digital I/O Interrupt Mask
DIOINT	Digital I/O Interrupt
DIOREFCLK/	Digital Input Reference Clock
DIOSDIN	Digital I/O Serial Data Input
DIOSDOUT	Digital I/O Serial Data Output
DISCARD	Disable PCMCIA Card
DISIGN	Digital Input (-)
DISIGP	Digital Input (+)

DISPBSY	Display Busy
DISPD<7:0>	Display Data Bus
DISPDWR	Display Data Write
DISPDWR/	Display Data Write Enable
DISPTST/	Display Test Mode
DMEMOP/	DRAM Memory Operation
DOSIGP	Digital Output
DSPHEN/	DSP Host Enable
DSPINT	DSP Interrupt
ECHSEL	Early Channel Select
ERF	Digital Input Error Flag
E0/C0/	Error/Channel Status Bit 0
E1/C1/	Error/Channel Status Bit 1
E2/C2/	Error/Channel Status Bit 2
FC<1:0>	Digital Output Frequency Control Status Bits
FINTMSK/	DSP56002 Interrupt Mask
FOOTSWT	Footswitch Jack Tip Input
FPASNA	Front-Panel Adjust Soft Knob A
FPASNB	Front-Panel Adjust Soft Knob B
FPDRNG	Footpedal Jack Ring Input
FPDTIP	Footpedal Jack Tip Input
FPLOCK/	DSP56002 PLL Lock Status
FPINT	Front Panel Interrupt
FPSSNA	Front-Panel Select Soft Knob A
FPSSNB	Front-Panel Select Soft Knob B
FRCMOD	DSP56002 Force Mode Line
FSDIV2	Wordclock ÷ 2
F0/C3/	Digital Input Frequency Reporting Bit 0 / Channel Status Bit 3
F1/ORG	Digital Input Frequency Reporting Bit 1 / Original Bit
F2/IGC	Digital Input Frequency Reporting Bit 2 / Ignorant Catagory
GTAIOSDIN	Gated AIOSDIN
GTREFCLK	Gate Digital Input Reference Clock
HA<19:0>	Host Address Bus
HACK/	Host DMA Acknowledge
HAD<7:0>	Host Multiplexed Address/Data Lines
HASTB	Host Address Strobe
HASTBQ	Clock-Delayed version of HASTB
HAUB<19:12>	Unbuffered Host Address Lines
HBEN/	Host Bus Enable
HBR/W	Host Bus Read-Not Write
HBS<2:0>	Host Bus Status
HBSQ0	Clock-Delayed Host Bus Status 0
HBSQQ0	Double Clock-Delayed Host Bus Status 0
HBW/R	Host Bus Write Enable (Asserted Low)
HBW/RQ	Clock Delayed version of Host Bus Write-Not Read
HCAS/	Host DRAM Column Address Strobe
HCLK	Host Clock
HD<7:0>	Host Data Bus
HDRA<9:0>	Host DRAM Address Lines
HIORD/	Host IO Read Enable
HIOUTLVL	High Output Level Enable
HIOWR/	Host IO Write Enable
HIOWRQ/	Clock-Delayed version of HCB-HIOWR/.
HIOWRQQ/	Double Clock-Delayed version of HCB-HIOWR/
HMRD/	Host Memory Read
HMRDQ/	Clock-Delayed version of HCB-HMRD/
HMRD2Q	Double Clock-Delayed version of HCB-HMRD
HMRD3Q	Triple Clock-Delayed Host Memory Read

HMRST	Host Master Reset Control Bit
HMWR/	Host Memory Write
HNMI	Host Non-Maskable Interrupt
HRAS/	Host DRAM Row Address Strobe
HREFREQ/	Host Refresh Request
HREQ	Host DMA Request Line
HREQQ	Host DMA Request
HRLEDWR/	Headroom LEDs Write Enable
HROMEN/	Host ROM Enable
HSTSLVCB	Host-Slave Control Bus
HST56KCB	Host-DSP56002 Control Bus
HTC/	Host DMA Transaction Complete
HWAIT/	Host Wait Enable
HX2..1	Host Crystal Oscillator Signals
INLVL+	Footpedal ADC Input Level
LARWR/	LEDs Row and Column / Switch Column Register Write Enable.
LED-6DB/	Headroom LED -6dB Row Line
LED-12DB/	Headroom LED -12dB Row Line
LED-18DB/	Headroom LED -18dB Row Line
LED-24DB/	Headroom LED -24dB Row Line
LEDOVRLD/	Headroom LED Overload Row Line
LEXRST/	Lexichip Reset
LHRCOL	Left Headroom Column Strobe
LEDROW<2:0>/	LED Row Lines
LEDSEN	LED Buffers Enable
LEXOVRL/	Lexichip Overload Bit
LIN	Left Analog Audio Input (post level control)
LOGICHI	LogicHigh
LOGICLO	Logic Low
LOUT	Left Analog Audio Output (from DAC)
LOVLDP/	Lexichip Overload Pulse
LWAITY/	Lexichip Wait Line
MAPINSRAM	Map In SRAM.
MIDIIN	MIDI Input Serial Data
MIDIINTHRU	Buffered MIDI Input for MIDI THRU
MIDIOUT	MIDI Output Serial Data
MIDITHOUT	MIDI Output for THRU Jack Testing
MIDITHRU	MIDI THRU
MUTE/	Analog Output Mute
NVRAMEN	Non-Volatile RAM Enable

OUTCS<15,3,2>	Output Channel Status Bits 15, 3 and 2
OUTVLD	Digital Output Validity Bit
PGAIOSDOUT	Pre-Gated AIOSDOUT
PGDIOSDOUT	Pre-Gated DIOSDOUT
PREBCWE/	Pre-Buffered Version of Card Write Enable
PRGINT7..5	Programmable Interrupts 7 thru 0
PT64FS	Pre-terminated 64FS
PT128FS	Pre-terminated 128FS
PT256FS	Pre-terminated 256FS
PTHCLK	Pre-terminated version of HCB-HCLK
PTHDRA<9:0>	Pre-terminated DRAM Address Lines
PTHIORD/	Pre-terminated version of HCB-HIORD/
PTHIOWR	Pre-terminated version of HCB-HIOWR/
PTHMRD/	Pre-terminated version of HCB-HMRD/
PTSELCA	Pre-terminated version of Select Column Address
PTWC/	Pre-terminated Wordclock
PWR_OK	Power OK
QNVRAMEN/	Qualify Non-Volatile RAM Enable
RHRCOL	Right Headroom Column Strobe
RIN	Right Analog Audio Input (post level control)
ROUT	Right Analog Audio Output (from DAC)
SBUSEN/	Slave Bus Enable
SHINT	Slave-to-Host Interrupt
SHSINT/	Set Slave-to-Host Interrupt
SINGOUT/	Single Analog Output Enable
SLVRST/	Slave Reset
SPDIFIN	SPDIF Digital Input
SPDIFOUT	SPDIF Digital Output
SRSSEL<1:0>	Wordclock Source Select Lines
SSNA	Select Soft Knob A
SSNB	Select Soft Knob B
STAT2..0RD/	Status Register Read Enable 2 thru 0
SWCOL<2:0>	Switch Column Strobe Bits
SWROW<3:0>	Switch Row 3 thru 0
TACOSWAP	Tacochip Swap Signal
VRAM	Non-Volatile SRAM Power
VREFADC	Footpedal ADC Voltage Reference
WCA/	Analog Wordclock
WDKICK/	Watchdog Timer Kick

Parts List

DSP BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
ASSEMBLED BOARD			
022-09804		1	
CONNECTORS			
490-02356	CONN,JUMPER,.1X025,2FCG	1	W1 PINS 2 & 3
510-09768	CONN,POST,100X025,HDR,3MC,THRM	1	W1
510-09784	CONN,POST,100X025,36X2FCG,TEMP	1	J4
520-09793	SCKT,SIMM,.100,30POS,LOPRO,G	2	J1,2

HOST BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS			
201-04756	RES,TRM,20T,PC,100K OHM,SA,CER	2	R52,54
202-00505	RES,CF,5%,1/4W,10 OHM	8	R31,34-37,92,115,182
202-00509	RES,CF,5%,1/4W,47 OHM	9	R114,126,133-138,172
202-00510	RES,CF,5%,1/4W,51 OHM	5	R17,20,24,25,33
202-00518	RES,CF,5%,1/4W,220 OHM	6	R123,160,162,164,165,168
202-00520	RES,CF,5%,1/4W,270 OHM	5	R87-91
202-00523	RES,CF,5%,1/4W,390 OHM	2	R78,179
202-00524	RES,CF,5%,1/4W,470 OHM	4	R29,30,130,171
202-00529	RES,CF,5%,1/4W,1K OHM	23	R61,70,73,74,76,82,83,85,93, R109,128,139,141,144,147-152 R174,180,181
202-00534	RES,CF,5%,1/4W,2.2K OHM	9	R69,75,84,86,156-159, R166,167
202-00542	RES,CF,5%,1/4W,4.7K OHM	2	R71,187
202-00549	RES,CF,5%,1/4W,10K OHM	26	R43,49,67,79-81,94,95, R97,107,108,116-122,127 R131,173,175-178,190
202-00561	RES,CF,5%,1/4W,36K OHM	4	R72,106,188,189
202-00563	RES,CF,5%,1/4W,47K OHM	3	R62,124,161
202-00570	RES,CF,5%,1/4W,100K OHM	1	R112
202-00576	RES,CF,5%,1/4W,200K OHM	2	R51,55
202-00579	RES,CF,5%,1/4W,470K OHM	4	R50,53,68,69
202-00580	RES,CF,5%,1/4W,1M OHM	5	R132,183,184,192,194
202-00581	RES,CF,5%,1/4W,10M OHM	2	R129,170
202-05761	RES,CF,5%,1/4W,120 OHM	8	R60,111,125,153-155,163,169
202-09776	RES,CF,5%,1/4W,91 OHM	15	R32,77,96,100-105,113,140, R142,143,145,146
203-00450	RES,MF,1%,1/4W,100 OHM	4	R1,2,4,11
203-00452	RES,MF,1%,1/4W,309 OHM	2	R42,48
203-00464	RES,MF,1%,1/4W,4.99K OHM	6	R18,21-23,27,28
203-00477	RES,MF,1%,1/4W,12.7K OHM	4	R38,39,44,45
203-01490	RES,MF,1%,1/4W,3.09K OHM	4	R40,41,46,47
203-02353	RES,MF,1%,1/4W,49.9K OHM	8	R3,5,8-10,12,15,16
203-02610	RES,MF,1%,1/4W,1.65K OHM	4	R19,26,186,191
203-02658	RES,MF,1%,1/4W,340 OHM	2	R185,193
203-03347	RES,MF,1%,1/4W,8.45K OHM	2	R7,14

PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS CONT'D.			
203-07557	RES,MF,1%,1/4W,806 OHM	2	R6,13
203-07558	RES,MF,1%,1/4W,374 OHM	2	R98,110
203-07561	RES,MF,1%,1/2W,75 OHM,FP	4	R56-59
203-09815	RES,MF,1%,1/4W,90.9 OHM	1	R99
205-05638	RES,NET,SIP,2%,BUS EL,10KX9	3	RP4,6,7
205-07157	RES,NET,SIP,2%,BUS EL,4.7KX9	1	RP5
205-09499	RES,NET,SIP,2%,ISOL EL,100X4	3	RP1-3
CAPACITORS			
240-00613	CAP,ELEC,22UF,25V,RAD	4	C27,28,31,104
240-01262	CAP,ELEC,330UF,25V,RAD	1	C46
240-06096	CAP,ELEC,10UF,25V,RAD,NON-POL	8	C5,6,11,12,44,45,86,87
240-07335	CAP,ELEC,47UF,25V,RAD,NON-POL	4	C57,61,65,69
240-09786	CAP,ELEC,100UF,25V,RAD,LOW ESR	5	C21,24,96,180,184
241-00652	CAP,TANT,4.7UF,25V,RAD	5	C63,64,71,72,111
241-00654	CAP,TANT,22UF,16V,RAD	9	C47,51,52,56,81,84,88,115,118
244-00662	CAP,MYL,.1UF,5%,RAD	1	C109
244-04960	CAP,MYL,1UF,5%,RAD	6	C16,18,19,22,106,183
244-06174	CAP,MYL,5600PF,5%,RAD	2	C37,40
244-06176	CAP,MYL,.047UF,5%,RAD	1	C112
244-06177	CAP,MYL,.33UF,10%,RAD	2	C101,103
244-06883	CAP,MYL,.01UF,5%,RAD	2	C74,80
244-07568	CAP,MYL,1000PF,5%,RAD	4	C73,75,78,79
245-00590	CAP,CER,150PF,500V,10%,Y5P	12	C1-4,92-95,125,130,143,167
245-01258	CAP,CER,470PF,50V,10%,Z5P	6	C15,17,20,23,129,142
245-03609	CAP,CER,.1UF,50V,Z5U,AX	62	C9,10,25,26,29,30,32,33,35,36, C41,43,48-50,53-55,60,62 C68,70,76,77,82,85,89,91,97, C102,107,108,110,114,116,121, C123,124,126,132,133,136,137, C139,140,147,148,150,153,155, C156,159,162,171,174,177,179, C181,185,186,188,189
245-03610	CAP,CER,.01UF,100V,Z5U,AX	28	C105,113,117,119,120,122, C127,128,131,134,135,138, C141,144,149,151,152,154, C157,158,168,172,173,175,176 C178,182,187
245-03867	CAP,CER,10PF,100V,COG,10%,AX	4	C7,8,13,14
245-03868	CAP,CER,33PF,100V,COG,10%,AX	4	C163,164,169,170
245-03869	CAP,CER,100PF,100V,COG,10%,AX	10	C34,38,39,42,83,90,160, C161,165,166
245-03870	CAP,CER,150PF,100V,COG,10%,AX	4	C58,59,66,67
245-08470	CAP,CER,15PF,100V,COG,5%,AX	2	C145,146
FERRITE BEAD			
270-00779	FERRITE,BEAD	18	FB1-4,8-21
270-06671	FERRITE CHOKE,2.5 TURN	2	FB5,7
DIODES			
300-01029	DIODE,1N914 AND 4148	27	D1-8,15-26,29-35
300-01030	DIODE,1N4004 AND 4005	7	D9-14,27
300-02401	DIODE,BAR 35,SCHOTTKY,LOW VF	1	D28

PART NO.	DESCRIPTION	QTY	REFERENCE
TRANSISTORS			
310-01007	TRANSISTOR,2N3904	5	Q1,4,5,12,13
310-01008	TRANSISTOR,2N3906	1	Q16
310-01646	TRANSISTOR,2N4403	7	Q6-11,14
310-06612	TRANSISTOR,J108	2	Q15,17
INTEGRATED CIRCUITS			
330-03482	IC,DIGITAL,74HC04	1	U37
330-03581	IC,DIGITAL,74HC138	2	U27,28
330-03585	IC,DIGITAL,74HC14	1	U58
330-03611	IC,DIGITAL,74HC273	4	U21,25,26,55
330-04509	IC,DIGITAL,74HC74	2	U31,35
330-04572	IC,DIGITAL,74HCT245	1	U65
330-04674	IC,DIGITAL,74HC4538	1	U14
330-04926	IC,DIGITAL,74HC08	3	U17,36,47
330-05901	IC,DIGITAL,74HC253	1	U44
330-07067	IC,DIGITAL,74HCU04	2	U45,56
330-07260	IC,DIGITAL,74HC32	1	U34
330-07262	IC,DIGITAL,74HC161	2	U32,33
330-07536	IC,DIGITAL,74HC574	2	U29,42
330-07596	IC,DIGITAL,74AC00	2	U15,61
330-07599	IC,DIGITAL,74AC32	1	U64
330-07713	IC,DIGITAL,74HC174	1	U48
330-07715	IC,DIGITAL,74HC541	7	U20,24,41,43,66-68
330-07717	IC,DIGITAL,FILTER,SM5813	1	U12
330-08169	IC,DIGITAL,74HC175	1	U30
330-08170	IC,DIGITAL,74AC157	3	U53,54,63
330-08952	IC,DIGITAL,74HC245	1	U59
330-09769	IC,DIGITAL,74HC573	3	U40,50,60
330-09777	IC,DIGITAL,74AC174	1	U62
340-00742	IC,LINEAR,7805 (LM 340 T-5)	2	U3,4
340-01525	IC,LINEAR,7905,-5V REG	1	U2
340-05945	IC,LINEAR,LM393	1	U18
340-08831	IC,LINEAR,SSM2142,BAL LINE DRV	2	U8,9
340-09787	IC,LINEAR,MC34164,+5V MONITOR	1	U16
340-09789	IC,LINEAR,MC33078,DUAL OP AMP	4	U1,5,6,10
345-09778	IC,INTER,CS8402,DIG I/O XMTR	1	U22
345-09779	IC,INTER,CS8412,DIG I/O RCVR	1	U19
350-04710	IC,SRAM,43256,150NS,LPS	1	U38
350-09749	IC,GAL,20V8,PCM-80,HOST,V1.00	1	U49
350-09750	IC,ROM,27C020,PCM-80,V1.00	1	U39
350-09998	IC,DRAM,256KX4,80NS,ZIP	2	U51,52
355-04283	IC,CONV,ADC0804	1	U23
355-09848	DAC,AD1865	1	U11
355-09849	ADC,CS5389	1	U7
365-09774	IC,UPROC,UPD70208(V40),8MHZ	1	U46
375-02247	IC,OPTO-ISOLATOR,6N138	1	U57
CRYSTALS			
390-06647	CRYSTAL,16.000 MHZ,.01%	1	Y1
390-09843	CRYSTAL,11.2896MHZ,3LEAD	1	Y3
390-09844	CRYSTAL,12.288MHZ,3LEAD	1	Y2
RELAYS/SWITCHES			
410-03584	RELAY,2P2T,LOW LEVEL,DIP,12V	2	RY1,2
453-09772	SW,PBPLP,4P2T,PCRA,2.5MMTRAV	1	SW1

PART NO.	DESCRIPTION	QTY	REFERENCE
BATTERY			
460-04598	BATTERY,LITH,3V,FLAT	1	BAT1
TRANSFORMER			
470-07031	XFORMER,PULSE,AES,5:1	1	TX2
CONNECTORS			
490-02356	CONN,JUMPER,.1X025,2FCG	2	W5,7
510-02899	CONN,POST,100X025,HDR,3MC	2	W5,7
510-06568	CONN,POST,079,HDR,6MC	1	J9
510-07785	CONN,RCA,PCRA,1FCGX2,VERT	1	J10
510-09765	CONN,POST,079,HDR,10MC	1	J16
510-09773	CONN,MEM CARD,PC,68PIN,CONTACT	1	J19
510-09783	CONN,POST,100X025,36X2MCG,ELEV	1	J17
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	3	J13-15
510-09975	1/4"PHONE JACK,PCRA,3C,SW,KINK	6	J1,2,5,6,11,12
SOCKETS			
520-00945	IC SCKT,24 PIN,PC,LO-PRO	1	U11
520-01458	IC SCKT,28 PIN,PC,LO-PRO	2	U7,19
520-04425	IC SCKT,24 PINX.3",PC,LO-PRO	1	U49
520-09077	IC,SCKT,PLCC,68 PIN	1	U46
520-09736	IC,SCKT,32 PIN,PC,TIN,LO-PRO	2	U38,39
LUGS/SPACERS			
620-09648	LUG,SOLDER,.5IDX.72OD/FL.25TAB	7	J1,2,5,6,10,11,12
635-09770	SPCR,SWAGE,4-40X7/8,1/4RD,BR	4	HOST TO DSP BD
CABLES			
680-09755	CABLE,HSG/ST&T,6C,30/8.5,SLV	1	PS TO HOST (J3,J18)
680-09757	CABLE,XITION/SCKT,20C,6"	1	DISPLAY TO HOST (J8)

FP LEVEL POT BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
POTENTIOMETERS			
200-09761	POT,RTY,PC,10KAX2,6MMFL,16,20L	1	R201
CABLES			
670-09817	CABLE,RIB,24-26AWG,7CX.1,1"L	1	LVL POT BD (J104) TO HOST BD (J4)

FP SWITCH BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
DIODES			
300-01029	DIODE,1N914 AND 4148	3	D112,115,119
DISPLAYS/INDICATORS			
430-09818	LED,GRN,T1,LITON,20DEG,12MCD	9	D111,113,114,116-118,120-122
SWITCHES			
453-09771	SW,PB,1P1T,6MM SQX7MM H,160GF	12	SW2-13
CABLES			
680-09763	CABLE,079,SCKT/SCKTRA,10C,2.0"	1	SWITCH BD (J102) TO HOST BD (J16)

FP ENCODER BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
RESISTORS			
202-00514	RES,CF,5%,1/4W,100 OHM	4	R202-205
CAPACITORS			
245-03610	CAP,CER,.01UF,100V,Z5U,AX	4	C200-203
SWITCHES			
452-09762	SW,RTY,ENCODER,36 POS,VERT MNT	2	SW14,15
CABLES			
680-09764	CABLE,079,SCKT/SCKTRA,6C,2.0"	1	ENCODER BD (J103) TO HOST BD (J9)

FP HEADROOM BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
DISPLAYS/INDICATORS			
430-03896	LED,GRN,RECT,.197X.079	6	D103-105,108-110
430-03897	LED,YEL,RECT,.197X.079	2	D102,107
430-03898	LED,RED,RECT,.197X.079	2	D101,106
CABLES			
680-10181	CABLE,RIB,24-28AWG,7CX.1,5.5"	1	HOST BD

MECHANICAL/MISC

PART NO.	DESCRIPTION	QTY	REFERENCE
430-09785	DISPLAY,VF,20X2 CHAR,5X7DOT	1	
510-09985	CONN,MEM CARD,68 PIN,EJECTOR	1	HOST BD (J19)
530-02488	TIE,CABLE,NYL,.14"X5 5/8"	1	PS TO HOST CABLE
530-09382	CLIP,WIRE HRNS,.15DIA,ADH BAK	3	PS TO HOST CABLE
530-09979	CLAMP,CABLE,.169",ZN	1	AC INPUT CABLE
541-00781	BUMPER,FEET,3-M #SJ5018	4	
KNOBS/BUTTONS			
550-03827	BUTTON,.346RD,BLK	2	PWR SW, LEVEL SW
550-09087	KNOB,15MM,6MM/FLAT,BLK	1	LVL POT
550-09759	BUTTON,.20X.50,BLK	3	
550-09760	BUTTON,.20X.50,BLK,W/LENS	9	
550-09767	KNOB,21MM,6MM/FL,BLK/BLK	2	ENCODERS
LUGS/WASHERS/SPACERS			
630-02737	WSHR,FL,#8CLX.02TH,BLK,NYL	4	FP TO CHASSIS
630-03669	SPCR,#4CLX3/8,3/16RD,NYL	2	PWR SW SUPPORT
630-09709	SPCR,PCB/FOOT,.188,NYL	1	HOST BD
630-09983	INSUL,SEMI,SIL RUB,ADH,1.95X1"	1	UNDER (3) REGULATORS
SCREWS			
640-01700	SCRW,4-40X1/2,PNH,PH,SS	2	H/S CLAMP TO CHASSIS(2)
640-01706	SCRW,4-40X3/8,PNH,PH,ZN	4	FP SW BD TO INSERT(2) AC CONN TO CHASSIS (2)
640-02034	SCRW,4-40X5/8,PNH,PH,ZN	2	MEMCD TO HOST BD
640-02736	SCRW,8-32X3/8,BH,SCKT,BLK	4	FP TO CHASSIS
640-03957	SCRW,6-32X3/16,TH,PH,BLK	16	COVERS TO CHASSIS
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	6	DSP TO HOST BD (4) HDRM BD TO INSERT(2)
640-07696	SCRW,M3X8MM,PH,PNH,ZN	2	DSPLY TO INSERT
640-09698	SCRW,2-56X5/8,PNH,PH,ZN	1	RCA CONN TO CHASSIS
640-09758	SCRW,M3X16MM,PH,FH,ZN	2	PWR SW TO CHASSIS
640-09987	SCRW,6-32X5/16,PNH,PH,SEMS,ZN	14	PS TO CHASSIS&BRKT (4); HOST BD TO CHASSIS, INSERT & PS BRKT(9); AC CLAMP TO CHASSIS (1)
641-09699	SCRW,TAP,AB,#2X5/16,PNH,PH,ZN	3	MIDI CONN TO CHASSIS
NUTS			
643-01728	NUT,6-32,KEP,ZN	2	CHASSIS GND (1) AC CABLE CLAMP (1)
643-01732	NUT,4-40,KEP,ZN	6	AC CONN TO CHASSIS (2) FP TO INSERT (2) MEMCD CONN TO HOST (2)
643-01855	NUT,2-56,HEX,ZN	1	RCA CONN TO CHASSIS
WASHERS			
644-01735	WSHR,FL,#6CLX3/8ODX1/32THK	1	CHASSIS GND
644-06635	WSHR,INT-STAR,#2,ZN	1	RCA CONN TO CHASSIS
644-07893	WSHR,FL,.427IDX.550X.035THK,ZN	2	FP ENCODER TO INSERT
650-05899	POPRVT,5/32X1/4,REG PROT HD,AL	3	PS BRKT TO CHASSIS

PART NO.	DESCRIPTION	QTY	REFERENCE
POWER CORDS			
680-08830	CORD,POWER,IEC,6A,2M,EURO	1	
680-09149	CORD,POWER,NA/IEC,SVT,VW-1,10A	1	
680-09756	CABLE,AC PWR,SHLD,14"	1	AC CONN TO PWR SUP & PWR SWITCH
	includes:		
	453-09868 SW,PBPLP,1P1T,PCRA,2.5MMTRAV	1	
	490-00798 CONN,AC,3MC,BULKHD IEC,6A	1	
680-10093	CORD,POWER,IEC,5A,2M,UK	1	
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1	
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1	
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1	
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1	
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1	
MECHANICALS			
690-02060	SLEEVING,SHRINK,3/16X1/2LG,BLK	4	PWR SW(2);AC CONN(2)
700-09853	CHASSIS,WRAPAROUND,PCM-80	1	
700-09856	CHASSIS,INSERT,FP,PCM-80	1	
700-09857	COVER,TOP/BOTTOM,PCM-80	2	
700-09859	BRACKET,PWR SUP,PCM-80	1	
701-09860	BRACKET,POT,SHIELD,PCM-80	1	INPUT LEVEL POT
701-09863	CLAMP,HEATSINK,TO-220	1	HOST BD
702-09850	PANEL,FRONT,PCM-80	1	
702-09858	COVER,PROTECTIVE,TOP,PS,PCM-80	1	
702-09861	COVER,PROTECTIVE,BOT,PS,PCM-80	1	
702-09988	PLATE,HEATSINK,TO-220	1	HOST BD
703-09854	PANEL,OVLY,REAR,PCM-80	1	
703-09862	LENS,DISPLAY,PCM-80	1	
710-10190	PC BD,MEMCD CONN CVR,PCM-80	1	
POWER SUPPLIES			
750-09766	PWR SUP,5V@5A,+15V@2A/-15V@.5A	1	

7

Schematics and Assembly Drawings

	Part No.	Title
1.	060-09827	Schematic, Host Bd
2.	-	Main Bd Component Layout
3.	060-09839	Schematic, Front Panel Bds
4.	060-10341	Schematic, Output Level Bd
5.	080-09865	Assembly Dwg, Chassis

REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
1	ADD PULLUP R181 TO HTC (RENAMED HTC/); CHANGE R106 FROM 10K TO 36K; UPDATE NOTE NOTE 6 - FOR REV 3 PCB PER PCR #940127-00	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94
2	REVISE SHEETS 4&7 PER ECO #940325-00; DELETE NOTE 6 & REVISE SHEETS 3&9 PER ECO #940520-00; REVISE SHEETS 2, 3, 9, 12 FOR REV 4 PCB PER ECO #940613-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94
3	REVISE SHEETS 4&7 FOR REV 5 PCB PER ECO #941025-01	RWH 11/7/94 KE 11/7/94	CW 11/7/94 AF 11/7/94
4	REVISE SHEET 4 (ROM/SRAM NOTES) PER ECO #941121-00	CW 1/17/95 KE 1/17/95	RWH 1/17/95 AF 1/17/95

SPARES

74HC32 U34: pins 9, 10 → 8 N/C; pins 12, 13 → 11 N/C

NOTES

1. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
2. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
3. 1 / A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
4. ON BOARD CONNECTION-TO; ON BOARD CONNECTION-FROM; SOLDER CONNECTION
5. REFERENCE DESIGNATORS, LAST USED: U68, R194, C189, G17, D35, FB21, RY2, Y3, RP7, SW1, BAT1, TX2, J19.

DOCUMENT CONTROL BLOCK: #060-09827

SHEET NUMBER	REVISION NUMBER
1 OF 13	4
2 OF 13	2
3 OF 13	2
4 OF 13	4
5 OF 13	0
6 OF 13	0
7 OF 13	2
8 OF 13	1
9 OF 13	1
10 OF 13	0
11 OF 13	0
12 OF 13	1
13 OF 13	1

CONTRACT NO.

Lexicon
100 BEAVER ST. WALTHAM, MA 02154

APPROVALS	DATE
DRAWN KE/SF	11/22/93
CHECKED KE	11/30/93
D.C. RWH	12/1/93
ISSUED AF	12/1/93

TITLE: SCHEM, HOST BD, PCM-80 HOST uPROC

SIZE	CODE	NUMBER	REV.
B		060-09827	4

SHEET 1 OF 13

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	P.E. AUTHORIZED
1	CHANGE R94 FROM 10K TO 1K - FOR REV 3 PCB PER PCR #940127-00	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94
2	CHANGE R94 FROM 1K TO 10K. CONNECT LWAITY/ TO U24-8. - FOR REV 4 PCB PER ECO #940613-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94

HOST STATUS REGISTER 0 — 74HC541 (U41)

HOST STATUS REGISTER 1 — 74HC541 (U24)

HOST STATUS REGISTER 2 — 74HC541 (U20)

HOST CONTROL REGISTER 0 — 74HC273 (U25)

HOST CONTROL REGISTER 1 — 74HC273 (U26)

HOST CONTROL REGISTER 2 — 74HC273 (U21)

HOST CONTROL REGISTER 3 — 74HC273 (U55)

LEXICHIP OVERLOAD HOLD / CLEAR LOGIC — 74HC74 (U35)

CONTRACT NO.		Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, HOST BD, PCM-80 CONTROL AND STATUS REGS	
DRAWN KE/SF	11/22/93	SIZE: B	CODE:
CHECKED KE	11/30/93	NUMBER: 060-09827	REV: 2
G.C. RWH	12/1/93		
ISSUED AF	12/1/93	SHEET 2 OF 13	

REVISIONS			
REV	DESCRIPTION	DRAWN BY / CHECKED	APP'D / AUTHORIZED
1	ADD FB21: MOVE FB14 FROM +5VD TO FPDRNG - FOR REV 3 PCB PER PCR #940127-00	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94
2	DELETE .01 UF CAP (C118). ADD 22 UF CAP (C118) TO U23-9. ADD 22UF CAP (C115) & 10 OHM RES (R182) TO U23-20 PER ECO #940520-00. CONNECT HEADROOM LED REGISTER BIT 7 (U29-12) TO OUTPUT LEVEL CIRCUIT ON SHEET 12 - FOR REV 4 PCB - PER ECO #940513-00.	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE SCHEM, HOST BD, PCM-80 HOST I/O	
DRAWN KE/SF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE
D.C. RWH	12/1/93	NUMBER 060-09827	REV. 2
ISSUED AF	12/1/93	SHEET 3 OF 13	

FLASHVPPEN

HA<0: 19>

SOCKET @ U39 ACCEPTS EITHER:

256K X 8 EPROM (27C020, 27C2001)

OR:

512K X 8 EPROM (27C040, 27C4001)

ACCESS TIME <= 150 NS

ROM

27C020

HROMEN/

HD<0: 7>

RAM CHIP-ENABLE POWER-DOWN TRACKING CIRCUIT

VRAM

R74 1K 1/4W 5%

NVRAMEN

PWR_OK

74AC00 U15

11 GNVRAMEN/

SRAM

43256

BATTERY BACKED-UP SRAM

32-PIN SOCKET @ U38 ACCEPTS EITHER:

28-PIN 32K X 8 SRAM (43256):

Install into socket such that Pin 1 of IC is in Pin 3 of socket.

OR 32-PIN 128K X 8 SRAM (431000)

ACCESS TIME <= 150 NS

FROMVPPD

+15VDU

R64 10K 1/4W 5%

R63 2.2K 1/4W 5%

2N3906 Q2

Q3 2N3904

R66 10K 1/4W 5%

C99 .1/50

U13 78L12 VIN VOUT GND

C100 .1/50

C98 100/25

R65 2.2K 1/4W 5%

+12VD

+5VD

R67 10K 1/4W 5%

W1

No Jumper for EPROM (27C0x0)
Jumper across 1-2 for 5V Flash Memory
Jumper across 2-3 for 12V Flash Memory
Pull-up not necessary for Flash Memory

FLASH MEMORY SUPPORT CIRCUITRY IS NOT CURRENTLY USED. LOCATIONS R63-66, C98-100, Q2-3, U13, AND W1 MAY BE UNPOPULATED.

HSTSLVCB

DRAM ADDRESS MUX

74AC157 U53, U54, U63

PTHDRA<0: 9>

HDRA<0: 9>

DRAM

2 X 256K X 4 DRAM
ACCESS TIME <= 100 NS

HM514256 U51, U52

SELCA

R174 1K 1/4W 5%

R173 10K 1/4W 5%

74AC174 U62

R145 91 5% 1/4W

R146 91 5% 1/4W

PTHRAS/ HRAS/ PTHCAS/ HCAS/

DMEMOP/

HBS<0: 2>

HBS0

LOGICHI

HCLK/

HST56KCB

HREQ

56KOVRL/

FINTMSK/

74HC08 U36

HMRDQ/

HREGQ

HBSQ0

HBSQQ0

56KINT

SPARES

VRAM 74AC00 U15 3 N/C

VRAM 74AC00 U15 6 N/C

VRAM 74AC00 U15 8 N/C

REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	E.C./ AUTHORIZED
1	CHANGE SIGNAL NAME GNVRAMEN TO GNVRAMEN/.	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94
2	REMOVE HREQ FROM U36-9 AND CONNECT IT TO 56KOVRL/ PER ECO #940325-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94
3	REMOVE HMWR/ FROM U39-31 AND CONNECT IT TO HA19. ADD NOTE TO NOT POPULATE FLASH MEMORY SUPPORT CIRCUIT. PER ECO #941025-01.	RWH 11/7/94 KE 11/7/94	CW 11/7/94 AF 11/7/94
4	UPDATE ROM/SRAM NOTES (U38, U39) PER ECO 941121-00	CW 1/17/95 KE 1/17/95	RWH 1/17/95 AF 1/17/95

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, HOST BD, PCM-80 HOST MEMORY
DRAWN KE/AEJ	11/22/93	
CHECKED KE	11/30/93	SIZE: B; CODE; NUMBER: 060-09827; REV.: 4
G.C. RWH	12/1/93	
ISSUED AF	12/1/93	SHEET 4 OF 13

REVISIONS			
REV	DESCRIPTION	DRAFTSM/ CHECKER	D.E./ AUTHORIZED

HMWR/
HAST80
74AC32 U64
74AC32 U64
74AC32 U64
PREBCWE/

HBSGQ0
HBSG0
CWRPROT
HD <0:7>
HA <0:19>
HSTSLVCB
CARDEN/
CARDBUS

CARD DATA BUFFER
74HCT245 U65
HD0 HD1 HD2 HD3 HD4 HD5 HD6 HD7 HMRD/
CD0 CD1 CD2 CD3 CD4 CD5 CD6 CD7
DIR
+5VD
R176 10K 5% 1/4W
CARDENB/

CARD ADDRESS BUFFERS
74HC541 U68
HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7
CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7
74HC541 U67
HA12 HA15 HA14 HA13 HA8 HA9 HA11 HA10
CA12 CA15 CA14 CA13 CA8 CA9 CA11 CA10

CARD CONTROL BUFFER
74HC541 U66
HMRD/ CWP
CCE1/ COE/ CWE/ CWRPROT N/C N/C N/C
PREBCWE/
CARDENB/
74HC14 U58
DISCARD/
DISCARD

RP5 4.7K
CCE1/ CCE2/ COE/ CWE/ CWP CWRPROT N/C N/C N/C
RP4 10K
N/C CD0 CD1 CD2 CD3 CD4 CD5 CD6 CD7
RP7 10K
N/C CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7
RP6 10K
N/C CA12 CA15 CA14 CA13 CA8 CA9 CA11 CA10

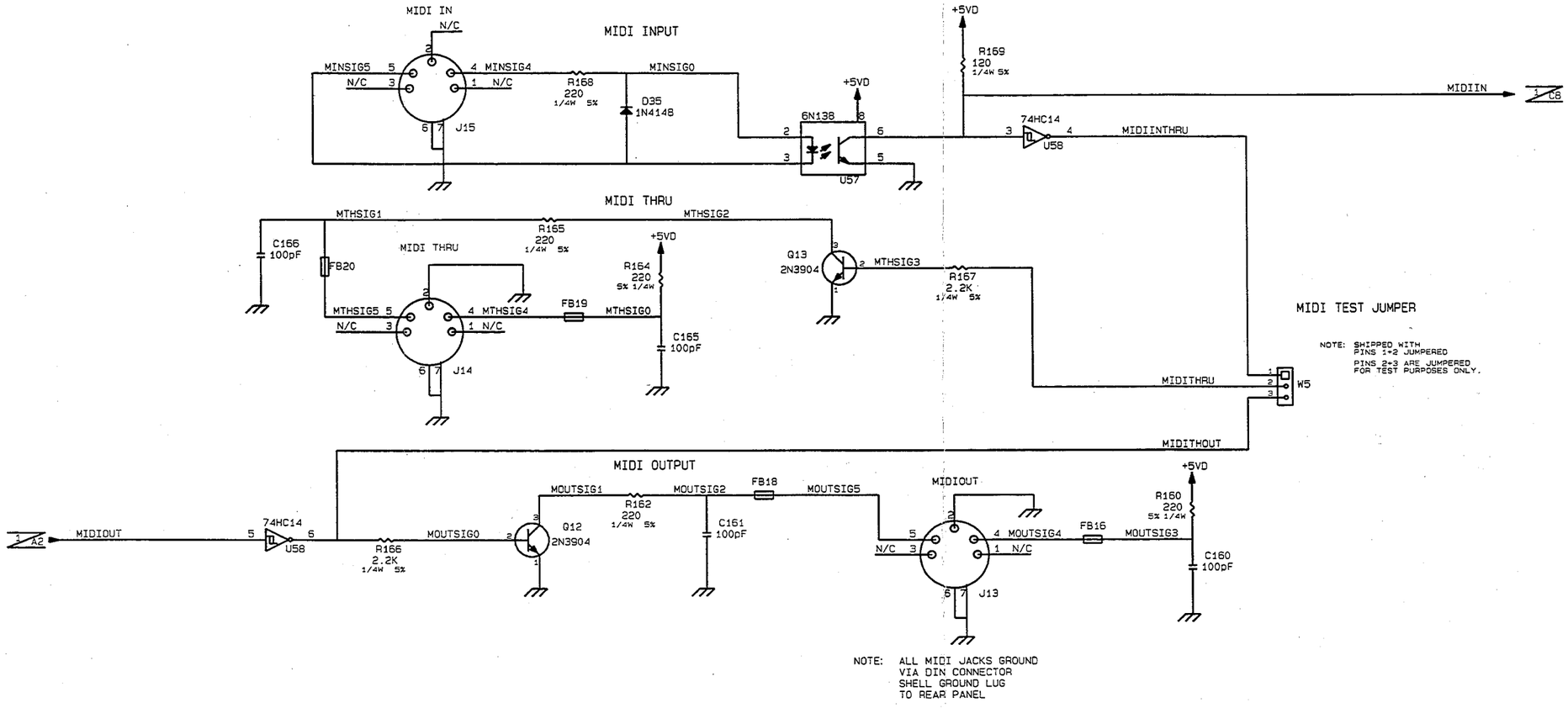
CVCC
+5VD
R179 390 1/4W 5%
2N4403 Q14
C183 1uF MYLAR
R180 1K 5% 1/4W
C185 .1/50
R175 10K 5% 1/4W
R177 10K 5% 1/4W
74AC32 U64
CDET1/
CDET2/
CARDDET/
CWRPROT

CARD CONFIG. JUMPER
(TIE CVCCVPP TO CVCC FOR UV ERASABLE ROM; OTHERWISE LEAVE OPEN OR TIE TO GROUND)
W7
CVCCVPP

J19 PC MEMORY CARD INTERFACE ADAPTER (PCMCIA) SOCKET

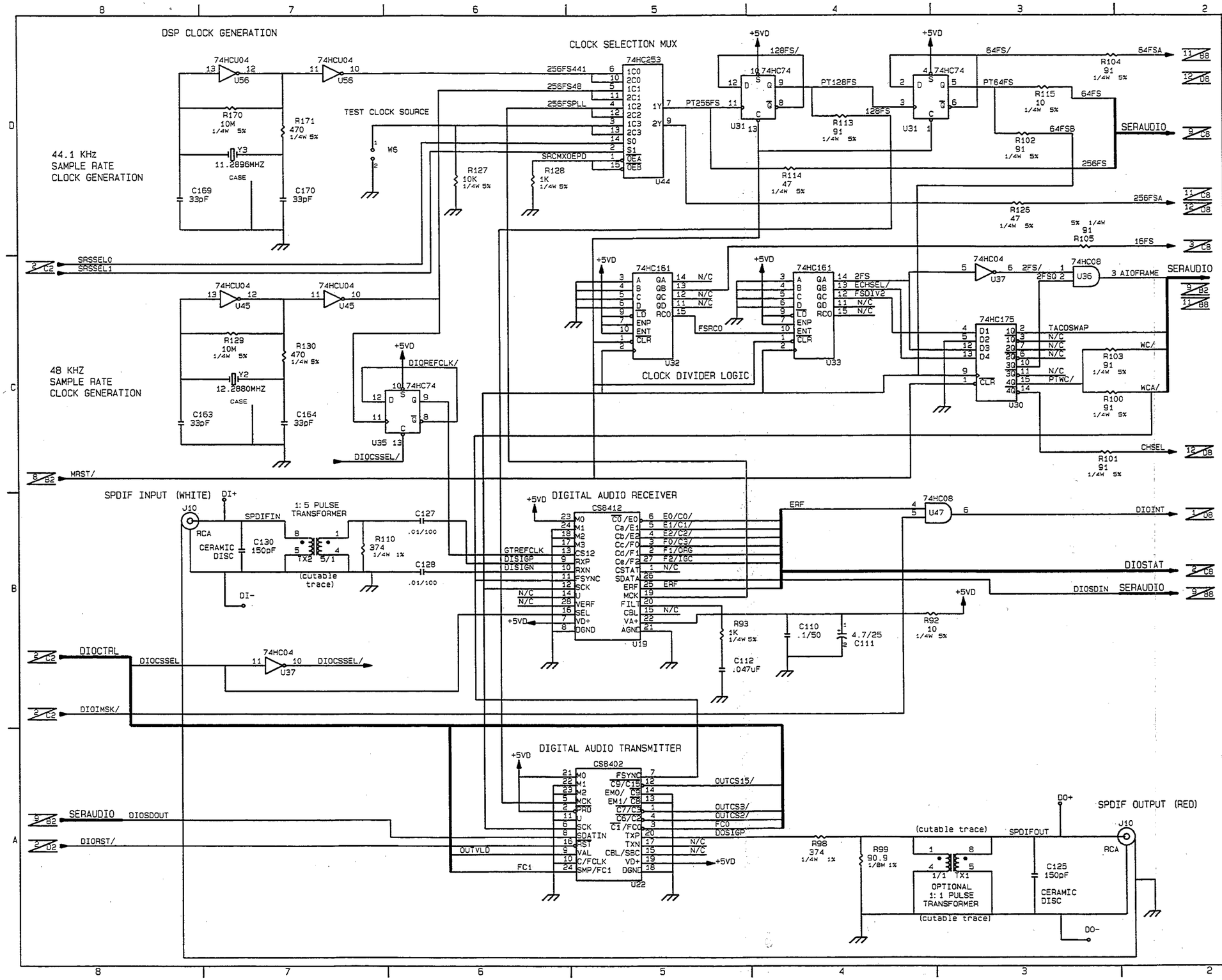
1	GND	GND
2	CD3	CD4
3	CD4	CD3
4	CD5	CD2
5	CD6	CD1
6	CD7	CD0
7	CCE1/	CA0
8	CA10	CA1
9	COE/	CA2
10	CA11	CA3
11	CA9	CA4
12	CA8	CA5
13	CA13	CA6
14	CA14	CA7
15	CWE/	CA8
16	N/C	CA9
17		CA10
18		CA11
19	CA16	CA12
20	CA15	CA13
21	CA12	CA14
22	CA7	CA15
23	CA6	CA16
24	CA5	N/C
25	CA4	N/C
26	CA3	N/C
27	CA2	N/C
28	CA1	N/C
29	CA0	N/C
30	CD0	N/C
31	CD1	N/C
32	CD2	N/C
33	CWP	N/C
34	GND	GND
35		
36	CDET1/	CDET2/
37	N/C	N/C
38	N/C	N/C
39	N/C	N/C
40	N/C	N/C
41	N/C	N/C
42	CCE2/	CA17
43	N/C	CA18
44	N/C	CA19
45	N/C	N/C
46	CA17	N/C
47	CA18	N/C
48	CA19	N/C
49	N/C	N/C
50	N/C	N/C
51	N/C	N/C
52	N/C	N/C
53	N/C	N/C
54	N/C	N/C
55	N/C	N/C
56	N/C	N/C
57	N/C	N/C
58	N/C	N/C
59	N/C	N/C
60	N/C	N/C
61	CREG/	CREG/
62	BVD2	BVD2
63	BVD1	BVD1
64	N/C	N/C
65	N/C	N/C
66	N/C	N/C
67	CDET2/	CDET1/
68	GND	GND

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE SCHEM, HOST BD, PCM-80 PC MEM CARD INTERFACE	
DRAWN KE/SF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE NUMBER 060-09827 REV. 0
Q.C. RWH	12/1/93		
ISSUED AF	12/1/93	SHEET 5 OF 13	



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	E.C./ AUTHORIZED

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154			
APPROVALS	DATE	TITLE SCHEM, HOST BD, PCM-80 MIDI		
DRAWN KE/SF	11/22/93			
CHECKED AF	11/30/93	SIZE B	CODE	NUMBER 060-09827 REV. 0
Q.C. RWH	12/1/93			
ISSUED KE	12/1/93	SHEET 6 OF 13		



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
1	DISCONNECT U22-13 & U22-14 FROM VCC AND CONNECT THEM TO DGND PER ECO #940325-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94
2	CHANGE THE VALUE OF R115 FROM 91 OHMS TO 10 OHMS PER ECO #941025-01	RWH 11/7/94 KE 11/7/94	CW 11/7/94 AF 11/7/94

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE SCHEM. HOST BD. PCM-80 DIGITAL I/O
DRAWN KE/SF	11/22/93	
CHECKED KE	11/30/93	SIZE B · CODE · NUMBER 060-09827 · REV. 2
Q.C. RWH	12/1/93	
ISSUED AF	12/1/93	SHEET 7 OF 13

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	D.O.T./ AUTHORIZED
1	REMOVE W2, W3; MOVE R73; CHANGE R73 FROM 10K TO 1K - FOR REV 3 PCB PER PCR #940127-00	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94

+5V MONITOR

MC34164 U16

RESET DELAY

WATCHDOG TIMER

RAM BATTERY BACKUP

BATTERY MONITOR

SPARE

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE SCHEM, HOST BD. PCM-80 RESET/BATTERY/PS CONNECTION	
DRAWN AEJ/SF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE	NUMBER 060-09827	REV. 1
Q.C. RWH	12/1/93		
ISSUED AF	12/1/93	SHEET 8 OF 13	

REVISIONS			
REV	DESCRIPTION	DRAFTSMAN/ CHECKER	ENG./ AUTHORIZED
1	DELETE 0.1 UF (C115) PER ECO #940520-00. ADD LWAITY/ TO J17-B23 - FOR REV 4 PCB - ECO #940613-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94

SPARE1

SPARE2

J17 IS CONNECTED TO DSP BOARD

GROUND TEST POINTS

TP1 TP2 TP3 TP5 TP6 TP7 TP8 TP9 TP10

J17

A1		B1	
A2	HD0	B2	HD1
A3	HD2	B3	HD3
A4	HD4	B4	HD5
A5	HD6	B5	HD7
A6		B6	
A7	AIOFRAME	B7	TACOSWAP
A8	DIOSDIN	B8	FPLOCK/
A9	DSPHEN/	B9	PGAIOSDOUT
A10	GTAIOSDIN	B10	56KRST/
A11	HMWRB/	B11	HACK/
A12	+5VD	B12	+5VD
A13	HMRD3Q	B13	56KOVRL/
A14	64FS	B14	FRCMOD
A15	HMRD/	B15	WC/
A16	SBUSEN/	B16	PGDIOSDOUT
A17	N/C (FCLKDIV2/)	B17	LOVLDP/
A18		B18	
A19	HREQ	B19	HCLK/
A20	LEXRST/	B20	SHSINT/
A21	HASTBQ	B21	CSHINT/
A22	SLVRST/	B22	SHINT
A23	HBW/RQ	B23	LWAITY/
A24	+5VD	B24	+5VD
A25	256FS	B25	N/C
A26	N/C	B26	HWAIT/
A27	HA14	B27	HA15
A28	HA0	B28	HA1
A29	HA2	B29	HA3
A30		B30	
A31	HA4	B31	HA5
A32	HA6	B32	HA7
A33	HA8	B33	HA9
A34	HA10	B34	HA11
A35	HA12	B35	HA13
A36		B36	

HD<0: 7>

HA<0: 13>

HSTSLVCB

HST56KCB

SERAUDIO

SERIAL I/O MUTING LOGIC

AIOSDIN — 74HC08 U47 (12, 13) — 11 GTAIOSDIN

PGAIOSDOUT — 74HC08 U47 (9, 10) — 8 AIOSDOUT

PGDIOSDOUT — 74HC08 U47 (1, 2) — 3 DIOSDOUT

MUTE/

+5VD

C91 .1/50, C102 .1/50, C108 .1/50, C97 .1/50, C114 .1/50, C121 .1/50, C123 .1/50, C124 .1/50, C116 .1/50, C126 .1/50, C133 .1/50, C137 .1/50, C140 .1/50, C132 .1/50, C136 .1/50, C147 .1/50, C156 .1/50, C148 .1/50, C153 .1/50, C159 .1/50

100/25 C184

C150 .1/50, C155 .1/50, C162 .1/50, C171 .1/50, C174 .1/50, C177 .1/50, C179 .1/50, C186 .1/50, C188 .1/50

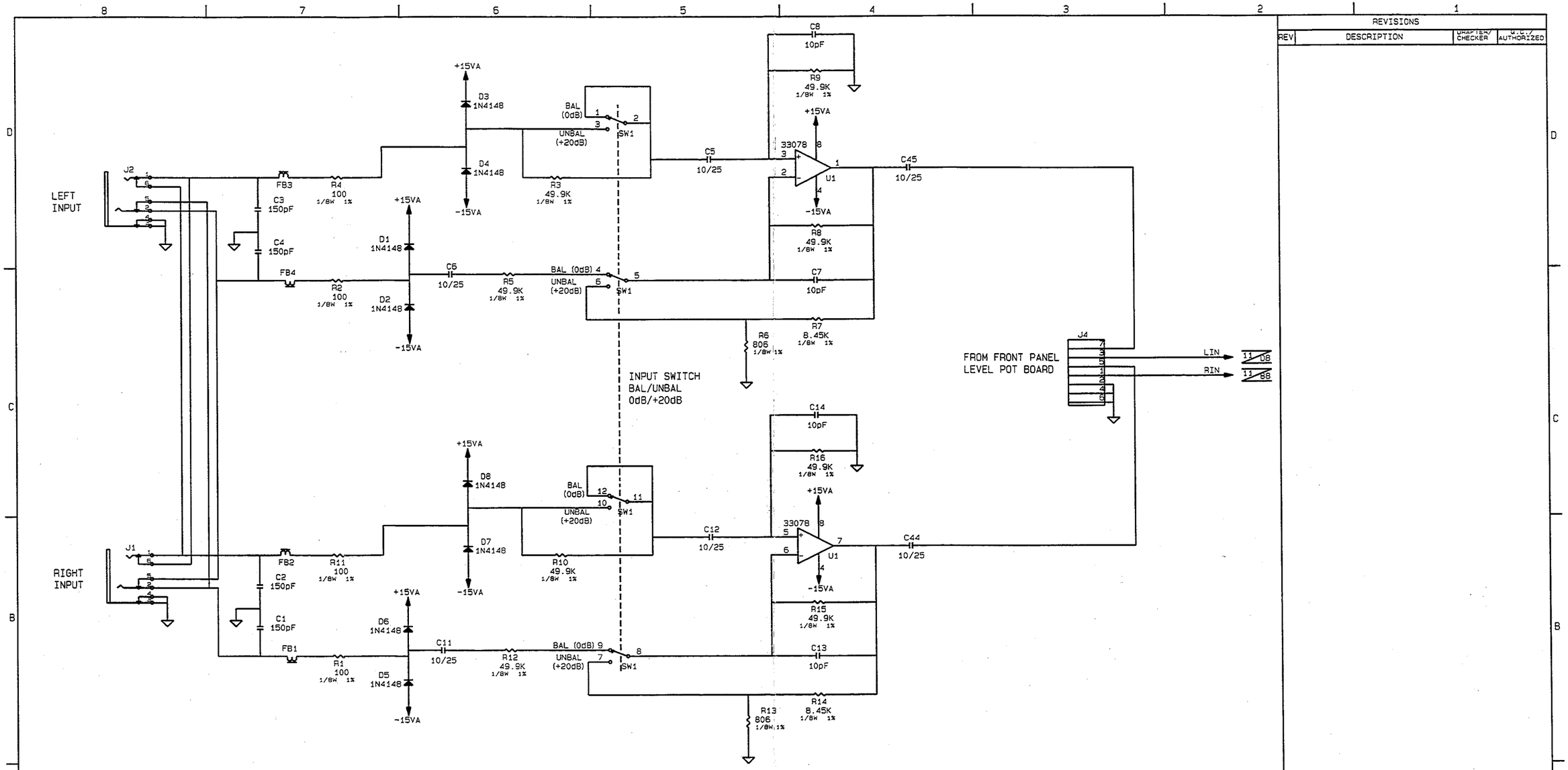
C105 .01/100, C113 .01/100, C122 .01/100, C119 .01/100, C131 .01/100, C135 .01/100, C141 .01/100

C134 .01/100, C138 .01/100, C152 .01/100, C158 .01/100, C144 .01/100, C149 .01/100, C154 .01/100, C151 .01/100, C157 .01/100, C173 .01/100, C175 .01/100, C172 .01/100, C176 .01/100, C168 .01/100, C178 .01/100, C182 .01/100, C187 .01/100

VRAM

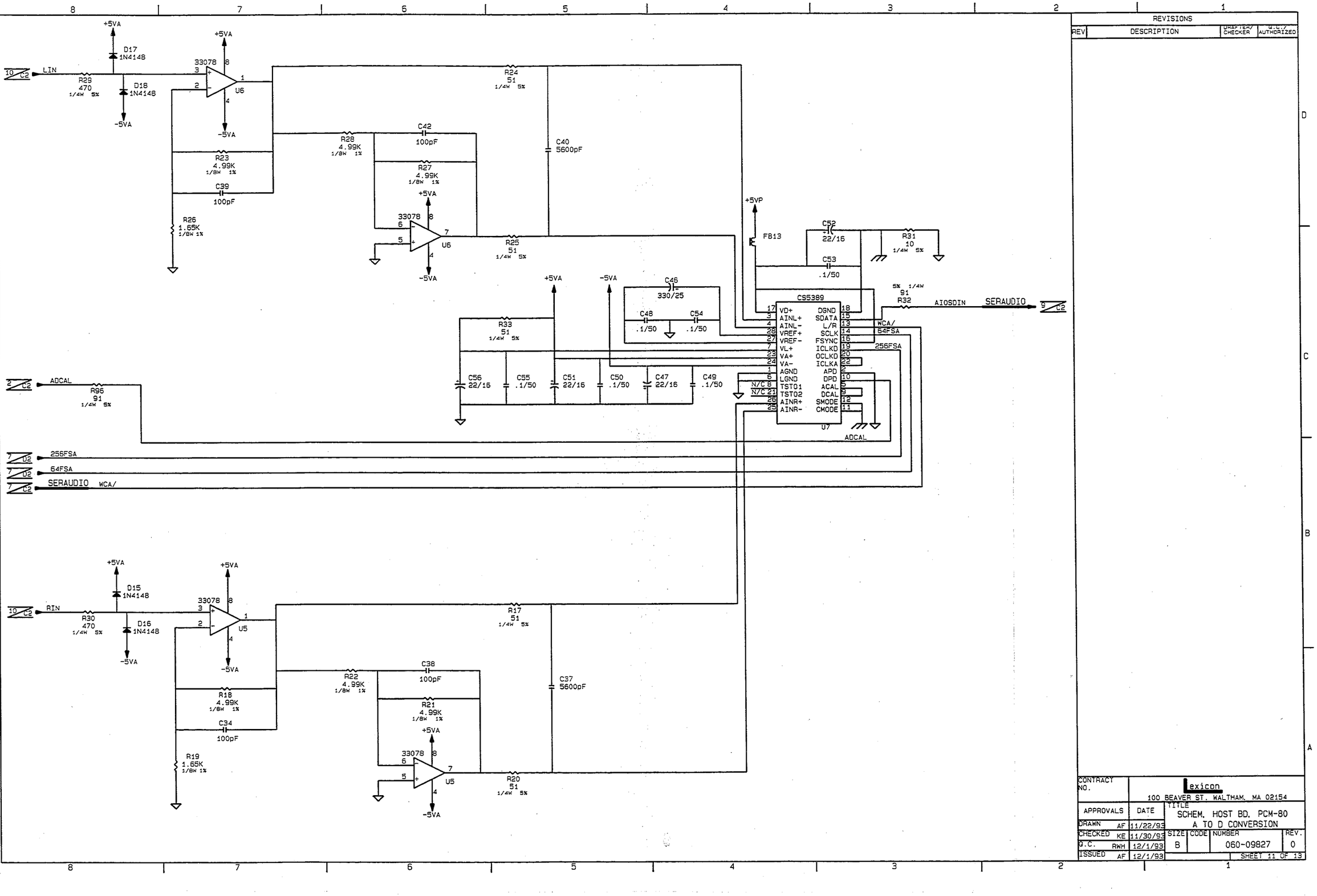
C120 .01/100, C139 .1/50

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEM, HOST BD, PCM-80 DSP BOARD CON./BYPASS CAPS
DRAWN KE/SF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE NUMBER 060-09827 REV. 1
Q.C. RWH	12/1/93		
ISSUED AF	12/1/93		SHEET 9 OF 13



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	E.E./ AUTHORIZED

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE SCHEM. HOST BD. PCM-80 ANALOG INPUTS	
DRAWN AF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE
Q.C. RWH	12/1/93	NUMBER 060-09827	REV. 0
ISSUED AF	12/1/93	SHEET 10 OF 13	



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	C.E./ AUTHORIZED

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEM. HOST BD. PCM-80 A TO D CONVERSION	
DRAWN AF	11/22/93		
CHECKED KE	11/30/93	SIZE: B	CODE:
Q.C. RWH	12/1/93	NUMBER: 060-09827	REV.: 0
ISSUED AF	12/1/93	SHEET 11 OF 13	

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
1	ADD ANALOG OUTPUT LEVEL SELECTION CIRCUITRY FOR REV 4 PCB PER ECO #940513-00.	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEM, HOST BD, PCM-80 DAC & OUTPUTS
DRAWN AF	11/22/93		
CHECKED KE	11/30/93	SIZE B	CODE / NUMBER 060-09827 / REV. 1
Q.C. RWH	12/1/93		
ISSUED AF	12/1/93	SHEET 12 OF 13	

FRONT PANEL POWER SWITCH

AC INPUT

HOT 1

GROUND 2

NEUTRAL 3

IEC CONNECTOR

TO CHASSIS

POWER SUPPLY

+5V @ 5.0A

+15V @ 2.0A

-15V @ 0.3A

(ABSOLUTE MAX. RATINGS)

+15V 1
+5V 2
+5V 3
GND 4
GND 5
-15V 6

FERRITE SLEEVE 1.5 TURNS

+15V 1
GND 2
-15V 3

TO ANALOG CIRCUITRY

+5V 1
+5V 2
GND 3

TO DIGITAL CIRCUITRY

+15VDU

4 05

(Note: FB6 is unpopulated)

+15VDU

FB5

C16 1uF

C15 470pF

(cutable)

FB6

C21 100/25

C19 1uF

C20 470pF

J3
1 ORANGE
2 BLACK
3 BLUE

C18 1uF

C17 470pF

FB7

C24 100/25

C22 1uF

C23 470pF

-15VDU

+15VA

-15VA

J18
1 RED
2 RED
3 BLACK

C181 .1/50

C180 100/25

+5VD

D13 1N4004

U4 7805 VIN VOUT GND

+15VA

C33 .1/50

D14 1N4004

C31 22/25

C32 .1/50

+5VP

D11 1N4004

U3 7805 VIN VOUT GND

+15VA

C30 .1/50

D12 1N4004

C28 22/25

C29 .1/50

+5VA

C26 .1/50

D10 1N4004

C27 22/25

C25 .1/50

GND VIN VOUT 7905 U2

-15VA

-5VA

D9 1N4004

+5VA

C41 .1/50

C35 .1/50

C89 .1/50

-5VA

C43 .1/50

C36 .1/50

C82 .1/50

+15VA

C9 .1/50

C76 .1/50

-15VA

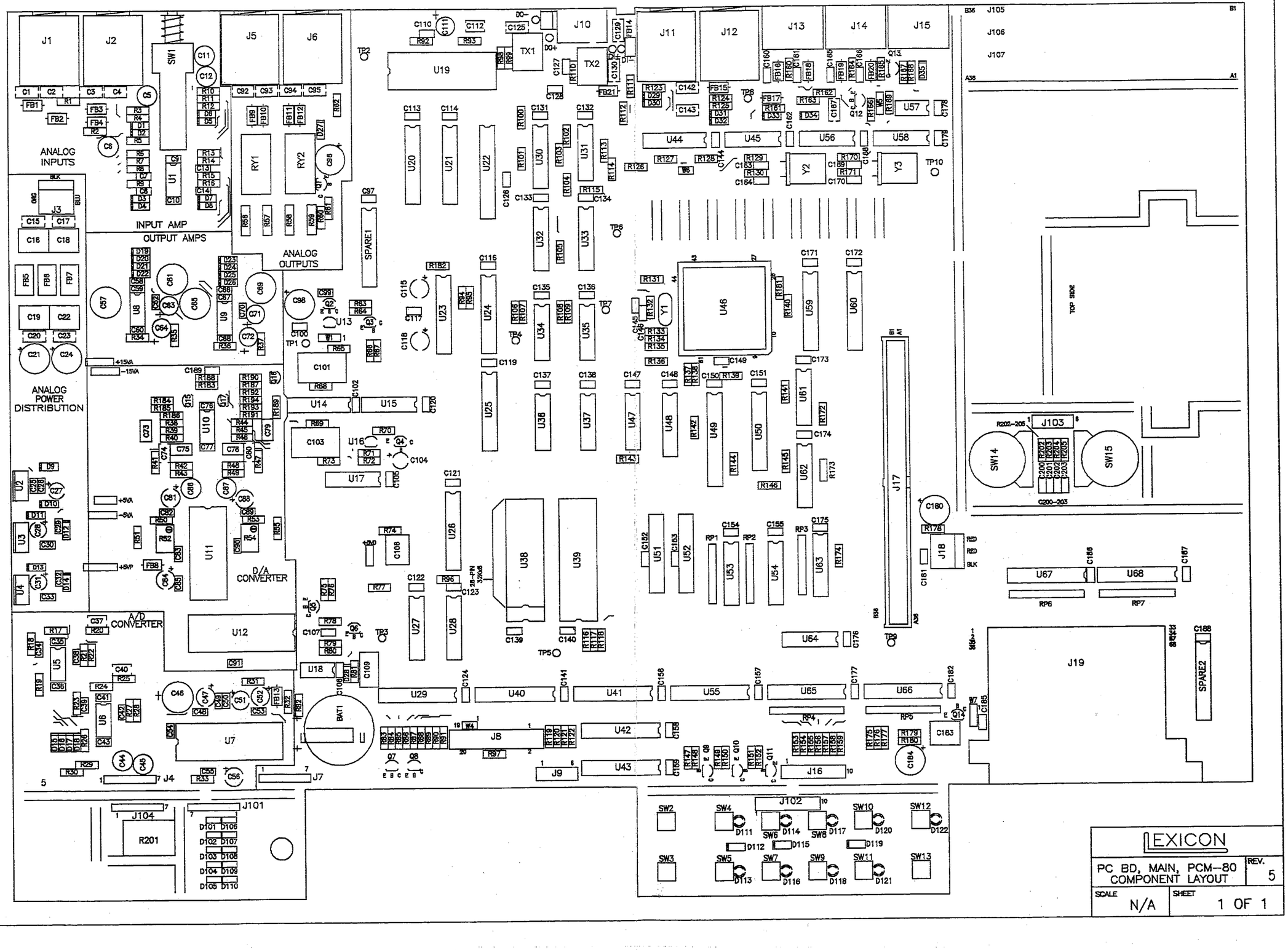
C10 .1/50

C77 .1/50

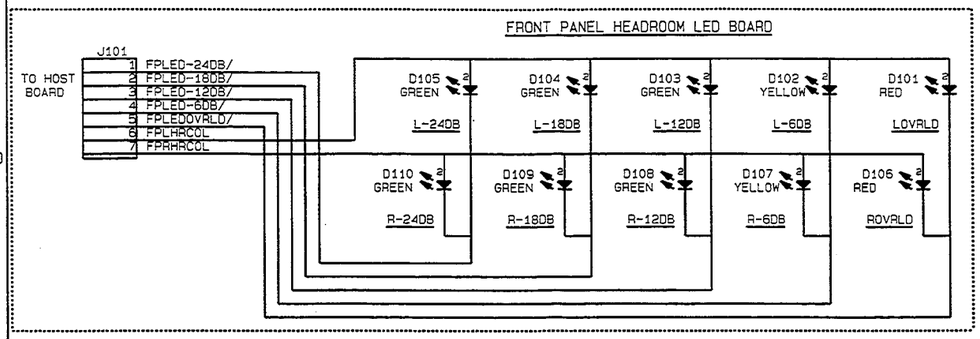
REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
1	DEPOPULATE FB6 - FOR REV 3 PCB PER PCR #940127-00	CW 2/10/94 KE 2/17/94	RWH 2/17/94 CB/AF 2/17/94

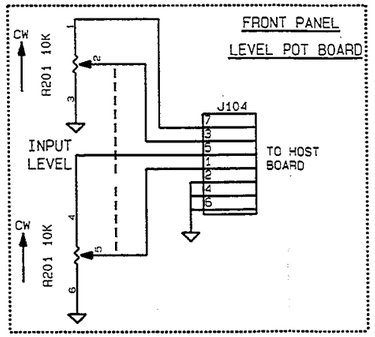
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, HOST BD, PCM-80 POWER SUPPLY			
DRAWN AF	11/22/93				
CHECKED KE	11/30/93	SIZE B	CODE	NUMBER 060-09827	REV. 1
Q.C. RWH	12/1/93				
ISSUED AF	12/1/93	SHEET 13 OF 13			


J1
J2
J5
J6
J10
J11
J12
J13
J14
J15
J105
J106
J107
SW1
TX1
TX2
U19
ANALOG INPUTS
INPUT AMP
OUTPUT AMPS
ANALOG OUTPUTS
ANALOG POWER DISTRIBUTION
RY1
RY2
SPARE1
U20
U21
U22
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U44
U45
U56
U58
U57
Y2
Y3
TP10
U46
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
TOP SIDE
J103
SW14
SW15
J17
J18
J19
SPARE2
U14
U15
U16
U17
U23
U24
U25
U26
U27
U28
U29
U40
U41
U42
U43
U47
U48
U49
U50
U51
U52
U53
U54
U55
D/A CONVERTER
A/D CONVERTER
U12
U11
U10
U8
U9
U5
U6
U7
U18
BAT1
J4
J7
J8
J9
J16
J101
J102
J104
R201
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
D111
D112
D113
D114
D115
D116
D117
D118
D119
D120
D121
D122
LEXICON
PC BD, MAIN, PCM-80
COMPONENT LAYOUT
REV. 5
SCALE N/A
SHEET 1 OF 1

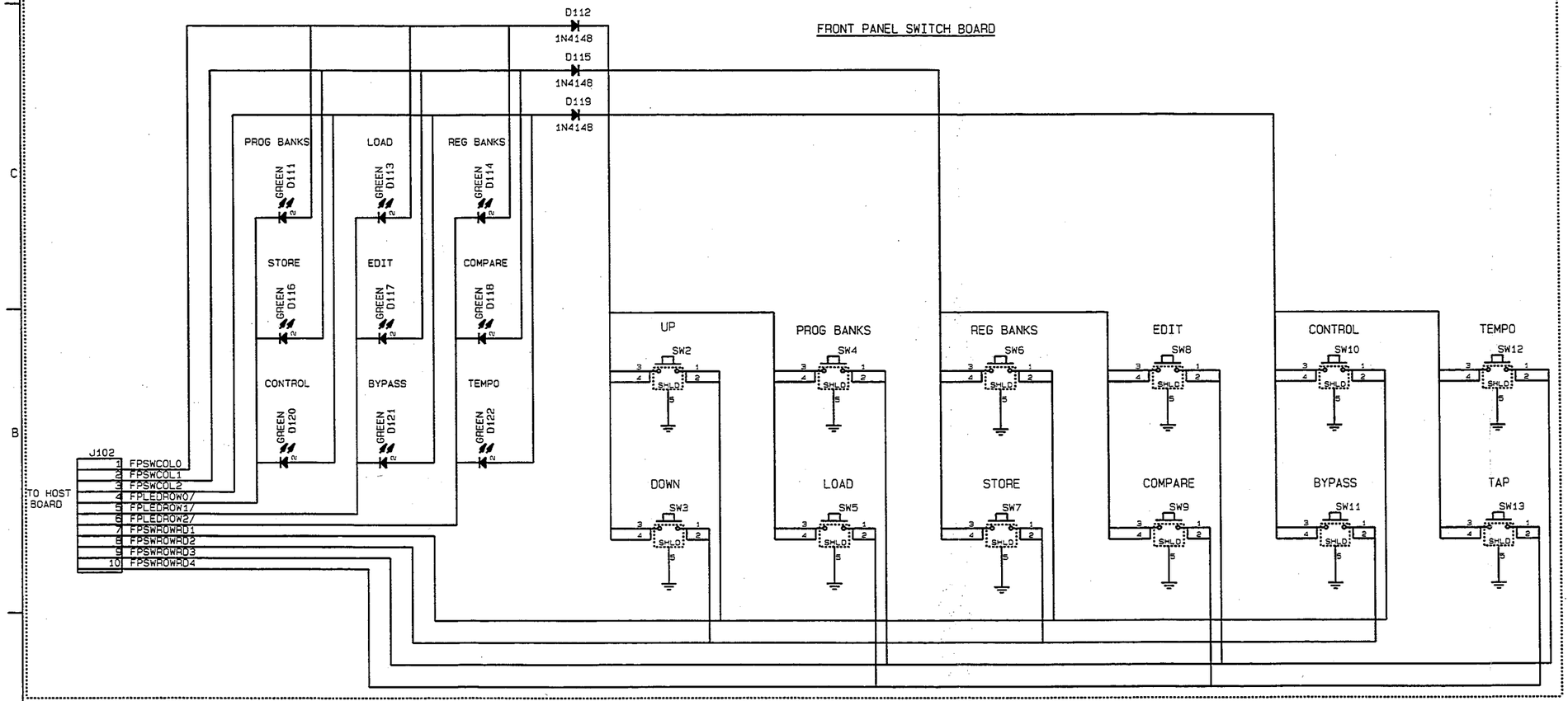
FRONT PANEL HEADROOM LED BOARD



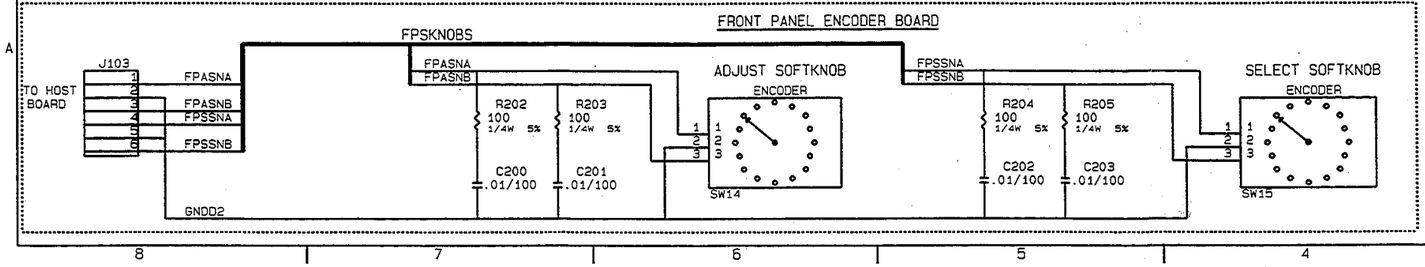
FRONT PANEL LEVEL POT BOARD



FRONT PANEL SWITCH BOARD



FRONT PANEL ENCODER BOARD



REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	E.C./ AUTHORIZED
1	ADD DEBOUNCE RES (R202-205) AND CAPS (C200-203) TO ROTARY ENCODER BOARD PER ECO #940613-00	CW 7/6/94 KE 7/6/94	RWH 7/6/94 AF 7/6/94

NOTES

1. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
2. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
3. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
4. ON BOARD CONNECTION-TO / ON BOARD CONNECTION-FROM / SOLDER CONNECTION
5. REFERENCE DESIGNATORS, LAST USED: C203, R205, D122, SW15, J104

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, FRONT PANEL BDS, PCM-80 HEADROOM LEDS/INPUT LEVEL POT/ SWITCHES/ENCODERS
DRAWN KE/SF	11/22/93	
CHECKED KE	11/30/93	SIZE: B; CODE: ; NUMBER: 060-09839; REV.: 1
Q.C. RWH	12/1/93	
ISSUED AF	12/1/93	SHEET 1 OF 1

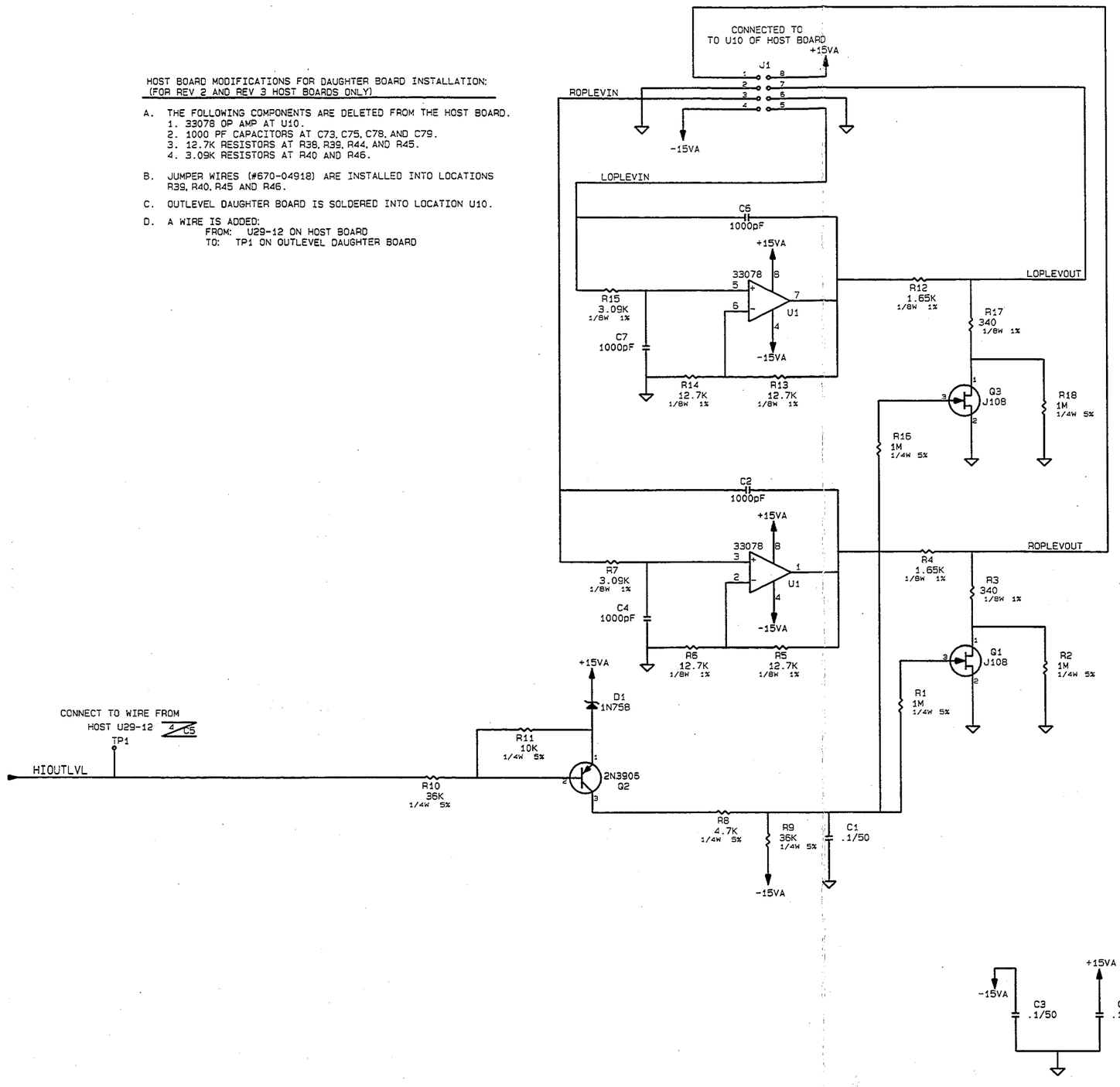
HOST BOARD MODIFICATIONS FOR DAUGHTER BOARD INSTALLATION:
(FOR REV 2 AND REV 3 HOST BOARDS ONLY)

A. THE FOLLOWING COMPONENTS ARE DELETED FROM THE HOST BOARD.
   1. 33078 OP AMP AT U10.
   2. 1000 PF CAPACITORS AT C73, C75, C78, AND C79.
   3. 12.7K RESISTORS AT R38, R39, R44, AND R45.
   4. 3.09K RESISTORS AT R40 AND R46.

B. JUMPER WIRES (#670-04918) ARE INSTALLED INTO LOCATIONS R39, R40, R45 AND R46.

C. OUTLEVEL DAUGHTER BOARD IS SOLDERED INTO LOCATION U10.

D. A WIRE IS ADDED:
   FROM: U29-12 ON HOST BOARD
   TO: TP1 ON OUTLEVEL DAUGHTER BOARD



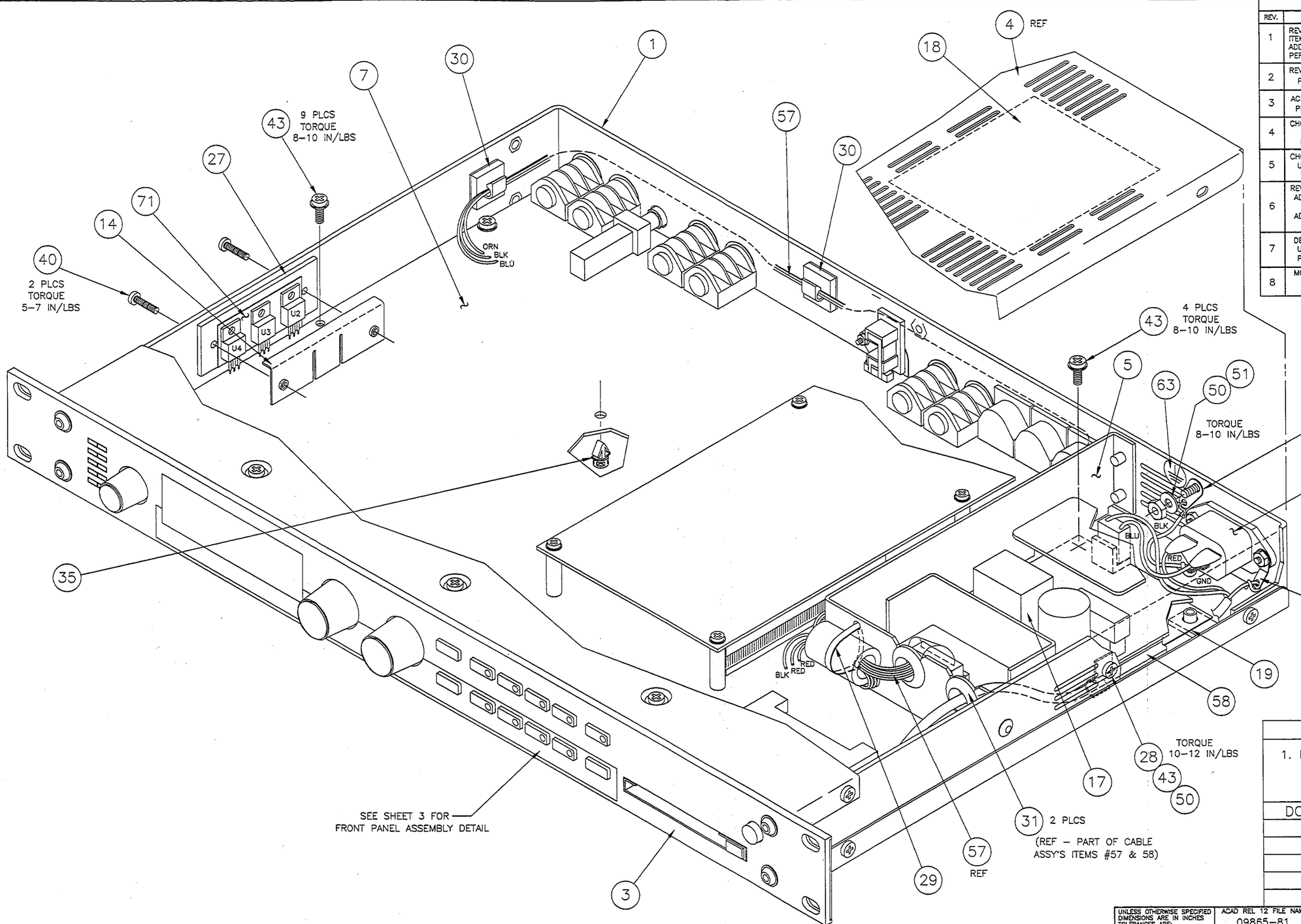
REVISIONS			
REV	DESCRIPTION	DRAFTER/CHECKER	D.E./AUTHORIZED

NOTES

1. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
2. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
3. DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
4. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
5. REFERENCE DESIGNATORS, LAST USED: U1, R18, C7, Q3, D1, J1

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEM, OUTLEVEL BD, PCM-80 ANALOG OUTPUT DAUGHTER BRD
DRAWN RWH	5/20/94	
CHECKED AF	5/25/94	SIZE: B; CODE: ; NUMBER: 060-10341; REV: 0
G.C. CW	7/6/94	
ISSUED KE	7/6/94	SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	REVISED WIRING AT AC CONN, ITEM 43 CHG'D TO SEMS, ADDED ITEM 27 PER DCR #931019-00	AN 10/21/93 MK 10/22/93	CB 10/25/93
2	REVISED WIRING AT AC CONN PER PCR #931109-00	AN 11/12/93 MK 11/17/93	CW 11/17/93 CB 11/23/93
3	AC CONN MOVED TO INSIDE PER DCR #931217-01	AN 12/20/93 MK 12/20/93	CW 12/20/93 CB 12/22/93
4	CHG COVER HOLE PATTERN & PROT. COVER SIZE PER PCR #940202-00	AN 3/11/94 MK 3/14/94	CW 3/14/94 CB 3/28/94
5	CHG SHEET 4 ITEM 68 UPDATED DOC. CTL BLK PER ECO #940609-00	JV 6/28/94 AN 6/28/94 MK 6/29/94	CW 6/30/94 CB 7/13/94
6	REV'D COVER & INSERT TO ADD 4 SCREWS (ITEM 42) PER ECO #941007-00 ADD GASKET (ITEM 76) PER ECO #941028-00	AN 11/3/94 MK 11/4/94	CW 11/10/94 DHS11/10/94
7	DELETED GASKET (ITEM 76) UPDATED DOC. CTL BLK PER ECO #950209-00	AN 3/9/95 MK 3/14/95	CW 5/18/95 CB 5/26/95
8	MOVED PARTS TO AC PWR CABLE ASSY PER ECO #950530-00	AN 8/4/95 MK 8/7/95	CW 9/5/95 CB 9/6/95



NOTES
1. REFER TO SHEET 4 FOR PART NUMBER LISTING.

DOCUMENT CONTROL BLOCK	
SHEET	REV
1 OF 4	8
2 OF 4	6
3 OF 4	3
4 OF 4	7

NEXT ASSY	PCM-80
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME: 09865-81

APPROVALS		DATE
DRAWN	AN	7/2/93
CHECKED	MK	9/7/93
Q.C.	CW	9/7/93
ISSUED	AF	9/8/93

lexicon

TITLE: ASSY DWG, CHASSIS, PCM-80

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-09865	8

SCALE 1/1 SHEET 1 OF 4

LEXICON, INC.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	REVISED LABEL POSITIONS, ADDED ITEMS 41, 62 & 74 PER DCR #931019-00	AN 10/21/93 MK 10/22/93	CB 10/25/93
2	REVISED AC CONN DETAIL, PER PCR #931109-00 ADDED COVER ITEM 73 PER DCR #931115-00	AN 11/12/93 MK 11/17/93	CW 11/17/93 CB 11/23/93
3	AC CONN MOVED TO INSIDE PER DCR #931217-01	AN 12/20/93 MK 12/20/93	CW 12/20/93 CB 12/22/93
4	REVISED THKN'S & HARDWARE FOR COVER ITEM 73 PER PCR #940128-00, & #940304-00	AN 3/11/94 MK 3/14/94	CW 3/14/94 CB 3/28/94
5	REV'D COVER & INSERT TO ADD 4 SCREWS (ITEM 42) PER ECO #941007-00	AN 11/3/94 MK 11/4/94	CW 11/10/94 DHS 11/10/94
6	MOVED PARTS TO AC PWR CABLE ASSY PER ECO #950530-00	AN 8/4/95 MK 8/7/95	CW 9/5/95 CB 9/6/95

2 PLCS 34
24
REF (21) (PART OF CABLE ASSY ITEM #58)
45 2 PLCS TORQUE 4-6 IN/LBS
29 REF
73
49 41 2 PLCS TORQUE 5-7 IN/LBS
60
74
8
38 4 PLCS TORQUE 4-6 IN/LBS
RED BLK
58 REF
50 43 28 REF
5 REF
36 4 PLCS
61
17 REF
J16
2
59
62
46 33 4 PLCS TORQUE 10-14 IN/LBS
J9
J8
PIN 1
J7
49 39 2 PLCS TORQUE 5-7 IN/LBS
20 REF (PART OF CABLE ASSY ITEM #58)
54 3 PLCS
47 3 PLCS TORQUE 4-6 IN/LBS
30
J4
56
37
48
52 TORQUE 4-6 IN/LBS
66
65
4 2 PLCS
67 64 69 68 24
ORIENT LABELS TO BE READ FROM THE REAR OF UNIT
42 16 PLCS TORQUE 10-12 IN/LBS
NUT SUPPLIED WITH CONNECTOR (P/N 510-09975) DISCARD WASHER - 6 PLCS TORQUE 5-7 IN/LBS
6

NOTES

1. REFER TO SHEET 4 FOR PART NUMBER LISTING.

	PCM-80
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX +/-.010
XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME 09865-62

APPROVALS		DATE
DRAWN	AN	7/2/93
CHECKED	MK	9/7/93
Q.C.	CW	9/7/93
ISSUED	AF	9/8/93

lexicon

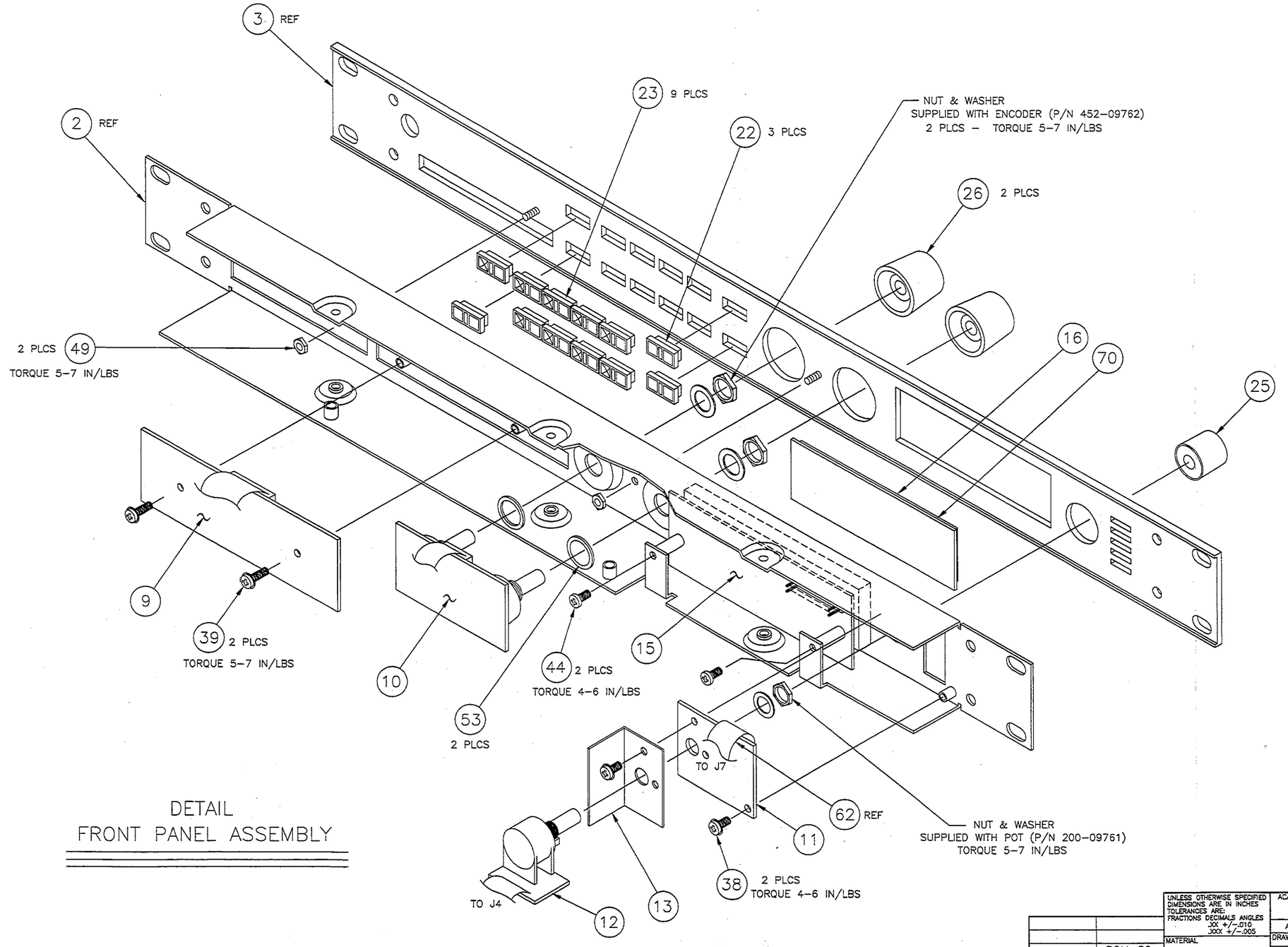
TITLE ASSY DWG, CHASSIS, PCM-80

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-09865	6

SCALE 1/1 SHEET 2 OF 4

LEXICON, INC.

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADDED WASHERS ITEM 53 PER DCR #931019-00	AN 10/21/93 MK 10/22/93	CW 11/17/93 CB 10/25/93
2	REV'D PICTORIAL OF INSERT PER ECO #941007-00 ADDED GASKET ITEM 76 PER ECO #941028-00	AN 11/3/94 MK 11/4/94	CW 11/10/94 DHS 11/10/94
3	DELETED GASKET ITEM 76 PER ECO #950209-00	AN 3/9/95 MK 3/14/95	CW 5/18/95 CB 5/26/95



DETAIL
FRONT PANEL ASSEMBLY

NOTES
1. REFER TO SHEET 4 FOR PART NUMBER LISTING.

	PCM-80
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME 09865-33

APPROVALS		DATE
DRAWN	AN	7/2/93
CHECKED	MK	9/7/93
Q.C.	CW	9/7/93
ISSUED	AF	9/8/93

lexicon

TITLE ASSY DWG, CHASSIS, PCM-80

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-09865	3

SCALE 1/1 SHEET 3 OF 4

LEXICON, INC.

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
1.	700-09853	CHASSIS, WRAPAROUND, PCM-80	1	
2.	700-09856	CHASSIS, INSERT, FP, PCM-80	1	
3.	702-09850	PANEL, FRONT, PCM-80	1	
4.	700-09857	COVER, TOP/BOTTOM, PCM-80	2	
5.	700-09859	BRACKET, PWR SUP, PCM-80	1	
6.	703-09854	PANEL, OVLY, REAR, PCM-80	1	
7.	022-09803	PL, HOST BD ASSY, PCM-80	1	
8.	022-09804	PL, DSP BD ASSY, PCM-80	1	
9.	024-09840	PL, FP SWITCH BD ASSY, PCM-80	1	
10.	024-09841	PL, FP ENCODER BD ASSY, PCM-80	1	
11.	024-09842	PL, FP HEADROOM BD ASSY, PCM-80	1	
12.	024-09814	PL, FP LVL POT BD ASSY, PCM-80	1	
13.	701-09860	BRACKET, POT SHIELD, PCM-80	1	
14.	701-09863	CLAMP, HEATSINK, TO-220	1	
15.	430-09785	DISPLAY, VF, 20X2 CHAR, 5X7 DOT	1	
16.	703-09862	LENS, DISPLAY, PCM-80	1	
17.	750-09766	PWR SUP, 5V@5A/+15V@2A/-15@.5A	1	
18.	702-09858	COVER, PROTECTIVE, TOP, PS, PCM-80	1	
19.	702-09861	COVER, PROTECTIVE, BOT, PS, PCM-80	1	
20.	490-00798	CONN, AC, 3MC, BULKHD, IEC, 6A	1	
21.	453-09868	SW, PBPLP, 1P1T, PCRA, 2.5MM TRAV	1	PWR SW
22.	550-09759	BUTTON, .20X.50, BLK	3	
23.	550-09760	BUTTON, .20X.50, BLK, W/LENS	9	
24.	550-03827	BUTTON, .346RD, BLK	2	PWR SW, LVL SW
25.	550-09087	KNOB, 15MM, 6MM/FLAT, BLK	1	LVL POT
26.	550-09767	KNOB, 21MM, 6MM/FL, BLK/BLK	2	ENCODERS
27.	702-09988	PLATE, HEATSINK, TO-220	1	
28.	530-09979	CLAMP, CABLE, .169", ZN	1	AC INPUT CABLE
29.	530-02488	TIE, CABLE, NYL, .14"X5 5/8"	1	PS TO HOST CABLE
30.	530-09382	CLIP, WIRE HRNS, .15DIA, ADH BAK	3	PS TO HOST CABLE
31.	540-00874	GROMMET, 9/16 OD, 7/16 ID	2	PS BRKT
32.	620-01999	LUG, SOLDER, LCKNG, #6, .020THK	1	CHASSIS GND
33.	630-02737	WSHR, FL, #8CLX.02 THK, BLK, NYL	4	FP TO CHASSIS
34.	630-03669	SPCR, #4CLX3/8, 3/16RD, NYL	2	PWR SW SUPPORT
35.	630-09709	SPCR, PCB/FOOT, .188, NYL	1	HOST BD
36.	635-09770	SPCR, SWAGE, 4-40X7/8, 1/4RD, BR	4	HOST BD/ DSP BD
37.	640-09698	SCRW, 2-56X5/8, PNH, PH, ZN	1	RCA CONN TO CHASSIS
38.	640-04339	SCRW, 4-40X1/4, PNH, PH, SEMS, ZN	6	HEADROOM BD TO INSERT (2) DSP BD TO HOST BD (4)
39.	640-01706	SCRW, 4-40X3/8, PNH, PH, ZN	4	SWITCH BD TO INSERT (2) AC CONN TO CHASSIS (2)
40.	640-01700	SCRW, 4-40X1/2, PNH, PH, SS	2	H/S CLAMP TO CHASSIS
41.	640-02034	SCRW, 4-40X5/8, PNH, PH, ZN	2	MEM CARD CONN TO HOST BD
42.	640-03957	SCRW, 6-32X3/16, TH, PH, BLK	16	COVERS TO CHASSIS & INSERT
43.	640-09987	SCRW, 6-32X5/16, PNH, PH, SEMS, ZN	14	HOST BD TO CHAS, INSERT & PS BRKT (9) PWR SUP TO CHAS & PS BRKT (4) AC CABLE CLAMP TO CHASSIS (1)
44.	640-07696	SCRW, M3X8MM, PNH, PH, ZN	2	DISPLAY TO INSERT
45.	640-09758	SCRW, M3X16MM, FH, PH, ZN	2	PWR SW TO CHASSIS
46.	640-02736	SCRW, 8-32X3/8, BH, SCKT, BLK	4	FP TO CHASSIS
47.	641-09699	SCRW, TAP, AB, #2 X 5/16, PNH, PH, ZN	3	MIDI CONN TO CHASSIS
48.	643-01855	NUT, 2-56, HEX, ZN	1	RCA CONN TO CHASSIS
49.	643-01732	NUT, 4-40, KEP, ZN	6	FP TO INSERT (2) AC CONN TO CHAS (2) MEM CARD CONN TO HOST BD (2)
50.	643-01728	NUT, 6-32, KEP, ZN	2	CHASSIS GND (1) AC CABLE CLAMP (1)
51.	644-01735	WSHR, FL, #6CLX3/8 ODX1/32 THK	1	CHASSIS GND
52.	644-06635	WSHR, INT STAR, #2, ZN	1	RCA CONN TO CHASSIS
53.	644-07893	WSHR, FL, .427 IDX .550 ODX .035THK, ZN	2	ENCODER BD TO INSERT
54.	650-05899	POPRVT, 5/32X1/4, REG PROT HD, AL	3	PS BRKT TO CHASSIS
55.				
56.	670-09817	CABLE, RIB, 24-26AWG, 7CX .1, 1"L	1	LVL POT BD TO HOST BD
57.	680-09755	CABLE, HSG/ST&T, 6C, 30/8.5, SLV	1	PS TO HOST BD
58.	680-09756	CABLE, AC PWR, SHLD, 14"	1	AC CONN TO PS & PWR SW
59.	680-09757	CABLE, XITION/SCKT, 20C, 6.0"	1	DISPLAY TO HOST BD
60.	680-09763	CABLE, .079, SCKT/SCKTRA, 10C, 2.0"	1	SWITCH BD TO HOST BD
61.	680-09764	CABLE, .079, SCKT/SCKTRA, 6C, 2.0"	1	ENCODER BD TO HOST BD
62.	680-10181	CABLE, RIB, 24-28AWG, 7C X .1", 5.5"	1	HEADROOM BD TO HOST BD
63.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	CHASSIS GND
64.	740-10160	LABEL, CE94	1	TOP COVER
65.	740-09175	LABEL, .65 X .20, DATE CODE	1	REAR PANEL
66.	740-09176	LABEL, .65 X .20, S/N	1	REAR PANEL
67.	740-09980	LABEL, WARNING/APPROVAL, PCM-80	1	TOP COVER
68.	740-06678	LABEL, CSA CERTIFIED, CONSUMER	1	TOP COVER
69.	740-08558	LABEL, TUV CERTIFIED, BAYERN	1	TOP COVER
70.	120-09571	ADHESIVE, CONTACT CEMENT	0.03oz	DISPLAY LENS TO FRONT PANEL
71.	630-09983	INSUL, SEMI, SIL RUB, ADH, 1.95 X 1.00	1	CHASSIS UNDER REGULATORS
72.				
73.	710-10190	PC BD, MEM CD CONN CVR, PCM-80	1	HOST BD
74.	510-09985	CONN, MEM CARD, 68 PIN, EJECTOR	1	HOST BD
75.	620-06638	LUG, SOLDER, LCKING #4	1	AC CABLE GND

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
5	ITEM 42 QTY CHG'D FROM 12 TO 16 PER ECO #941007-00 & ADDED GASKET ITEM 76 PER ECO #941028-00	AN 11/3/94 MK 11/4/94	CW 11/10/94 DHS11/10/94
6	DELETED GASKET #630-10371 PER ECO #950209-00	AN 3/9/95 MK 3/14/95	CW 5/18/95 CB 5/26/95
7	MOVED PARTS TO AC PWR CABLE ASSY PER ECO #950530-00	AN 8/4/95 MK 8/7/95	CW 9/5/95 CB 9/6/95

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ITEM 43 WAS #640-01713, ADDED ITEMS 27, 41, 53, 62, & 74 PER DCR #931019-00	AN 10/21/93 MK 10/22/93	CB 10/25/93
2	ADDED ITEMS 41, 73 ,75 QTY CHG ITEMS 40, 43, 49, 50, 54 PER PCR #931109-00 & DCR #931115-00	AN 11/12/93 MK 11/17/93	CW 11/17/93 CB 11/23/93
3	QTY CHG ITEMS 40, 49; P/N CHG ITEMS 41, 62, 64 & 73 PER PCR'S #940128-00, #940131-01, #940304-00, & #940310-00	AN 3/11/94 MK 3/14/94	CW 3/14/94 CB 3/28/94
4	ITEM 58 WAS #740-08471, PER ECO#940609-00	JV 6/28/94 AN 6/28/94 MK 6/29/94	CW 6/30/94 CB 7/13/94

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERCEDE THE BILL OF MATERIAL #021-09802.

NEXT ASSY	PCM-80
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME: 09865-74

APPROVALS		DATE
DRAWN	AN	6/23/93
CHECKED	MK	9/7/93
Q.C.	CW	9/7/93
ISSUED	AF	9/8/93

lexicon

TITLE: ASSY DWG, CHASSIS, PCM-80

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-09865	7

SCALE NONE | SHEET 4 OF 4

LEXICON, INC.