PCM 81

Digital Effects Processor

Service Manual

Lexicon

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturer's operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure... voltage that may be sufficient to constitute a risk of shock.

This triangle, which appears on your component, alerts you to important operating and maintenance instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems."

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

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Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.

*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when:

the power supply cord or the plug has been damaged,

objects have fallen, or liquid has been spilled into the unit,

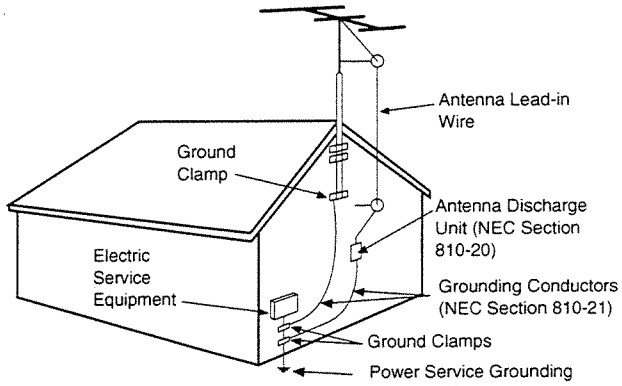
the unit has been exposed to rain,

the unit does not appear to operate normally or exhibits a marked change in performance,

the unit has been dropped, or the enclosure damaged.

Outdoor Antenna Grounding If an outside antenna is connected to the receiver, be sure the antenna system is grounded so as to provide some protection against voltage surges and built-up static charges. Section 810 of the National Electrical Code, ANSI/NFPA No. 70-1984, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna-discharge unit, size of grounding conductors, location of antenna-discharge unit, connection to grounding electrodes, and requirements for the grounding electrode. See figure below.

Power Lines An outside antenna should be located away from power lines.



NEC — National Electrical Code

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

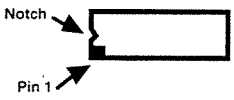
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

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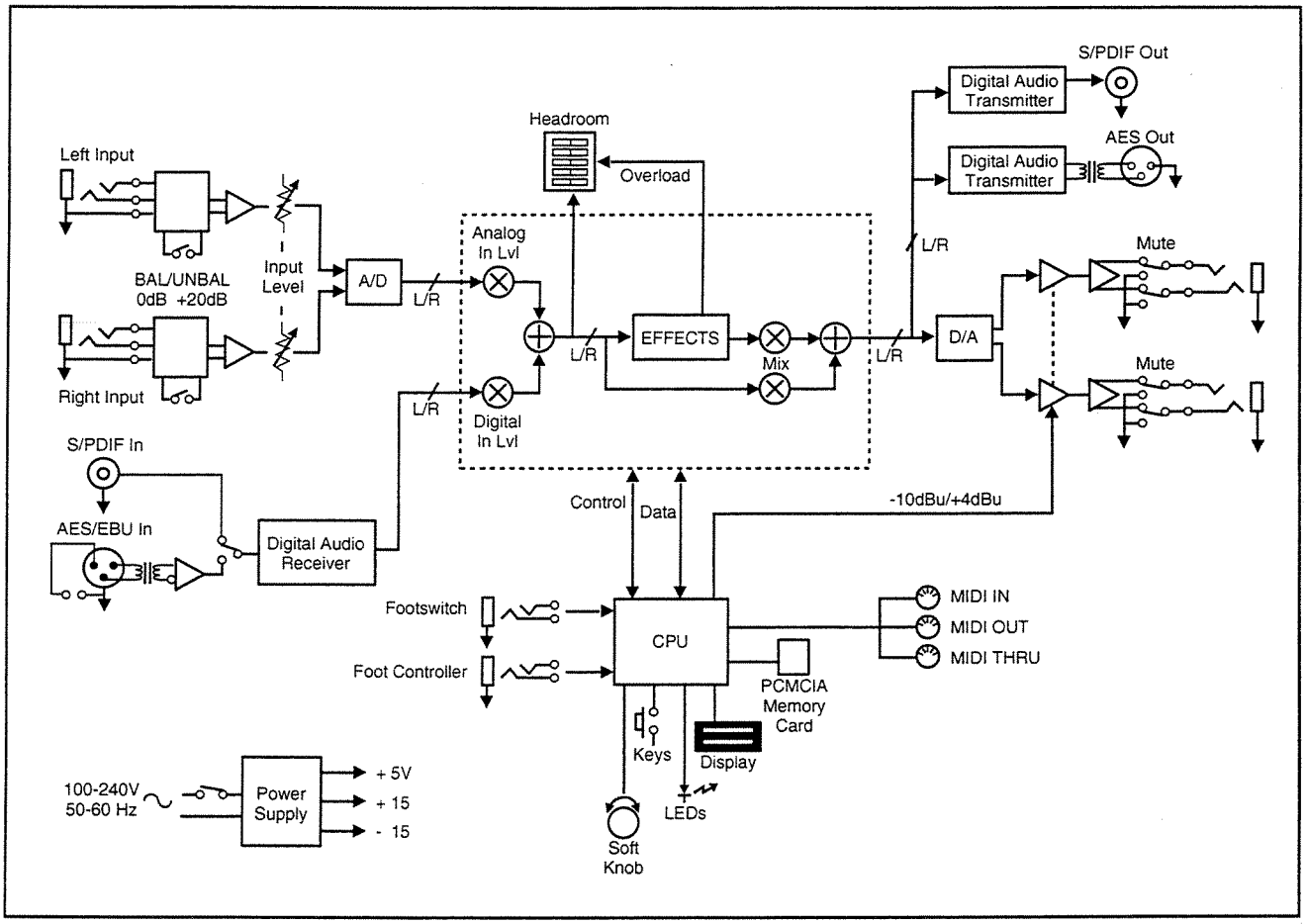
Product Overview

Block Diagram



The Front Panel

Headroom
5-position indicator for analog and digital signal levels and overload conditions.

INPUT
Adjusts analog input level.

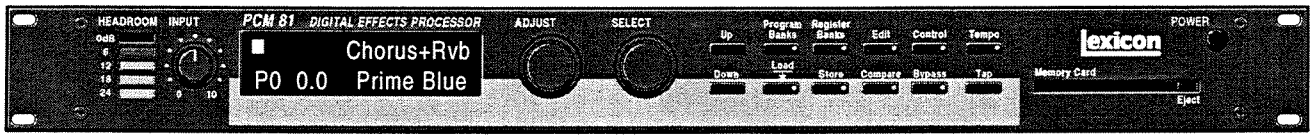
Display
Two rows of 20 alphanumeric characters display effect names and ID numbers, and parameter names and values.

ADJUST
In Edit mode, changes values of parameters chosen with SELECT. With Program Banks or Register Banks selected, behaves as a soft knob for patched parameters.

SELECT
Scrolls through presets, registers or parameters. With Program Bank or Register Bank selected, scrolls through the 50 programs in the selected bank. With Edit selected, scrolls only through the parameters of the active row.

POWER
On/Off.

Memory Card
Slot for optional preset ROM or register RAM cards. Press Eject button to remove card.



Up/Down
Press to move up and down through a program, register, or parameter matrix.

Program Banks
Enables selection of factory presets. Press repeatedly to cycle selection of 4 internal preset banks. Press and hold to display the name of the current bank.

Load/*
In Program or Register mode, loads the selected program. In Edit mode, scrolls through any multi-field parameter.

Register Banks
Enables selection of user memory. If a RAM card is loaded into the Memory Card slot, each press of this button selects a new register bank. Press and hold to display the name of the current bank.

Store
Initiates register store function.

Edit
Enables parameter selection for editing of values.

Compare
Active in Program, Register, and Edit modes. Press to compare the active version of the current effect with the most recently stored version.

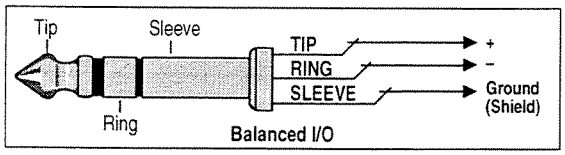
Control
Enables selection of system and global parameters.

Bypass
Bypasses or mutes audio, depending on the setting of each program's bypass parameter.

Tempo
Press to display tempo rate and to initiate tempo functions. LED flashes in time with current tempo rate.

Tap
Sets tempo. Press twice in rhythm to establish tempo rate. Press once to reset LFO.

The Rear Panel



Balanced Outputs

Output impedance is 50Ω, each side, balanced, and levels up to +18dBu maximum full scale. 1/4" phone connectors and XLRs provided. Both S/PDIF and AES outputs are active at all times.

Input Level

2-position (In/Out) switch for matching input gain to the source being used. In position adds 20dB of gain to the input stages. Out position provides 0dB of gain. Either position may be used for balanced or unbalanced sources.

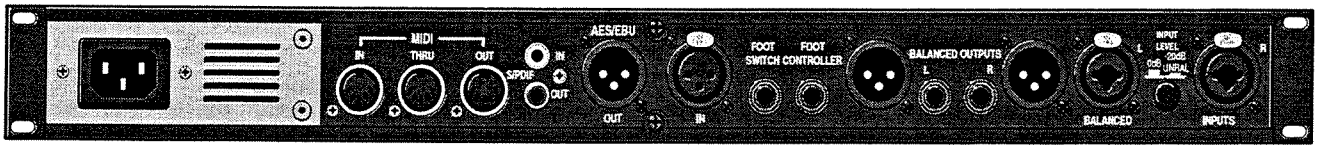
Balanced Inputs

Combined 3 pole XLR and 1/4" jacks, electronically balanced.

Input impedance is 50kΩ unbalanced, and 100kΩ balanced. Inputs accept input levels from -22dBu to +20dBu.

AES/EBU and S/PDIF Inputs

AES/EBU format digital connectors conform to AES 3-1992 and EBU professional standards. S/PDIF format digital connectors conform to IEC-958 consumer standards. Only one of these options (AES or S/PDIF) may be selected for input.



AC Power

Standard 3-pin IEC power connector. 100-240V, 50-60Hz automatic switching to correct voltage range.

MIDI

IN

Receives MIDI information from other MIDI equipment such as master keyboard controllers, MIDI foot controllers, sequencers and synthesizers.

THRU

Passes any MIDI data received without change.

OUT

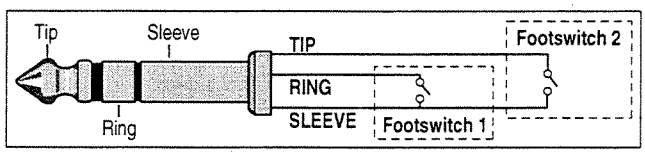
Transmits MIDI data to other equipment.

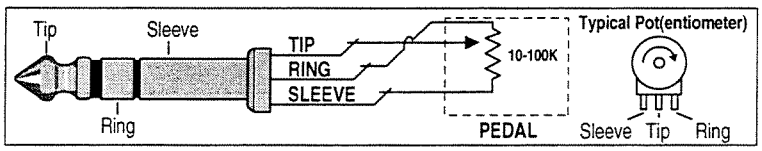
Footswitch

1/4" Tip/Ring/Sleeve phone jack for two independent momentary footswitches

Foot Controller

1/4" Tip/Ring/Sleeve phone jack provided for footpedal with 10kΩ to 100Ω impedance.





Installation Notes

Mounting

The PCM 81 uses one EIA-standard rack space, and can be mounted on any level surface or in a standard 19 inch (483 mm) rack. If the PCM 81 is mounted in a rack or road case, support the rear of the chassis to prevent possible damage from mechanical shock and vibration.

The maximum ambient operating temperature is 104°F (40°C). Provide adequate ventilation if the PCM 81 is mounted in a closed rack with heat-producing equipment such as power amplifiers.

Power Requirements

The PCM 81 is equipped with a 3-pin IEC power connector and detachable cord.

The PCM 81 will operate with power sources from 100 to 240 volts AC, 50-60Hz. Power switching to actual line voltage is automatic.

Audio Connections

Analog Audio

For best performance, maintain balanced connections, and use high-quality, low-capacitance, twisted-shielded pair cable.

When connecting to single-ended, unbalanced devices, connect the low side to signal ground at the unbalanced piece of equipment. Output level does not change when connected to an unbalanced input.

Mono Applications

Use a Y-connector inserted at the analog inputs and outputs to have the signal summed to mono.

NOTE

Be careful to keep input and output to all channels wired consistently. Out-of-phase wiring can produce audible effects.

Digital Audio

S/PDIF (IEC-958) Consumer Digital Audio connections require 75Ω coaxial cable suited for digital audio or video signals. Audio grade cable is *not* suitable.

AES/EBU connections require balanced connections using high-quality, low-capacitance, controlled-impedance, data communication, twisted-shielded pair cable. **Microphone cable may introduce a significant amount of jitter into the signal, causing distortion.**

Control Connections

Footswitch/Foot Controller

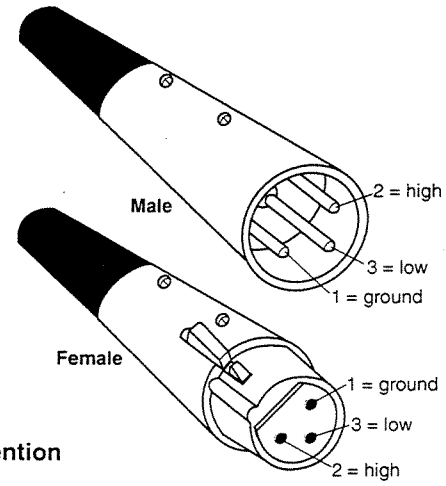
One 1/4 inch T/R/S phone jack is provided for 2 momentary footswitches. Another 1/4 inch T/R/S phone jack is provided for a footpedal (minimum 100Ω to maximum 10k impedance). Normally open or normally closed momentary switches are suitable. At power on, the PCM 81 assumes the switch is off. Use shielded, twisted-pair cable with shield connected to sleeve. See diagram on page 3.

MIDI

5-pin DIN connectors are provided for MIDI IN, THRU and OUT. Use standard 5-pin DIN MIDI cable assemblies, available from your local dealer.

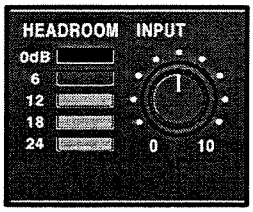
Connectors

Signal	Mating Connector	Description
L and R Analog Audio Input	XLR A3M	Active balanced, pin 2 high +2dBu min; +20dBu max at 0dB setting
L and R Analog Audio Output	XLR A3F	Active balanced, pin 2 high -2dBu to +18dBu at full scale output
AES/EBU Digital Input	XLR A3M	AES 3-1992 Professional Digital Audio Format, balanced, pin 2 high
AES/EBU Digital Output	XLR A3F	AES 3-1992 Professional Digital Audio Format, balanced, pin 2 high
S/PDIF CP-340 Type II Consumer Digital Audio Input and Output	RCA	IEC-958 Consumer Digital Audio Format tip high
MIDI In MIDI Out MIDI Thru	5-pin DIN	Standard MIDI Interface



pin 2 high by convention

Setting Audio Levels



The PCM 81, with both analog and digital input and output connections, requires some attention to proper setting of signal level.

Analog inputs are first gain-conditioned by the rear panel input gain switch, and then by the front panel INPUT knob. Proper setting of both the switch and knob are important for best performance of the A/D converter. Audio data from the A/D converter is level adjusted by the Analog Lvl parameter before reaching the effects processors. Digital inputs are also level adjusted before reaching the effects processors via the Digital Lvl parameter.

Analog and the selected digital source are mixed at the input to the effects processors. For example, setting both Analog Lvl and Digital Lvl to 50% will mix the analog and the selected digital input signals equally and send them to the effects. Creating a mix which exceeds 100% can cause overload.

Proper setting of Input level on the PCM 81 is dependent on:

- Proper signal level into the analog front end to avoid signals causing overload at the DSP input
- Proper adjustment of the signal level into the analog-to-digital converter to optimize noise and avoid overload
- Proper setting of signal level into the digital signal processor to optimize noise.

Headroom Display

The headroom display provides both headroom and overload information from a variety of measurement points. The meters display the sum of both the analog and the digital input data. Examining either the analog or the digital level alone requires that the Level parameter of the subject data stream be set to 100%, while the Level parameter of the other is set to 0%.

The chart below illustrates the adjustment range that will set input levels for both balanced and unbalanced operation.When a choice can be made, it is best to operate at the higher amplitude end of the recommended range to optimize noise performance.

	+20dB Gain	0dB Gain
overload:	> 0dBu	>+20dBu
acceptable:	0dBu to -22dBu	+20dBu to -2dBu
too low (noisy):	<-22dBu	<-2dBu

Overload

The 0db (overload) indicators will light under the following conditions:

- A/D overload
- overload at any point in effects processing

For example, internal peaking of high Q filters, or level buildup from certain reverberation modes can result in overload, even when the input A/D or digital receiver data stream is not at full scale. Such conditions are most often caused by a combination of extreme parameter settings. Adjusting parameter/level settings can eliminate these overload conditions.

Selecting a Digital Input Source

1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.0 Word Clock**, and turn ADJUST to display **Ext: XLR or Ext: Coax**, depending on the input you are using.

Selecting Word Size

1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.3 Word Size**, and turn ADJUST to display desired Word Size.

   NOTE: When using analog outputs as primary outputs, set **Word Size** to **20 bits**.

Setting Analog and Digital Input Level

1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.2 Dig In Lvl**, and turn ADJUST to display **0%.**

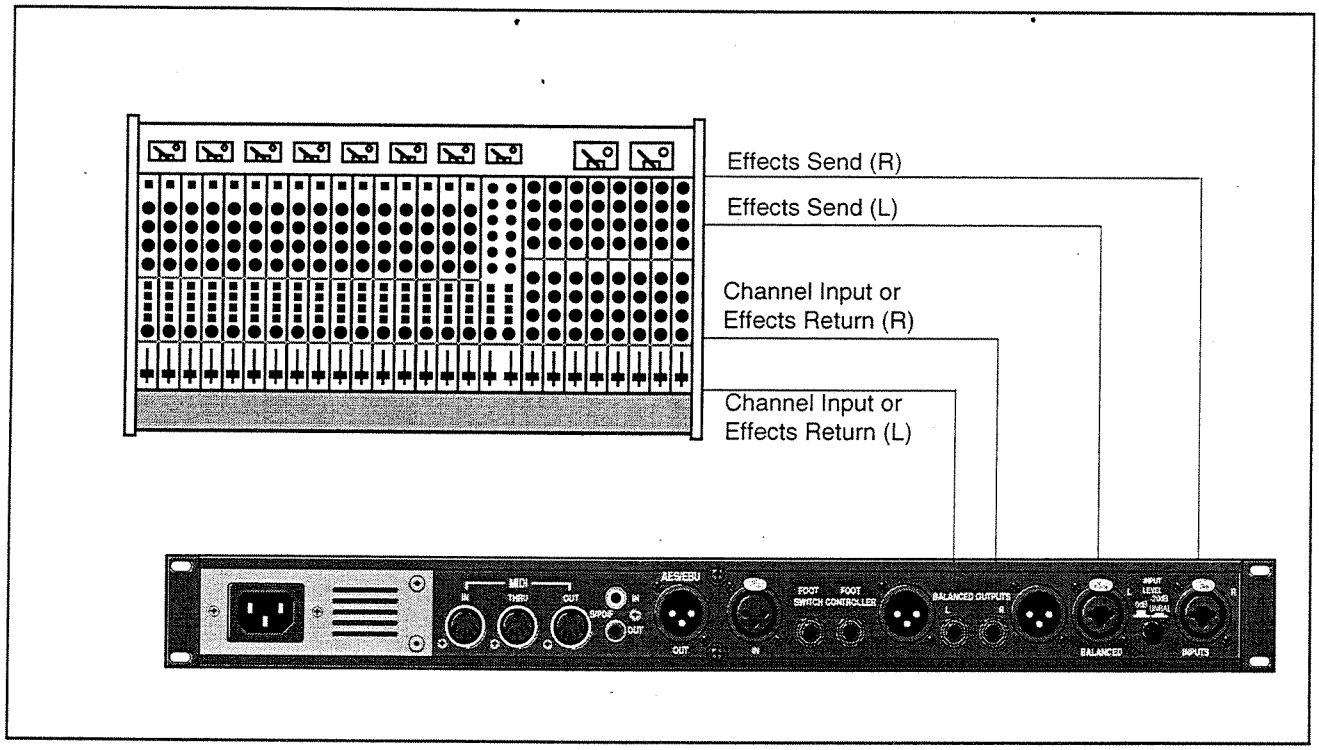
   NOTE: If you are not running digital audio, controlled by External Clock, into the PCM 81, the digital audio input will be disabled or muted. Until there is valid digital audio input, select **0.0 External** to enable the digital input level control. Until valid digital audio is connected, the **Dig In Lvl** control will remain muted.
4. Turn SELECT to **0.1 Analog In Lvl**, and turn ADJUST to display **100%.**
5. Adjust the front panel INPUT knob so that program material level peaks cause the headroom display to reach the top of the column *without* lighting the overload indicators. An occasional large signal peak causing momentary flashing of the overload indicator is acceptable in most instances, but should be validated by listening to the actual result.
6. If you are running digital audio, turn SELECT back to **0.2 Dig In Lvl**, and turn ADJUST to the desired level. You may want to back off the **Analog In Lvl** setting to prevent the analog/digital mix from overloading the effects processor.

Setting Output Level

While still in Control mode, turn SELECT to **0.6 Output Level**. The Output Level parameter has two range positions. The appropriate position depends on the level handling capability of the device connected to the analog outputs. Devices capable of handling outputs with peak levels of 18dBu require setting **Output Level** to the **+4dBu** setting. Devices which cannot handle peak levels greater than +4dBu require the **-10dBu** setting.

Configurations

Connection to a mixing console's effects sends



If you will be using a PCM 81 as your primary effects unit, and your system includes a console with one or more auxiliary (effects) sends, connect the PCM 81 as shown above. In most applications, it is preferable to connect the PCM 81 outputs to two of the console's input channel strips, panned full left and right, rather than to the effects returns. This allows the greatest flexibility in routing and equalization.

In this configuration the console controls are used to set the amount of effect heard—the PCM 81's MIX control should be set for 100% wet. To assign a global MIX setting:

1. Press **Control.**
2. Press **Up** or **Down** until **1.x** is displayed in the lower left of the display and **System** is displayed on the upper line.
3. Turn SELECT until **System Mix Mode** is displayed on the upper line. **1.1** will be displayed in the lower left.
4. Turn ADJUST until the lower line reads:

   1.1 ✱ Global
5. Press **Load /✱** to show the current global setting of MIX; use ADJUST to set it to 100% wet.

Memory Cards

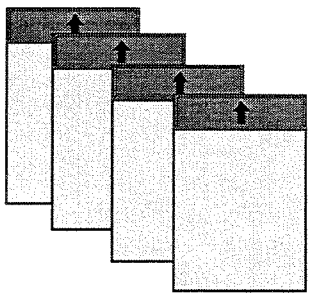
You can use Memory cards to store as many as 2350 PCM 81 registers (47 banks of 50 — on a 1 Meg card). Registers stored on a properly formatted card will be recognized whenever the card is inserted, and can be accessed via the front panel **Register Banks** button, exactly as internal registers.

Memory cards can also be used to store "setups" (your system configuration, as set in Control mode). As many as 5 PCM 81 setups can be stored on a card, allowing you to transport not only your effects, but complete PCM 81 environments to another PCM 81. Cards also provide storage for additional program maps and effect chains.

See *Control Mode* Store and Load functions for details on saving setups on a card and reloading them.

Memory cards must be of the following type:

PCMCIA SRAM Memory Card — 68 pin, Type I	
Usable densities:	64 kByte 128 kByte 256 kByte 1 MByte
Access Time:	250 nsec or faster
Conforms to PCMCIA 2.0/JEDIA 4.1. Can use either 8-bit or 8/16-bit bus configuration. Attribute memory can be present, but is not used.	



Memory cards can be used to store PCM 81 registers, or setups.

Periodic Maintenance

Under normal conditions the PCM 81 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon, Inc.
3 Oak Park
Bedford MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499
ATT: Customer Service

Returning units for service

Before returning a unit, for warranty or non-warranty service, consult with Lexicon to determine the extent of the problem, and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return a PCM 81 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, both inside and outside of package

Please enclose a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Service personnel.

2

PCM 81 Specifications

Audio Input	**Connectors:**	Combined 3 pole XLR and 1/4 inch T/R/S phone jacks (2)
	Impedance:	0 dB/BAL switch position: 100kΩ, balanced -20 dB/UNBAL switch position: 50kΩ, unbalanced
	Levels:	0 dB/BAL switch position: -2 dBu min for full scale, +20 dBu max -20 dB/UNBAL switch position: -22 dBu min for full scale, 0 dBu max
	CMRR:	0 dB/BAL switch position: 50 dB minimum, 10 Hz to 20 kHz
Audio Output	**Connectors:**	1/4 inch T/R/S phone jacks (2); balanced XLRs, pin 2 "high" (2)
	Impedance:	100Ω, balanced
	Levels:	+18 dBm, full scale (+4 dBu setting) balanced, unbalanced +4 dBm, full scale (-10 dBu setting)
	Protection:	Relays provided for output muting during power on/off
A/D Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-65 dB, 10 Hz to 20 kHz
	S/N Ratio:	>102 dB, 20 kHz bandwidth
	THD:	<0.003% max, 10 Hz to 20 kHz
	Dynamic Range:	>102 dB, 20 kHz bandwidth
	Delay:	24 samples (0.54 msec for 44.1 kHz, 0.50 msec for 48 kHz)
D/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-80 dB, 10 Hz to 20 kHz
	S/N Ratio:	>98 dB, 20 kHz bandwidth
	THD:	<0.005%, 10 Hz to 20 kHz
	Dynamic Range:	>98 dB, 20 kHz bandwidth
	Delay:	50 samples (1.13 msec for 44.1 kHz, 1.04 msec for 48 kHz)
A/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-55 dB, 10 Hz to 20 kHz
	S/N Ratio:	>96 dB, 20 kHz bandwidth
	THD:	<0.005%, 10 Hz to 20 kHz
	Dynamic Range:	>96 dB, 20 kHz bandwidth

Digital Audio Interface	**Connectors:**	Coaxial, RCA type (2); balanced, XLR (2)
	Format:	S/PDIF (IEC-958) and AES/EBU (AES3-1992) professional interface
	Sample Rates:	44.1 kHz, 48 kHz
Internal Audio Data Paths	**Conversion:**	20 bits
	DSP:	20 to 24 bits
External Memory Card	**Connector:**	Accepts PCMCIA Type I cards, 68 pins
	Standards:	Conforms to PCMCIA 2.0 / JEIDA 4.0
	Card Format:	Supports up to 1MB SRAM (attribute memory not required)
Control Interface	**MIDI:**	5-pin DIN connectors provided for MIDI IN, THRU, & OUT
	Footswitch:	1/4 inch T/R/S phone jack provided for 2 independent momentary footswitches System detects normal-open, or normal-closed on power up
	Foot controller:	1/4 inch T/R/S phone jack provided for footpedal (100Ω minimum, 10kΩ maximum impedance)
General	**Dimensions:**	19.0"W x 1.75"H x 12.0"D (483 x 45 x 305 mm) 19 inch rack mount standard, 1U high
	Weight:	Net: 6.4 lbs (2.9 kg) Shipping: 9.5 lbs (4.3 kg)
	Power Requirements:	100-240 VAC, 50-60 Hz, 35 W, 3-pin IEC power connector
	RFI/ESD:	Conforms to FCC Class B, EN55022 Class B (CE), IEC 801-2, IEC 801-3
	Environment:	Operating temperature: 32˚ to 104˚F (0˚ to 40˚C) Storage temperature: -22˚ to 167˚F (-30˚ to 70˚C) Humidity: maximum 95% without condensation

Unless otherwise noted, all audio specifications assume rear-panel switch set to BAL, input level control is set for unity gain (0dB), and analog I/O connections wired for balanced configuration.

Specifications subject to change without notice.

3

Performance Verification

Quick Performance Check

This section describes a quick verification of the normal operation of the PCM 81's internal processors and the integrity of the analog and digital audio signal paths. This procedure does not require extensive equipment or removal of the PCM 81 covers.

Diagnostics

When the PCM 81 is powered up, the unit will go through a self-test to verify proper operation of its internal system, and digital signal processors. When proper operation is confirmed, the unit exits the self-test mode and will briefly display the following message:

Lexicon PCM 81
Version n.nn

This message is followed by information on the amount of audio memory installed in the unit, and the final message: **Loading effect...** while the last effect used is loaded to the digital signal processors.

The following series of tests will be run automatically:

Host V40 CPU Test
ROM Checksum Test
Host (V40) SRAM Test
Display Test
Host (V40) Timer/Counter Test
Host (V40) Interrupt Mask Test
56k CPU and DRAM Test
Lexichip DRAM Test
Host (V40) DRAM Test
Battery Test
TACOchip Test

When the unit is powered on, all of the front panel switch LEDs and all of the display pixels are turned on. The display pixels remain on for approximately two seconds, during which time the first three diagnostic tests are run.

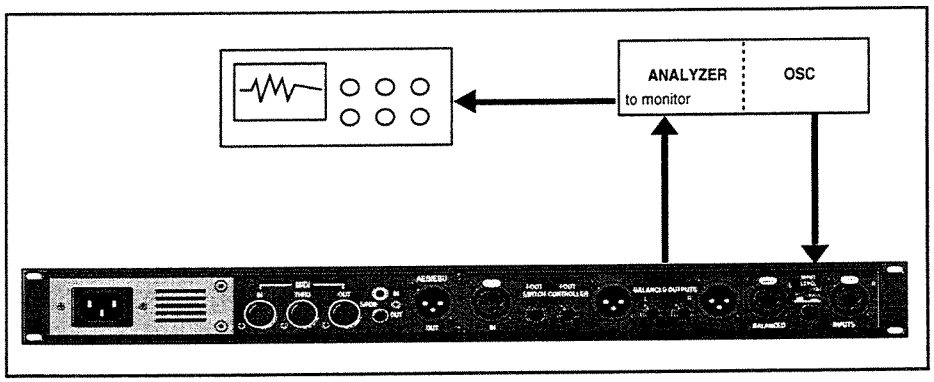
Once the Display Test is complete, and while the rest of the tests are running, the message **Memory Tests** is displayed. If the operator presses the front panel Compare button, the displayed message will change to **Extended Memory Test** and additional memory tests will be performed. The Extended Memory Test will also be run automatically if the SRAM is cleared.

When all the diagnostics have been executed, all of the headroom LEDs are turned on briefly while the unit is initializing, and **Lexicon PCM 81** appears on the display. Detailed descriptions of the Power On Diagnostics Tests are given in Chapter 4.

Analog Audio Performance Check

Required Equipment

- Low Distortion Oscillator with single-ended or balanced output,<100Ω output impedance, <0.005% THD.
- Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30 kHz high pass filter or audio bandpass (20-20 kHz) filter.
- Oscilloscope
- Audio Input Cable with shield and Male XLR or 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to Low Distortion Oscillator.
- Audio Output Cable with shield and Female XLR or 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to the Distortion Analyzer.
- Two (2) Audio Terminator Plugs, 1/4" with 600Ω-100kΩ resistor between tip and sleeve (single-ended configurations) or tip and ring (balanced configurations). An extra audio cable with a 1/4" connector at one end may be substituted if a termination plug is not available.



Setup

1. **Set Audio Word Clock to 48kHz**
   Turn the unit on and wait for the Power On Diagnostic cycle to finish, and the last used effect to be loaded. Once the effect is loaded, press **Control**. The light on the Control button should be lit, and the display should read:

   Audio *Word Clock
   0.0 Int: 48kHz

   If this display is not shown, simultanously press **Up** and Down to call the display. If the display shows **44.1kHz, turn ADJUST to the left once to select 48kHz**, before running the following tests.

2. **Set Analog In Lvl to 100%.**
   Turn SELECT once to the right to display the Analog Input Level parameter.

   Audio Analog In Lvl
   0.1 100%

   If the percent value is not 100% turn ADJUSTclockwise until 100% is displayed.

3. **Set Output Level to +4dBu.**
   Turn SELECT clockwise to select the Output Level parameter.

   Audio Output Level
   0.6 +4dBu

   If the Output Level is not set to +4dBu, turn ADJUST clockwise until +4dBu is displayed.

4. **Put the PCM 81 into Bypass mode.**
   Press **Down** once. The display should read:

   System Auto Load
   1.6 Off

   Turn SELECT counterclockwise until the following message is displayed:

   System*Bypass Mode
   1.3 InputMute

   Turn ADJUST clockwise until the display reads:

   System*Bypass Mode
   1.3 Bypass

   Press **Bypass on the front panel. T**he LED in the button should light and the display should briefly show the messsage:

   Bypass is on

5. **Connect the audio input cable between the Low Distortion Oscillator and the Left input of the PCM 81 and insert terminator plug.**
   As the PCM 81 automatically routes any audio signal present at either input to both Left and Right inputs, you must insert a terminator plug into the unused input jack to activate only one input channel.

6. **Select balanced or unbalanced input switch.**
   Set the PCM 81 rear panel switch out for input requiring 0dB gain. Push the switch in to test unbalanced input requiring +20dB gain.

7. **Connect the audio output cable between the PCM 81 Left Output and the Distortion Analyzer.**

8. **Insert an audio terminator plug into the PCM 81 Right Output jack.**

Check Signal Levels

1. Apply a 1 kHz sinewave signal to the left input at +20dBu=7.75Vrms for balanced (0dBu=0.775Vrms for unbalanced).

2. Measure the Left output level:
   - Connect the Oscilloscope to the Monitor jack of the Distortion Analyzer.
   - Set the Analyzer to voltmeter mode
   - Turn the PCM 81 front panel Input Level knob up full (completely clockwise). The signal on the oscilloscope will be clipping.
   - Slowly turn the Input Level knob counterclockwise until the signal is just below clipping. Note this setting as you will be reminded to return to it in the following tests.

3. Switch the Distortion Analyzer back to level and read the Left output measurement. Acceptable levels are between +18.5 and +21.5dBu.

4. On the PCM 81, press **Control** then turn SELECT to display **Output Level**. Turn ADJUST to display **-10dBu**.

5. Measure the Left output again on the Distortion Analyzer. The reading should be between 7.5 and 4.5dBu .

6. Swap the I/O and terminator connectors, reset the PCM 81 **Audio Output Level** to **+4dBu** , and repeat steps 2-5 for the right output .

Frequency Response Measurement

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 81. Turn the PCM 81 front panel Input Level to the position established as being just under clipping .

2. Measure the right output and set the Analyzer for 0dBu reference.

3. Turn off all filters on the Analyzer.

4. Sweep the Oscillator from 10Hz to 20kHz.

5. The right output should vary less than $\pm$0.5dB, referenced to the 1kHz output level.

6. Swap the I/O and terminator connectors and repeat steps 1-5 for the left output.

THD+N Measurement

1. Apply a 1kHz +20dBu sinewave signal to the left input of the PCM 81. On the Analyzer the only filter used should be in the range of 20Hz to 20kHz of audio bandpass, or 30kHz low pass filters can be used.Turn the PCM 81 front panel Input Level to the position established as being just before clipping .

2. Set the PCM 81 **Audio Output Level** to **+4dBu**.

3. Measure the Left output THD+Noise level on the Analyzer, for a reading of <0.008 %

4. Swap the I/O and terminator connectors on both inputs and outputs and measure THD+Noise level for the right output <0.008 %

Signal To Noise Ratio

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 81. Turn the PCM 81 front panel Input Level to the position established as being just before clipping .

2. Set Analyzer to dB Ratio and zero it for a reference level. Turn off the oscillator output and measure the right output. The reading should be greater than a 90dB ratio.

3. Swap the I/O and terminator connectors and repeat on the left output.

Digital I/O Test

The following two tests confirm the PCM 81 S/PDIF and AES/EBU digital input and output ports.

S/PDIF Test

The S/PDIF circuit is verified with an on-board wraparound test in the Extended Diagnostics.

1. Connect an RCA cable between the PCM 81 S/PDIF IN jack and the S/PDIF OUT jack.
2. Press and hold the front panel **Control** and **Tempo** buttons while powering up the PCM 81. Continue to hold down the buttons until the display reads:

   PCM 81 Diagnostics
   SELECT Test
3. Turn SELECT until the display reads: **Dig Aud IO Wrap Test**
4. Press **Load**. The lower half of the display should read: **WAIT! Executing Test**

If the test passes the display will read: **PASSED.** If it fails the display will read: **FAILURE.**

AES Test

The following test, which verifies the AES/EBU ports, requires a second PCM 81, or another device that can transmit and receive AES/EBU formatted signals.

1. Place the two devices one on top of the other. Connect power to each and power on.
2. Attach XLR cables between the AES/EBU inputs and outputs of both units.
3. On the PCM 81 you are testing, press **Control** and select

   Audio*Word Clock
   Analog: 44.1kHz

4. Turn ADJUST tol change the display to::

   Audio*Word Clock
   Ext:XLR Prf 44.1

   This verifies that the PCM 81 under test is receiving a 44.1kHz digital signal from the other device.
5. To test the 48kHz path, set the transmitting device to 48kHz. The PCM 81 display should read:

   Error:Lock
   (Press any button)

6. Press any button on the PCM 81 front panel to have the PCM 81 attempt to lock to the incoming signal. If lock is successful, the PCM 81 display should read:

   Audio*Word Clock
   0.0 Ext:XLR Prf 48

Footpedal Functionality

Before performing this test, press **Control**. Use **Up** and **Down** and SELECT to locate matrix position **1.0 Edit Mode**. Use ADJUST to set the mode to **Pro**.

1. Connect a footpedal to the PCM 81 rear panel Foot Controller connector.
2. Press **Program Banks** repeatedly to display Program Bank 2 (**P2**).
3. Turn ADJUST to select **4.0 Pedal Swell**.
4. Press **Load/*** to load the program.
5. Press **Edit**, then use **Up** and **Down** and SELECT to locate matrix position **0.2 InLvl L**.
6. Slowly depress the footpedal and verify that the parameter smoothly changes from **Off**, to **Full**.

Footswitch Functionality

1. Connect a dual footswitch with a 1/4" tip-ring-sleeve plug into the PCM 81 rear panel Foot Switch connector. These tests can also be done with a single footswitch with a mono 1/4" tip-sleeve plug inserted half-way in to test Foot Switch 1, then inserted completely to test Footswitch 2.
2. Press **Control**. Use **Up** and **Down** and SELECT to locate matrix position **1.3 * Bypass Mode**.
3. Press **Load/*** to display the parameter **Bypass Src**.
4. Use ADJUST to select **Foot Sw 1**.
5. Press the first footswitch. The Bypass light should toggle from off to on, or on to off.
6. Use ADJUST to select **Foot Sw 2**.
7. Press the second footswitch. The Bypass light should toggle from off to on, or from on to off.

After finishing this test, use ADJUST to select **Off** (and leave Bypass in its Off default state).

Listening/Q.C.

Required Equipment

- Clean, antistatic, well lighted work area
- Low Distortion sine wave oscillator
- Headphone Amplifier
- (4) 1/4" to 1/4" stereo phone plug cable (3 ft. minimum)
- Two 1/4" female to 1/4" male Y-adapter cables
- Stereo Headphones

Setup

1. Use two audio cables and a Y-adapter to connect the output of a low distortion sine wave oscillator to the left and right audio inputs of the PCM 81.
2. Use 2 cables to connect the headphone amp inputs to the PCM outputs.
3. Set the oscillator to 220Hz at –45dBV.
4. Turn the volume control on the headphone amplifier all the way to minimum (fully counterclockwise) and plug in the headphones.
5. Set the Input Level switch on the rear panel of the PCM 81 to the IN position (-20dB).
6. Power up the PCM 81. Press **Program Banks** repeatedly to select Program Bank 0 (**P0**).
7. Turn the SELECT knob clockwise to display:

   ConcertHallP0 1.9

   ***ADJUpMyEchos**
8. Press **Load/***. (Make sure **Bypass** is OFF.)

Verify Clean Audio

1. Put the headphones on.
2. Set the PCM 81 INPUT control fully clockwise.
3. Slowly increase the volume on the headphone amplifier until it's at a comfortable listening level.
4. Adjust INPUT over its entire range.
5. Verify that no pops, clicks or scratchiness are heard when turning the pot.
6. Adjust PCM 81 INPUT so the peak level just turns on the –6dB (yellow) headroom LED.
7. Adjust the volume on the headphone amplifier to a comfortable listening level.
8. Mute and unmute the signal source at different frequencies. Carefully listen to the outputs for grossly unusual noise, audible distortion or other gross audio irregularities through entire decay time of the reverb.

Shock Test

1. Lift each corner of PCM 81 four inches off of the workbench and drop.
2. Verify that no audio or display intermiitents are caused by this action.

KEEP ONE CORNER OF UNIT TOUCHING THE BENCH AT ALL TIMES TO PREVENT DAMAGE TO THE UNIT

MIDI Functionality

The following is a quick test of MIDI functionality. A more thorough test is included in the Extended Diagnostics (described in Chapter 4). The following test requires a second PCM 81. You may want to record the parameter values changed during the test so that they can be restored when the test is completed.

1. Power up both PCM 81s and load **P0 0.0 Prime Blue** on each unit. (Press **Programs Banks** repeatedly until **P0** is displayed. Turn SELECT to display **P0**, then press **Load/✱**.)
2. Connect a MIDI cable between MIDI OUT on the reference PCM 81 and MIDI IN on the PCM 81 under test.
3. On each unit:
   a. Press **Control** and use **Up** and **Down** and SELECT to locate matrix position **3.1 MIDI Receive**. Turn ADJUST to select **1**.
   b. Turn SELECT to locate matrix position **3.2 Transmit**. Turn ADJUST to select **1**.
   c. Turn SELECT to locate matrix position **3.4 Pgm Change**. If **MIDI Automation** is not displayed, press **Load/✱** until it appears. Turn ADJUST to select **On**.
   d. Press **Load/✱** to display **MIDI Target ID**. Turn ADJUST to select **All**.
   e. Turn SELECT to locate matrix postion **3.7 SysEx**. If **MIDI SysEx Receive** is not displayed, press **Load/✱** repeatedly until it appears. Turn ADJUST to select **On**.
   f. Press **Load/✱** to display **MIDI SysEx Device ID**. Turn ADJUST to select **0** (the default setting).
   g. Press **Edit** to enter the edit matrix. Use **Up** and **Down** and SELECT to locate matrix position **S.0 Controls Mix**.4.
4. On the reference PCM 81, use ADJUST to slowly increase the parameter from 0-100%. The **Controls Mix** parameter on the PCM 81 under test should track the reference PCM 81 as you turn ADJUST.

This completes testing of MIDI input to the unit under test. Swap the MIDI IN and OUT connections and repeat step 4 to test MIDI output.

MIDI THRU can be tested by verifying the transfer of MIDI data from any device's MIDI OUT to the PCM 81 MIDI THRU, then to any device's MIDI IN. Two MIDI devices with a PCM 81 connected between them, or three PCM 81s can be used for this.

4

Troubleshooting

Power On Diagnostics*

When the PCM 81 is powered up, the unit will go through a self-test to verify proper operation of its internal system, and digital signal processors. When proper operation is confirmed, the unit exits the self-test mode and will briefly display the following message:

Lexicon PCM 81
Version n.nn

This message is followed by information on the amount of audio memory installed in the unit, and the final message: **Loading effect...** while the last effect used is loaded to the digital signal processors.

Following is a list of the Power On Diagnostic Tests in the order in which they are executed. Each test is identified by a code number which is used to identify tests in the failure log.

Test	ID #
Host V40 CPU Test	01
ROM Checksum Test	02
Host (V40) SRAM Test	03
Display Test	04
Host (V40) Timer/Counter Test	05
Host (V40) Interrupt Mask Test	06
56k CPU and DRAM Test	07
Lexichip DRAM Test	08
Host (V40) DRAM Test	09
Battery Test	0AH
TACOchip Test	0BH

An additional test number (FFH), is used to indicate a problem in the link between the Host and the Z80 bus when the Z80 CPU tries to load code from the Slave RAM to the Lexichip.

The 56k DRAM, Lexichip DRAM test, and Host DRAM tests are executed simultaneously by the independent CPUs to shorten the total Power On Tests execution time.

When the unit is powered on, all of the front panel switch LEDs and all of the display pixels are turned on. The display pixels remain on for approximately two seconds, during which time the first three diagnostic tests are run.

Once the Display Test is complete, and while the rest of the tests are running, the message **Memory Tests** is displayed. If the operator presses the front panel **Compare** button, the displayed message will change to **Extended Memory Test** and additional memory tests will be performed. The Extended Memory Test will also be run automatically if the SRAM is cleared.

* PCM 81 software contains two types of diagnostics: Power On Diagnostics and Extended Diagnostics. This section describes the Power On Diagnostics which are executed automatically each time the PCM 81 is turned on, as well as the Extended Diagnostics.

Before each Diagnostic test is executed, the Test ID# is displayed on the headroom LEDs. This display remains while the test is running, and can be used to identify the failed test in the event that the unit hangs or crashes during the test. See Diagnostic Fa*ilures.*

When all the diagnostics have been executed, all of the headroom LEDs are turned on briefly while the unit is initializing, and **Lexicon PCM 81** appears on the display.

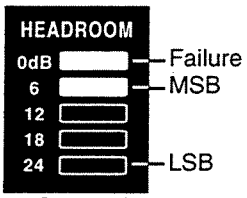
Diagnostic Failures

Errors which occur during the Power On Diagnostic Tests are available in an error log file. When a failure occurs during the test sequence, the red 0dB LED will light and a binary test/error code will be displayed on the LEDs. An **E** and the test ID# will also appear on the front panel display to indicate which test failed. Information about the failure will be stored in an error log file in the SRAM for future analysis. The LED code is a 4-bit binary number displayed on both headroom columns with the -24 dB LED as the LSB, and the yellow -6 dB as the MSB.

The figure below shows an example of the LED binary failure code indicating that the Lexichip Power On DRAM Test failed. In this case, the front panel display would additionally display E8. (Memory Card diagnostic test failures are not reported on the headroom LEDs.)

Failure of any test will stop the Power On Diagnostic Tests sequence. When a failure occurs, the operator has the following options:

1. Power cycle the unit and see if the Power On Diagnostics pass on restart.
2. If the failure occurred during the CPU, ROM and SRAM tests, press **Down** to enter a special diagnostic test loop in which 1's and 0's are walked through the Address and Data bus.



Binary Code 8 (1000)

3. If any test but the CPU test failed, press **Load** to execute the next test. Although you can step through all of the tests by continuing to press **Load** after each test, the unit will not become operational at the end of the sequence. (Once **Load** is pressed, you can enter a special error log viewing mode — See *Error Log and Failure Viewing Mode.*)
4. Power cycling the PCM 81, then pressing **Control** and **Tempo** simultaneously will initiate Functional Diagnostic Tests.

NOTE: If a failure occurs during the CPU test, the failure will not be stored in the error log. Failures that occur during the ROM and SRAM test will not be stored unless **Load** is pressed and the test cycle is allowed to progress beyond the SRAM test. Data may not be stored, or the unit may crash, depending on the seriousness of the problem.

Bypassing Diagnostic Failure Lockup

If problems arise during the power-on cycle, the unit will not boot into the main system. The message **Diagnostic Failure Occurred** will be displayed if Load is pressed when the failure occurs.

There are two options for bypassing system lockup: entering Extended Diagnostics, or simply bypassing the diagnostics and continuing the boot cycle. **Bypassing error messages with either method can result in excessive speaker excursion, and/or lost user register data.** Of the two options, entering Extended Diagnostics involves less risk of loss of user registers than does bypassing diagnostics altogether.

You can enter Extended Diagnostics by simultaneously pressing **Control** and **Tempo. The message: PCM 81 Diagnostics SELECT Test** will be displayed To enter the Error Log Failure Viewing Mode, turn the SELECT knob counterclockwise three times when this message appears.

To completely bypass a diagnostic failure, simultaneously press Up and Tempo when the failure occurs. The message: WARNING! Do not continue will be displayed. Simultaneously press **Down** and **Tap** to bypass the failure message and continue the boot sequence.

Error Log and Failure Viewing Mode

All failures that occur are stored in a 20 record ring buffer (First In First Out) called the Error Log File. Each record consists of 5 elements:

1. Test number, which indicates which test failed. For example, the number 09 means that the Host V40 DRAM Test failed. Test number 00 indicates no failure.
2. Tested value. As an example, in the case of a Host DRAM Test failure, this data could be 000000AA — a pattern written by the CPU to the DRAM. A value of 00000000 may indicate that the CPU tried writing all zeros to the DRAM or it could mean that this value is not applicable for the type of failure that occurred (such as timeout failure).
3. Failed value. As an example, in the case of a Host DRAM Test failure this data could be 0000002A, indicating a problem with bit 7 on the Host Data Bus, or perhaps a cold solder connection on the DRAM. A value of 00000000 may indicate that this value is not applicable for the type of failure that occurred (such as timeout failure).
4. Address/location where failure occurred. In case of the Host DRAM Test failure, the address could be 00000000 which is where the DRAM is located. (00000000 could also mean that this value is not applicable for the type of failure that occurred.)
5. Type of failure. This value indicates which type of failure occurred. For example, in the Host DRAM Test, 01 indicates data failure.

Simultaneously press **Control** and **Tempo** to enter Failure Viewing mode, where as many as 20 failure codes are listed (most recent first). A single failure record is shown below:

XXXXXXXX YYYYYYYY
AAAAAAAA TT

Use **Up** or **Down** to display all of the failures. Press **Load** to exit.

Remember that the unit suspends operation when CPU failures occur, and CPU failures are, therefore, never stored. ROM and SRAM failure information is not stored unless the SRAM test has been completed and Load has been pressed in repsonse to the ROM and/or SRAM failure message.

#	=	Test number (00 indicates cleared error record)
X	=	Tested value (e.g. data written to RAM)
Y	=	Failed value (e.g. data read back from RAM)
A	=	Address where failure occurred
T	=	Describes failure type:

Error Log Failure Codes

Display	Hex	Description
0	00H	Unknown / No failure
1	01H	Data failure (Indicates that failure happened, for example during RAM Data test)
2	02H	Address failure (Indicates that failure happened during RAM Address test)
3	03H	Timeout failure (Occurs if there is no response from the co-processor or if a test is taking too long.)
4	04H	No RAM size information available
5	05H	Wrong RAM size
6	06H	Data transfer failure
8	08H	CPU failure
9	09H	Slave Z80 loading the Lexichip WCS failed
10	0AH	Data transfer to Slave Z80 SRAM failure
12	0CH	MIDI Test timeout failure, Transmit buffer didn't get emptied*
13	0DH	MIDI Test timeout failure, Receive buffer didn't get filled*
14	0EH	MIDI Test data transfer error detected by the Serial Control Unit*
15	0FH	MIDI Test transmitted data vs. received data mismatch*
16	10H	MIDI Test Transmit interrupt failed*
17	11H	MIDI Test Receive interrupt failed*
18	12H	PCMCIA Card Test, No card installed*
19	13H	PCMCIA Card Test, Write Protect is on*
20	14H	PCMCIA Card Test, Backup battery voltage is too low*
21	15H	PCMCIA Card Test, Bank switching failed*
22	16H	PCMCIA Card Test, Attribute register failed*
23	17H	PCMCIA Card Test, Transferring code from card to DRAM failed*
24	18H	Foot controller ADC test failed (Requires special test fixture)*
25	19H	Watchdog Timer Test failed, timed-out too soon*

26	1AH	Watchdog Timer Test failed, failed to time-out*
28	1CH	Stack failure during Watchdog Timer test (Software related)
29	1DH	The Z80 did not initialize the mailbox and has ikely crashed*
30	1EH	48 kHz Word Clock frequency is too high*
31	1FH	48 kHz Word Clock frequency is too low*
32	20H	44.1 kHz Word Clock frequency is too high*
33	21H	44.1 kHz Word Clock frequency is too low*
39	27H	The Digital Audio Receiver is locking to a data stream that shouldn't be there
40	28H	The Digital Audio Receiver is detecting a word clock frequency outside the 48kHz +/- 400 PPM tolerance. Note: The receivers reference clock is the 48kHz crystal oscillator for the transmitter chip
41	29H	The Digital Audio Receiver is detecting a word clock frequency outside the 44.1kHz +/- 400 PPM tolerance. Note:The receivers reference clock is the 48kHz crystal oscillator for the transmitter chip
42	2AH	The Digital Audio Receiver is detecting Professional Audio coming in instead of Consumer
432	40H	The Digital Audio Receiver detected an error by setting the ERF signal high
44	41H	The Digital Audio Receiver detected a Validity error
45	42H	The Digital Audio Receiver detected a Confidence error
46	43H	The Digital Audio Receiver detected a Slip Sample error
47	44H	N/A (The Digital Audio Receiver detected a CRC error)
48	45H	The Digital Audio Receiver detected a Parity Error
49	46H	The Digital Audio Receiver detected a Bi-Phase Error
50	47H	The Digital Audio Receiver detected a No Lock Error

* Tests residing in the Extended Diagnostics. Note that the failure codes are different for the Host (V40) Timer/Counter Test.

Failure indications marked with an * are created by tests residing in the Diagnostic card. Note that the failure codes are different for the Host (V40) Timer/Counter Test.

Power On Diagnostics Active Buttons

During the Power On test sequence, the front panel buttons will be scanned. The buttons must be pressed when power is turned on, until all the front panel display pixels are turned off.

Push Button Combination:	Action Taken
Up and **Bypass**:	Bypasses some of the diagnostics and speeds up the boot cycle.
Compare	Initiates extensive 56k-, Lexichip- and Host DRAM test. (This test can take up to 2 minutes depending on the size of the installed DRAM). If the 56k DRAM size is changed, the change will be detected and the 56k extensive test will be initiated automatically at the time the unit is first turned on. The message: **Extended DRAM test** is displayed during the test.
Up and **Control**	The unit will loop the Power On Diagnostics until the unit is powered off.
Control and **Tempo**	Will activate the Extended Diagnostics. Turn the SELECT knob counterclockwise three times to access the error log. Press **Load**, then **Up** or **Down** to scroll through the failure records. Upon entry into this mode, the most recent failure is displayed. Press **Load** to exit. Pressing these buttons when ROM- or SRAM test failure occurs will activate the card diagnostics if the diagnostic card is installed. WARNING! Depending on the seriousness of the failure, data stored in the registers could be lost if the operator decides to ignore the failure message and continue. In order for the card diagnostics to work, certain parts of the system have to be working. (V40-CPU, ROM, SRAM, Host DRAM, and card interface.) These buttons can also be pressed when the Diagnostic Failure **Occurred** message is displayed to enter the Diagnostics.
Up and **Tempo**	Can be pressed when the **Diagnostic Failure Occurred** message is displayed and the operator wishes to ignore the error message. For more detail, see above description. WARNING! Bypassing this error message is not recommended. If the operator wishes to enter the diagnostics or look at the failure log, **Control** and **Tempo** can be pressed (see button sequence description above).
Load	If diagnostic failure occurs and **Load** is pressed, the failure is ignored and the boot cycle will continue.
Down	This button is only active when the V40-CPU, ROM- and/or SRAM tests fail. Pressing it will activate a special test that keeps the Host Data and Address bus active.

Down and **Tap** Initialize PCM 81 to factory settings.

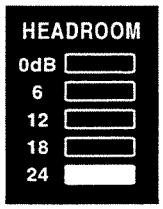
WARNING! This action erases the user setup and the diagnostic failure log by clearing the memory (SRAM). The message: **WARNING! Press STORE to clear the SRAM** is displayed. The memory is cleared by pressing **Store**. The message: **SRAM Cleared press any button to cont.** is displayed. Press any button and the unit reboots. If any button other than **Store** is pressed, **SRAM clear cancelled** is briefly displayed and the boot cycle will continue without clearing the memory.

Power On Diagnostics Test Descriptions

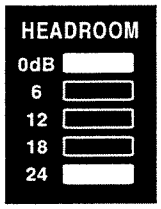
Host V40 CPU Test (1)

This test verifies any stuck CPU register bits. The V40 Host processor (U34) tries to pass the value 55AAH through its internal registers. In second pass, the data is inverted to AA55H and passed through the registers. If an error is detected, an attempt is made to write an error code to the front panel headroom LEDs and the boot cycle will be halted.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Host V40 CPU Test



Host V40 CPU Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code.

If a CPU error occurs, the operator has the option of pressing **Down** to enter the test loop. Besides reading data from the ROM, the V40 writes a walking "1" value to location "0000H" in the SRAM. (Mapped to B0000H.) By using an oscilloscope and triggering on the HMWR/ pulse, you can verify that all the data lines are connected to all the devices and that there are no shorts. If there is a problem with the data bus and/or the address bus between the V40 CPU and the ROM, the unit will not boot at all. An additional walking "1" test on the address bus is performed by rotating a "1" through the 20-bit address bus by reading data from the entire address space If the CPU registers used by this test are broken, the test will not work as intended.

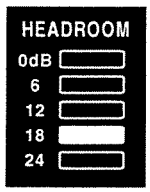
A CPU error is a serious problem. The program will not be able to proceed from here to the diagnostic system and may not even reach the test loop. The only way to exit the test loop is by power cycling the unit.

No failure log is generated.

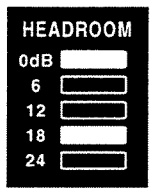
ROM Checksum Test (2)

The ROM checksum, which is a byte size value, is located as the last byte in the ROM (U55). The test adds up the entire ROM including the Checksum byte. The result should be zero (8 bit value.)

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



ROM Checksum Test



ROM Checksum Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code, and an attempt is made to write E2 to the front panel display.

If a ROM checksum error occurs, you can press **Load**, simultaneously press **Control** and **Tempo**, or to press **Down**. If **Load** is pressed, the failure is ignored and the next test will be executed. The failure will not be stored until just before the Display Test is executed.

Pressing **Control** and **Tempo** invokes the Extended Diagnostics.

Note: There is a risk in doing this if there is a ROM problem, as the diagnostic system may not function and the user registers may be destroyed.

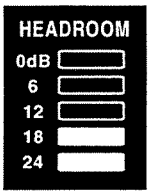
Pressing **Down** causes the CPU to start executing the same test loop as described in the CPU test. The unit has to be power cycled to exit the test loop.

Failure log

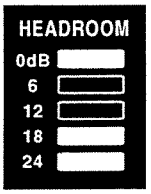
Test number	: 2
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: N/A

Host (V40) SRAM Test (3)
This SRAM test does not touch the volatile SRAM area (where register and other system information is stored). It does nondestructive testing in the first 4k of the SRAM (U54). The nondestructive test reads one location and stores it in a CPU register. Then, it performs a marching "1" test on that location followed by a marching "0" test on the same location. The test location is incremented by one until the end of the diagnostic SRAM area is reached. Since the SRAM is used as a temporary stack until the DRAM has been tested, a destructive counting test is done on the area where the temporary stack is located (approx. the first 200H bytes). This will ensure address independence in the temporary stack area.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Host V40 SRAM Test



Host V40 SRAM Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and an attempt is made to write E3 to the front panel display.

If a Host SRAM failure occurs, you can press **Load**, simultaneously press **Control** and **Tempo** or press **Down**.

If **Load** is pressed the failure is ignored and the next test will be executed. The failure will not be stored until just before the Display Test is executed.

Pressing **Control** and **Tempo** invokes the Extended Diagnostics.

Note: There is a risk in doing so if there is a SRAM problem. The program stack may not be (and probably will not be) operational. Therefore, the program is likely to crash and destroy all the user register setups. The diagnostic system may not function.

Pressing **Down** will cause the CPU to start executing the same test loop as described in the CPU test. The unit has to be power cycled to exit the test loop.

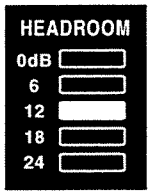
Failure log

Test number	: 3
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: address or data

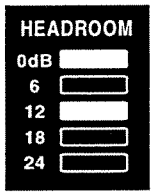
Display Test (4)

This test checks the display busy bit (U33 pin 9) by writing a "reset" display command to the display. The test verifies if the display busy signal is activated and then deactivated again. If not, a failure is reported. Maximum busy time is specified as 45µs.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Display Test



Display Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and an attempt is made to write E4 to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. pressing **Load** will execute the next test.

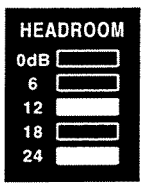
Failure log

Test number	: 4
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: N/A

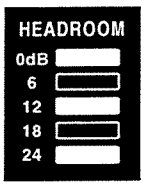
Host (V40) Timer/Counter Test (5)

The timer/counter test checks the 3 V40 (U34) internal counters. The test verifies that the status registers and the count registers don't have any stuck bits.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Host Timer/Counter Test



Host Timer/Counter Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E5 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.

NOTE: The failure codes do not apply to this test.

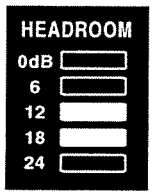
Failure log

Test number	: 5
Tested value	: N/A
Failed value	: N/A
Address/location	: N/A
Type of failure	: Bit 0 = Timer 0 Status test failed if 1 Bit 1 = Timer 1 Status test failed if 1 Bit 2 = Timer 2 Status test failed if 1 Bit 4 = Timer 0 Counter test failed if 1 Bit 5 = Timer 1 Counter test failed if 1 Bit 6 = Timer 2 Counter test failed if 1

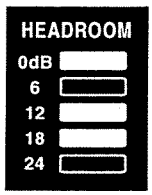
Host (V40) Interrupt Mask Test (6)

This test is limited to the internal V40 (U34) interrupt controller mask register. The register will be tested by a marching "1" and a marching "0" test.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Host V40 Interrupt Mask Test



Host V40 Interrupt Mask Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E6 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.

Failure log

Test number	: 6
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: N/A
Type of failure	: N/A

56k CPU and DRAM Test (7)

This test is executed by the 56k and consists of the 56k (U15 DSP) doing a CPU test and a DRAM test. The 56k does not have enough code space to be able to do both the CPU and DRAM test in the same sequence. The Host V40 (U34) therefore loads and executes the CPU and the DRAM tests separately. The CPU test is executed first. A DRAM sizing test is a part of the DRAM test.

When the 56k finishes the test, it will send a done message to the Host. If it found an error, it will send an error message. If the Host gets the error message, it will log the error and report it to the display. The Host is also running a timer to keep track of the execution time and report error if the test is not completed in time.

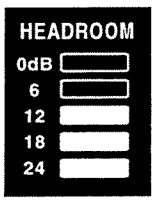
As this test can take quite some time, the Host doesn't wait for the test results. The Host goes and boots the Lexichip DRAM test and completes the Host V40 DRAM test before getting the test results from the 56k.

There are two versions of the 56k DRAM test. The first version tests only the standard 256k of memory, not the 56k Data Window Address Register. This is done to shorten the test time and therefore shorten the boot cycle time. The other version tests all of the installed DRAM (1M). This extended version also tests the 56k Data Window Address Register, accessing all of the memory.

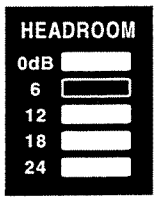
The extended version is invoked when:

- **Compare is pressed during power-on.**
- 56k DRAM size has been changed. DRAM size changes are automatically detected when the unit is turned on.
- SRAM has been cleared.

Before the test is executed, the following binary code will be put out on theHeadroom LEDs:



CPU and DRAM Test



CPU and DRAM Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E7 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing Load will execute the next test. If the 56k- CPU or DRAM test fail, the TACOchip test will not be executed.

Failure log

Test number	: 7
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

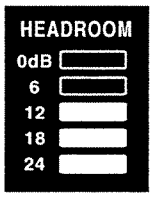
Lexichip DRAM Test (8)

Like the 56k DRAM Test, the Lexichip DRAM (U16, U17 DSP) Test is not controlled by the Host V40. The Hosts role is to load a test code to the Slave Z80 SRAM (U35 DSP) and to communicate with the Z80 (U36 DSP) regarding test results. The Host V40 CPU ensures that the 56k Phase Locked Loop (PLL) is running before loading code to the Z80 SRAM (The 56k has to be able to run the 56k DRAM code for the PLL to work). The Host -Z80 interface will not work properly unless the 56k PLL is working. The Z80 controls the Lexichip (U18 DSP) which actually performs the DRAM test. When the Z80 and the Lexichip finish the test, the Z80 will send a done message to the Host. If it found an error it will send an error message. If the Host gets the error message it will log the error and report it to the display. The Host is also running a timer to keep track of the execution time and report error if the test is not completed in time.

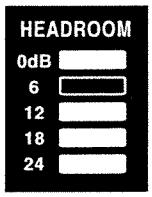
As this test can take quite some time, the Host doesn't wait for the test results. The Host goes and completes the Host V40 DRAM test and the 56k DRAM test before getting the test results from the Z80.

The Host V40 can instruct the Z80 to initiate two different versions of the Lexichip DRAM test. A simpler version, which shortens boot time is usually executed. A longer version is executed when the Compare button is pressed during power-on, or when the SRAM is cleared.

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



DRAM Test



DRAM Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E8 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing Load will execute the next test. If the Lexichip DRAM test fails the TACOchip test will not be executed.

Failure log

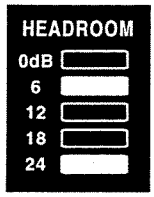
Test number	: 8
Tested value	: Expected written data
Failed value	Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

Host (V40) DRAM test (9)

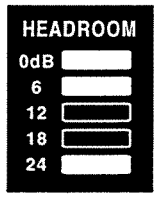
The Host DRAM test is executed by the V40 CPU while it is waiting for the other CPUs to complete their respective DRAM tests. As with other DRAM tests, there are two versions, one executed under normal conditions, the other initiated by:

- pressing Compare during power-on
- clearing SRAM

Before the test is executed, the following binary code will be put out on the Headroom LEDs:



Host V40 DRAM Test



Host V40 DRAM Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E9 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test. If the Host DRAM test fails, execution of Card Diagnostics is not recommended, as the DRAM is used by the Diagnostics. Execution may result in speaker damage and/or lost user registers.

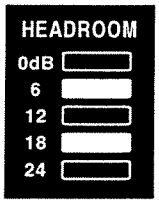
Failure log

Test number	: 9
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: Address of first bad location
Type of failure	: Various

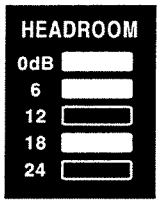
Battery test (0AH)

The Host CPU reads the battery low indicator and passes low/good battery information to the main operating system. The boot cycle is not discontinued if there is a low battery condition. When the battery voltage is close to the trigger level of the comparator, the comparator could start oscillating.

Before the test is executed, a binary code will be put out on the Headroom LEDs. The code is:



Battery Test



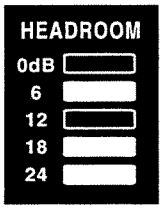
Battery Test Failure

No failure log is generated, but a warning message will be displayed.

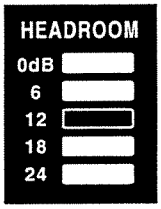
TACOchip Test (0BH)

The TACOchip test utilizes all CPUs. The 56k processor (U15 DSP) is in charge and sends data through the various slots of the TACOchip (U10 DSP). The Lexichip receives data, stores it in its DRAM, reads it back, and transfers it to the various slots in the TACOchip. Then the 56k fetches the data from the TACOchip and makes sure that data received matches data sent. When the 56k finishes the test, it will send a done message to the Host. If it found an error, it will send an error message. The Host logs the error and reports it to the display. The Host also runs a timer to track execution time, and reports an error if the test is not completed in time. The Z80's duty in this test is to transfer the Lexichip code that the Host V40 loads into the Slave Z80 SRAM (U35 DSP)to the Lexichip. The Z80 (U36 DSP) takes no part in determining failures. This test will not be executed if either the 56k or the Lexichip DRAM test fails.

Before the test is executed, a binary code will be put out on the Headroom LEDs. The code is:



TACOchip Test



TACOchip Test Failure

If failure occurs, the 0dB (red) LED is turned on in addition to the binary code and E11 is written to the front panel display. The unit will terminate the boot cycle and wait for the operator input. The error information is stored in the failure log automatically when failure occurs. Pressing **Load** will execute the next test.

Failure log

Test number	: 0BH
Tested value	: Expected written data
Failed value	: Actual read back value
Address/location	: TACOchip Address of first bad location
Type of failure	: Various

Extended Diagnostics Test Descriptions (Functional Tests)

To access the Extended Diagnostics Tests and Troubleshooting Tools, press and hold the PCM 81 front panel **Control** and **Tempo** buttons while powering on the PCM 81. Continue to hold these two buttons until the PCM 81 display reads:

PCM 81 Diagnostics
SELECT Test

Release the buttons once this display appears.

To run a test or tool, turn the SELECT knob on the PCM 81 until the desired test is on the display and then press the **Load** button to enter the test. The following tests and tools are available:

Encoder Test
Switch Test
LED Test
Display Char Test
Display Block Test
PCMCIA Card Test (#0DH)
Auto Test Execution
Foot Cntrl. ADC Test (#0EH)
MIDI Test # (0CH)
DMA Data Transfer Test (#11H)
Watchdog Timer Test (#0FH)
Word Clock Select Tst (#10H)
Digital Audio Wrap Test (#13H)
Digital Audio I/O Through
Infinite Test Loop
Show Error Log
Clear Error Log

The following tests require technician interaction and judgment. As these tests do not generate any error messages that are stored in the Error Log File, no test numbers are assigned to them.

Encoder Test (using the ADJUST and SELECT knobs)
Switch Test
LED Test
Display Char Test
Display Block Test

Encoder Test

This test verifies the operation of the encoders (2), including correct sequence and ID. The test displays the encoder name (ADJUST or SELECT) and the bit pattern status of the encoder. It also displays an accumulative value and increments or decrements depending on the rotational direction. Press **Load** to exit the test.

Switch Test

This test verifies the operation of the front panel buttons (12), footswitches (2) and audio output jacks (2). Two 1/4" phone plugs should be connected to the audio output jacks during this test. Otherwise, the bottom half of the display will read **Single Aud Out Jack** when no switches are being tested. When a button or a footswitch is being pressed, the bottom half of the display will read **Pressed** next to the button name. When the button is released, the display will read **Press Any Button**. The same approach is used for the Footswitches. When one or both of the 1/4" phone plugs are removed from the audio output jacks, the bottom half of the display will read **Single Aud Out Jack** to verify that the mono audio output feature is working. To exit the test, press and hold **Load** for five seconds, or until the display blanks.

LED Test

This test verifies that all LEDs (D101-122) are working. When the test is first executed, all the headroom and button LEDs are lit. Turning ADJUST clockwise, or pressing ▲, causes individual LEDs to light sequentially, with **Bypass** being the last in the sequence. Turning ADJUST one more position clockwise will cause all of the LEDs to light again. (Turning ADJUST counterclockwise or pressing ▼, will reverse the sequence.)

Display Char Test

This test lets you easily identify display problems and control the activity on the driver lines for easier troubleshooting. The test displays a single character on each of the 40 display positions. The character displayed can be changed by turning ADJUST, or by pressing ▲ or ▼. All of the letters in the alphabet and some additional ASCII characters are available.

Display Block Test

This is another tool for checking and troubleshooting the display. When used in conjunction with the character test, most display problems can be easily identified and debugged. This test turns on all the pixels of a single display character with all of the other characters off. When ADJUST is turned, or the ▲ or ▼ buttons are pressed, the lit character increments or decrements, effectively walking the block. When the position jumps from the last position to the first or vice-versa, the display is filled with a block character.

PCMCIA Card Test (#0D)

This test, which checks the Memory Card Socket, requires a 1 Meg card with Attribute Register. The memory card is installed in the UUT, data is written to the memory card, then read back from the card. If the data received matches the data sent, the display will indicate that the test passed. If the data does not match, the display will indicate that the test failed. Note that this test verifies that all the Data lines (D0-D7), Address lines (A0-A15, CA16-CA19) and control lines work as intended. It does not verify the card itself. If there are problems with any of the control lines, the display will indicate which test has failed and the test will halt until the problem has been repaired. The test can be aborted by pressing **Load**.

A PCMCIA Memory Card Fixture enables troubleshooting of control line failures. When the procedure prompts the technician to install the Test Card, the fixture is installed in the PCM 81 card slot with the Test Card installed in the fixture's card slot. Prior to installing the fixture in the card slot, the five toggle switches on the fixture must be set "ON". (These toggle switches are wired to the above **Control** lines so that the logic state of each line can be changed to verify that they're not stuck permanently in a high or low state.) The following is a procedure for individual testing of the control lines:

1. Press **Load**. The bottom half of the display will read **No PCMCIA Card Inst.**
2. Set the CD1 switch to its "down" position. The display should not change.
3. Set the CD2 switch to its "down" position. The display should change to read **Write Protect is On.**
4. Set the WP switch to its "down" position. The display should change to read **BVDT1 Lo and BVDT2 Lo.**

5. Set the B1 switch to its "down" position. The display should change to read **BVDT2 Lo**.
6. Set the BVD2 switch to its "down" position. The display should change to read

PCMCIA Card Test
Passed

7. Remove the Memory Test Card and the Memory Card Test Fixture from the Memory Card Slot.

Error report

Test number:	(0DH)
Expected data	8 bits
Actual read data	8 bits
Address location	20 bits, shows where failure occurred (if applicable)
Type of failure	(data, address, **Control** signals)

Auto Test Execution

This test was created to reduce test time in manufacturing. In order to run this test without causing false errors, the following test cables and fixture must be connected to the PCM 81.

1. Connect a standard MIDI Cable between PCM 81 MIDI Out and MIDI In.
2. Connect the Foot Controller Test Fixture (Lexicon part #770-08508) to the PCM 81 Foot Controller Input Jack.
3. Connect a digital I/O cable between PCM 81 S/PDIF In and S/PDIF Out.

The following tests are performed:

Foot Cntrl. ADC Test (0EH)
MIDI Test (#0CH)
DMA Data Transfer Test (#11H)
Watchdog Timer Test (0FH)
Word Clock Select Tst (#10H)
Digital Audio IO Wrap Test (#13H)

If a failure occurs, the Auto Execution Test will halt on the test that failed, display the name of the test on the top half of the display and **FAILURE** on the bottom half of the display. Press **Load** to continue the Auto Test Execution. (Note the **FAILURE** message remain on the bottom half of the display while the remaining tests are being executed.

Foot Cntrl. ADC Test (#0EH)

This test is performed with the Foot controller Test Fixture to check out part of the ADC804 (U23). The test checks out only the Foot Pedal controller Input to the chip and must be run with the test fixture or comparable circuitry. Testing the controller Input and the ADC chip with foot pedal can be accomplished using the ADC Monitor test. The ADC test will check the Foot Pedal controller Input by using the Foot controller Test Fixture which contains an LFO to sweep the controller input from it's minimum value (0VDC) to it's maximum voltage (+5VDC) then back to it's minimum. The ADC Test will analyze the data generated by the ADC chip during the sweep and confirms that the chip accurately reports the voltage to the Processor. When the sweep from min to max to min has been completed successfully, the test will display **PASSED**.

Error report

Test number	(0EH)
Expected data	N/A
Actual read data	N/A
Type of failure	(ADC Test Failed 03H, 18H)

Foot Controller Test Fixture

Lexicon uses a specially-designed test fixture for testing foot controllers. Following is a description of this fixture as well as a parts list and a reference drawing, in the event you want to build a similar fixture for your own use.

The Foot Controller Test Fixture provides an automatic 0 to +5V sweep for testing Lexicon products equipped with foot controller inputs. The fixture minimizes operator error when testing the controller inputs while still providing a thorough test.

The fixture provides a triangle waveform to the Controller Inputs with a low frequency sweep rate of approximately .5Hz. When monitored by the Foot Controller, A/D Converter Test (OEH), the display will sweep from 00 to FF in hex with a short pause at each extreme.

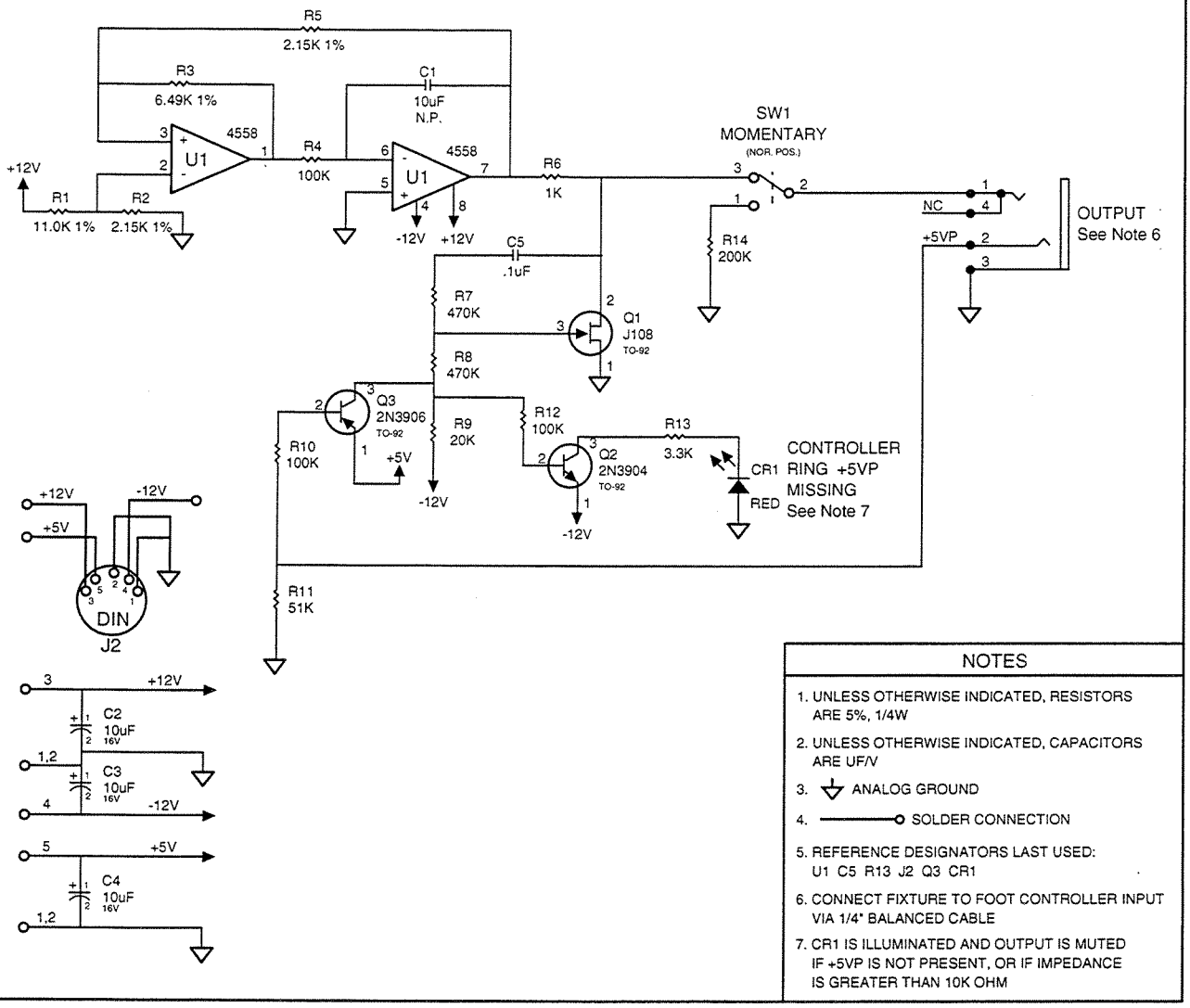
The fixture also contains a circuit for detecting the presence of +5V at the ring of the controller input beingtested. If the voltage at the ring is below 4V, the fixture output is muted and its LED will light.

Theory Of Operation

The fixture is powered by an external ELPAK WM063, or equivalent, power supply module which provides ±12V at 180mA each and +5V at 380mA. Power is fed into the fixture via a 5-pin DIN connector. The first half of U1 (a 4558 op amp) is configured as a low-frequency oscillator with R4 setting the rate. The output of U1 is routed through a 1kΩ resistor to SW1 which normally connects to the output of the fixture. When SW1 is pressed, the output of the fixture is connected to R14 (200K) which forms a resistive ladder with the internal pullup resistor.

When the fixture is connected to the PCM 81, +5V will be fed from the ring of the controller input being tested to the ring on connector J1 of the fixture. This voltage is sent to the base of transistor Q3 through resistor R10. R10 combined with R11 enables the voltage and/or impedance of the +5V line to turn the transistor on or off. If voltage drops below 4V, Q3 turns on. This biases both Q1 and Q2 on, lighting the LED and muting the fixture output. This verifies that +5V is present at the ring of the controller input and also checks the value of the resistor feeding the ring of the controller input.

Foot Controller Test Fixture



NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
3. ANALOG GROUND
4. SOLDER CONNECTION
5. REFERENCE DESIGNATORS LAST USED: U1 C5 R13 J2 Q3 CR1
6. CONNECT FIXTURE TO FOOT CONTROLLER INPUT VIA 1/4" BALANCED CABLE
7. CR1 IS ILLUMINATED AND OUTPUT IS MUTED IF +5VP IS NOT PRESENT, OR IF IMPEDANCE IS GREATER THAN 10K OHM

Foot Controller Fixture Parts List

PART NO.	DESCRIPTION	QTY	REFERENCE
340-00740	IC,LINEAR,4558	2	U1
520-00941	IC SCKT,8 PIN,PC,LO-PRO	2	U1
202-00529	RES,CF,5%,1/4W,1K OHM	1	R6
202-00538	RES,CF,5%,1/4W,3.3K OHM	1	R13
202-00555	RES,CF,5%,1/4W,20K OHM	1	R9
202-00564	RES,CF,5%,1/4W,51K OHM	2	R11
202-00570	RES,CF,5%,1/4W,100K OHM	2	R4,10,12
202-00576	RES,CF,5%,1/4W,200K OHM	2	R14
202-00579	RES,CF,5%,1/4W,470K OHM	3	R7,8
203-00460	RES,MF,1%,1/8W,2.15K OHM	1	R2,5
203-00465	RES,MF,1%,1/8W,6.49K OHM	3	R3
203-00474	RES,MF,1%,1/8W,11.0K OHM	1	R1
240-00609	CAP,ELEC,10uF,16V,RAD	4	C2,3,4

MIDI Test (#0CH)

To run this test, a MIDI cable must be connected between the MIDI IN jack and the MIDI OUT jack. The test verifies functionality of the MIDI input and MIDI output circuit by transmitting data to the MIDI OUT jack and attempting to read it back through the MIDI IN jack. The first stage of the test sends data through the Transmitter and then polls the receiver until data sent is received. This is repeated several times. The correctness of the data is also verified. The second stage of the test verifies that the MIDI interrupt (internal to the V40) is working satisfactorily.

NOTE: Each stage is repeated 255 times and the data transmitted error value is the actual counter value. Thus, it is possible to determine from the failure log how many bytes were transmitted successfully before failure occurred.

Error report

Test number	(0CH)
Transmitted Value	8 bit data sent out
Received Value	8 least significant bits data received
	(8 most significant bits indicate the status of the SCU status register)
Address	N/A
Type of failure	Transmit, receive, interrupt, data, timeout

DMA Data Transfer Test (#11H)

This test is verifies the Direct Memory Access (DMA) data transfer from the Host V40 memory to the 56K DSP. Both the V40 (U34) and the 56k (U13 on DSP Board) CPUs have a built-in DMA controller. The test verifies DMA controller functionality and a DMA handshake between the processors. The test uses Interrupt 3 to acknowledge completion of the DMA data transfer. A block of data from the Host ROM is transferred to the 56k internal, 24-bit wide Y memory. The same block of data is then transferred back from the 56k memory to the Host DRAM. The block of data in the DRAM is then compared to the original block of data in the Host ROM. The signals used in the handshaking are HACK/, HREQQ and HTC.

Watchdog Timer Test (#0FH)

The Watchdog Timer Test verifies that the Watchdog Timer is operational by first kicking the Watchdog approx. every 50ms for a period of approximately two seconds. During this time period the Watchdog should not reset the unit. (If it does, the test fails.) The second stage of the test lets the Watchdog Timer time-out and reset the unit. (If it does not reset the unit, the test fails.) Due to the structure of the Power On Diagnostics (the "boot code") the "Power On" CPU, ROM and SRAM Tests will be executed after the reset has taken place, before completing the Watchdog Timer test.

In the unlikely event the CPU, ROM and/or SRAM Tests fail, the Watchdog test will be aborted and the unit will go through regular cold boot cycle and report and log that error.

Error report

Test number	(0F)
Type of failure	(19H, 1AH)

Word Clk Select Test (#10H)

The Word Clock Test confirms that the internal 48kHz and 44.1kHz word clocks are operational and within a reasonable preset frequency limit. It utilizes the V40 built-in timer. The accuracy of the test is therefore also dependent on the accuracy of the Host V40 oscillator. The test is set to detect failures that are not within +/- 0.5% tolerance (47760Hz - 48240Hz for 48kHz clock in order for the test to pass, 44321Hz - 44830Hz in order for the 44.1kHz test to pass.) If 1 or both of the word clocks are not present, the system will lock up. This test starts the 56K and Z80 slave processors and leaves them running after the test is completed. In other words, the processors are not reset after the Word Clock Test is completed. The following error messages are available and will be displayed in the Error Log File if the Word Clock frequencies are out of spec:

44.1kHz WC Freq. too high
10 00000000 00000000
00000000 20

44.1kHz WC Freq. too low
10 00000000 00000000
00000000 21

48kHz WC Freq. too high
10 00000000 00000000
00000000 1E

48kHz WC Freq. too low
10 00000000 00000000
00000000 1F

Error report

Test number	(0FH)
Expected data	N/A
Actual read data	N/A
Type of failure	(Word Clock Freq. too high or too low)

Digital Audio I/O Wrap Test (#13H)

In this test the 56k processor generates a digital audio sinewave at 187.5Hz. The test verifies that this signal is wrapped from the S/PDIF output to the S/PDIF input. (There is no test for the AES input and output.) The V40 (U34) Host processor then reads the status of the digital audio receiver to determine whether it is receiving the data correctly.

To run this test, connect an RCA cable with a braided shield between the PCM 81 S/PDIF In and S/PDIF Out jacks. Press **Load** to exit the test.

Error report

Test number	(13H)
Expected data	N/A
Actual read data	N/A
Type of failure	Digital Audio Receiver detects bad data

Dig Aud IO Through

This test is a quick diagnostic tool that bypasses the main operating system to set up digital input and analog input mixing. The mixed stereo output is then fed to both the analog output and the digital output. The left and right digital outputs should put out the same as the left and right analog outputs. Internal 44.1kHz or External 48.0kHz wordclock can be selected. Note that if this test is used for critical audio testing, the fact that analog and digital inputs are summed together must be taken into account. For instance, D-to-D and D-to-A performance will have analog noise added in. However, A-to-A and A-to-D performance will be accurate if no digital input is plugged in since the digital input is zeroed under that circumstance. In general, it is better to follow previously outlined procedures that take performance measurements while running the main operating system of the unit.

Infinite Test Loop

Before running the Infinite Test Loop, note that previous error log information may be overwritten (erased) if a failure occurs. It's good practice to clear the Error Log File before executing the loop. It will then be easier to identify which test failed and how many times the failure occurred.

This test continuously runs a series of tests to uncover intermittent failures. In order to use this test without causing a false errors, a MIDI cable must be connected between the PCM 81 MIDI Out and MIDI In jacks. The following tests are executed in the Infinite Test Loop:

MIDI Test (#0CH)
Slave Z80 SRAM Test (#14H)
Word Clock Select Tst (#10H)
Slave To Host Interrupt Test (#16H)

After the first successful loop, **PASSED** will be displayed. If a failure occurs, the bottom half of the display will indicate **FAILURE**. If ten errors occur during the Infinite Test Loop, the test will halt to prevent the information in the Error Log file from being overwritten. (This file protection feature is active only during the Infinite Test Loop. In other situations where the Error Log is recording errors from the Power On Diagnostics errors and Extended Diagnostic errors, the oldest information in the Error Log will be over written when 20 errors are recorded in the Error Log file.)

Show Error Log

This feature allows the Error Log File to be viewed while the Extended Diagnostics are being executed. When selected (after pressing **Load**), the display will indicate the last test that was able to get recorded in the 20-record ring buffer.

Clear Error Log File

Clearing the Error Log File erases all error information in the 20-record ring buffer. When selected (after pressing **Load**), the message **WARNING! Erase Log?** will appear on the bottom half of the display.

Press **Store** to clear the Error Log. The message **Error Log Cleared** will be displayed. The Error Log can also be cleared by clearing the SRAM. This is done by pressing and holding down the ▼ and **Tap** buttons while powering on the PCM 81 and waiting for the display to read:

WARNING! Press STORE
to clear the SRAM

Press **Store** to clear the SRAM, then press any button to continue the Power On diagnostics.

The Error Log File is not cleared during System Initialization.

Troubleshooting

Problems with the PCM 81 can usually be classified as user interface problems or audio problems. User interface problems can range from one non-functioning front panel control to no display. Audio problems affect the signal quality from the analog or digital audio inputs and outputs. Some failures can be traced directly to one particular subsystem within the PCM 81, while others are caused by multiple sub-system failures.

When a problem is encountered, it is good practice to verify overall operation of the PCM 81 by running both the Power-On Diagnostics and the supplemental Extended Diagnostics. Refer to the Diagnostic functional instructions and troubleshooting hints given earlier in this chapter.

User Interface Problems

Display problems

Verify that all cable connections from the Host/Motherboard (J18-J22) to the various Front Panel boards are secure.

Vibration can eventually break the strands of cables making them intermittent or possibly open. Connections can become oxidized, corroded or otherwise contaminated causing them to be intermittent, open or resistive. For all of these reasons, caution should be used in troubleshooting. Before any cables are removed, they should be carefully inspected for proper seating and checked for continuity at all points between the Host/Motherboard and the Front Panel boards.

Verify that the +5VD supply is operational and within specification. Check the distribution of the supply to ensure that power is reaching the appropriate front panel display buffer and the register ICs.

If only one control on the Front Panel is failing, then the problem is probably a bad switch, encoder or potentiometer. If more than one control is failing, the problem may be with the Host Processor. Refer to the Diagnostic Descriptions and Theory of Operation.

Audio Problems

The first step when troubleshooting audio problems is to collect as much information as possible. The following lists some basic questions which should be answered before any repairs are attempted.

Is the problem:

1. on one output only?
2. at certain signal frequencies only?
3. at certain signal levels only?
4. in certain programs only?
5. at certain sample frequencies only?
6 with input only?
7. only without input?
8. temperature sensitive?
9. shock sensitive?

In general, it is best to verify overall audio performance and to further isolate the problem by running all of the audio proof-of-performance tests. This can be vital when troubleshooting subtle problems. Some system failures may cause a variety of tests to fail but troubleshooting based on one symptom type may be much easier than another. For example, a bad capacitor may produce a high level of distortion and a frequency response problem. The frequency response problem is easier to trace because the signal level can be monitored throughout the signal path on an ordinary oscilloscope.

One Bad Channel

One of the most useful pieces of information is determining whether a problem occurs on only one or on both channels. If the problem occurs at only one output, the following assumptions can generally be made with some level of confidence:

1. The power supplies are OK.
2. The system timing (clocks) is OK.
3. The digital circuitry (except for A/D and D/A conversion) is OK.

This type of problem can be fairly easy to troubleshoot, as the working channel can be used as a reference. With the same signal applied to both inputs, compare the signals on both channels at various points along the analog signal path. This may localize the problem fairly quickly.

The system diagnostics may be helpful in isolating RAM or DSP processor failures that might cause bad audio. Refer to the Diagnostics Descriptions for more information.

Both Channels Bad

As the likelihood of two separate components failing in the same way at the same time is remote, problems which occur in both channels can usually be traced to a component or components that are common to both channels, or to a system problem such as a power supply or timing problem. Verify that the power supplies are operational and within specification. If there is no output, refer to the next section.

No Output

First, determine whether the problem occurs on one or both channels.

When the machine has no output from only one channel, apply the same signal to both inputs, then compare the signals on both channels at various points along the analog signal path.

When the machine has no output from either channel, verify that the ±15V and the ±5V analog power supplies are operational and within specification. If the power supplies are OK, determine whether the problem lies within the A/D or the D/A conversion, then troubleshoot the corresponding circuitry.

Internal Adjustments and Troubleshooting

The following information allows testing of a non-functioning unit: no display, pegged input meters, load noises, popping crashes and /or no output. Test procedures are provided for checking power supplies, system clocks , battery voltage, and both analog and digital signal paths.

WARNING **CAUTION**

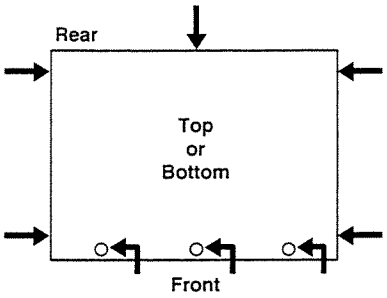
As these tests require removal of the PCM 81 cover, it is imperative that these tests be performed with regard to all safety and ESD precautions.

Required Equipment

- DMM (Digital Mulitimeter)
- Frequency Counter
- 100 MHz oscilloscope (with 1X ,10X probes)
- Bench power supply providing a variac voltage adjustment and transformer isolation

Removing the Top and Bottom Covers

Remove the eight screws which attach the top cover. Repeat for the bottom cover.



WARNING

THE POWER SUPPLY IN THIS UNIT HAS A LIVE HEAT SINK. DO NOT TOUCH WHILE THE UNIT IS PLUGGED IN AND POWERED ON.

Power Supply

1. Plug in the PCM 81 and set the variac for nominal line voltage. A clicking noise from the relays should occur 30 seconds after you have powered up the PCM 81.
2. Set DMM to measure VCD, and check the regulated voltages for proper levels. Use the ground test point (GND-4), located on the board to the right of U9 as a ground reference, The test points for the supplies in the unit are shown below.

Supplies	Location	Range
+5VD	U37 Pin 20	(4.85-5.35)
+15V	Right of U9	(15.00-16.95)
-15V	Just above U9	14.25-15.75)
+5VA	Right of U9	(4.75-5.25)
-5VA	Right of U9	(4.75-5.25)

Internal Battery Voltage

1. Power off the PCM 81 and detach the power cord.
2. Set DMM for a DC voltage reading on the 20volts DC scale.
3. Place the positive (red) DMM Probe on top of the battery located just behind the front panel on the main board.
4. Place the negative (black) probe on the test point marked FOOTPEDAL ADC GND-10 to the right of U37 in the middle of the board.
5. The reading on the DMM should be ≥ 2.75volts. Replace the battery if the voltage is at 2.75 volts or lower.

System Clocks

These procedures test the major crystals and other clocks that are important to the operation of the unit. A frequency counter and an oscilloscope are required for these tests. The oscilloscope's ground lead should be connected to the PCM 81 chassis (away from the power supply).

1. Looking down on the unit with the top cover off, locate the DSP board which is screwed on to standoffs just to the right of the power supply area. Near the center of this board is Y1, a crystal that runs the Lexichip. Measure either side of this with the frequency counter. The reading should be 25.8MHz.

2. Turn PCM 81 power off and detach the power cord. Remove the screws that hold the DSP board in place. Remove the board and turn the power on. The message: Error E7 will be displayed.

3. Measure Y1, Y2, and Y3. Y3, the 16MHz clock that runs the microprocessor, is located to the left of the microprocessor (U34). Place the probe at U40 pin 1.

   Crystals Y1 (the 12.28MHz crystal) and Y2 (the 11.29MHz crystal) are located toward the rear of the unit. To measure Y1, which is used to generate the 48kHz Sample Rate Clock, place the probe at U21 pin 10.

   To measure Y2, which is used to generate the 44.1 kHz Sample Rate, place the probe at U22 pin 10.

Analog Audio Signal Tracing

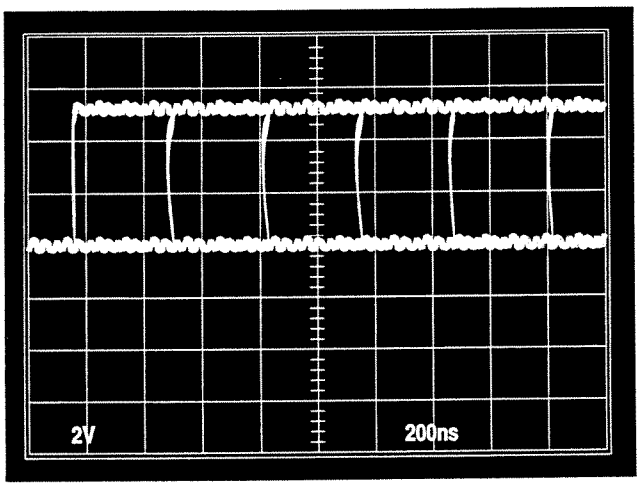
Required Equipment

- Level meter with oscillator
- Oscilloscope (to confirm audio signals for any visible problems)

Setup

1. Place the PCM 81 in Bypass, Analog InLvl=100%, OutLvl=+4dBu, Sample Rate=Internal 44.1 or 48kHz. (See Analog Audio Performance Check: Setup).
2. Apply a 1kHz signal @ -20dBu (77.5 mVrms)
3. Turn input pot fully clockwise.

Name	Measurement Point	Levels
Input Stage	U3 Pin 7 Left signal U3 Pin 1 Right signal	-20dBu–Input Switch OUT or 0dBu–Input Switch IN
Input Level Pot	R93 Left Signal R92 Right Signal	-20dBu OUT or 0dBu IN (77.5mVrms-0.775 Vrms)
Left ADC Buffer	LADC+, LADC-	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
Right ADC Buffer	RADC+, RADC-	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
ADC Inputs	U10 Pins 4+5 Left U10 Pins 24+25 Right	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
ADC Outputs	U10 Pin15 or R76	This is a Digital audio signal +5volt CMOS Characteristics If there is no output at this pin check for clocks at 256FSA at pin 19, 64FSA at pin 14, WCA/ at pin 13) WCA/ = Sample Rate (44.1 or 48kHz) 64FSA = 64xSample Rate (2.82 or 3.07MHz) 256FSA = 256xSample Rate (11.29 or 12.28MHz)



D/A Converter Input	U8, Pin10	Digital audio signal

DAC Outputs Audio signal	R58+R60 R72+R74	Left out Right out	-16dBu OUT (0.123m Vrms)	or	+4dBu IN (1.23 Vrms)
Lowpass Filter	LDAC RDAC	Left out Right out	-14dBu OUT (0.154mVrms)		+6dBu IN (1.54Vrms)
Output Gain Stage	LOUT ROUT	Left out Right out	With output level set at +4dBu: -4dBu OUT (0.489mVrms With output level set at -10dBu: -18dBu OUT (97.5mVrms)		+16dBu IN (4.89 Vrms) +2dBu IN (0.975Vrms)
Output Drivers	LOUT+, LOUT- ROUT+, ROUT-	Left out Right out	With output level set at +4dBu: -4dBu OUT (0.489mVrms With output level set at -10dBu: -18dBu OUT (97.5mVrms)		+16dBu IN (4.89 Vrms) +2dBu IN (0.975Vrms)

Digital Audio Signal Tracing

This procedure verifies the Digital Audio Path of the PCM 81.

1. The input for the Digital signal is RCA J12 (white, marked S/PDIF) or XLR J10 (marked AES/EBU) on the back of the PCM 81.Typical input level is 0.5 Vpp for S/PDIF. The signal goes to the input of the Digital Audio Receiver (U15, Pin 9) after buffering (U19 pin 12/10) and selected by U16 pin 2/15. Depending on which is selected, S/PDIF or AES/EBU digital signals will appear at U16 pin 15. U15 outputs a serial audio data stream at 5Vpp (typical) via Pin 26.
2. The signal travels to pin A8 of J16, then goes to the DSP board for processing.
3. After the signal is processed, it comes back down onto the Host board via pin B16 of J16, and then passes through a gate (U45, Pins 1 and 3). The 5Vpp signal goes to the input of the Digital Audio transmitters (U17, U18, pin 8). Audio Transmitter U17 generates the AES/EBU formatted signals which are output through the isolation transformer (TX2) to meet the AES standard at the output jack (J11).
4. The Digital Audio Transmitter (U18) generates the S/PDIF formatted signal. This 5Vpp signal exits U18 at Pin 20 and goes through a resister divider network (R110, R111) to bring the signal level down to 1Vpp. When properly terminated by 75Ω, the signal level will drop further to 0.5Vpp.

System Signal Tracing

This procedure tests basic digital control signals in the PCM 81. For each of the following signals, load **P0 0.0 Prime Blue**, probe at the indicated place, and check for the expected results.

DSP Board Clocks

FCLK — DSP board: Probe on circuit-side at either side of R44
DSP56002 Clock: Should be a 40MHz square wave.

SLVCLK, SLVCLK/ — DSP board: Probe on circuit-side at either side of R47 and R46, respectively
Slave Clocks: Should be a 10 MHz square wave.

Misc Signals

HWAIT/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin B26) Host Wait Signal. Double low-going pulse spaced at about 10 µS apart. These two pulses should repeat every 20mS. More activity can be seen when adjusting the size parameter in the Edit menu (matrix position **2.0**).

MUTE/ — (U32 pin 15) Master Mute Line: Normally high, low on power-up.

Reset Signals

MRST/ — (U69 pin 1) Master Reset: Normally high, low on power-up.

SLVRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin A22).
Slave Reset: Normally high, low on power-up.

LEXRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin A20).
Lexichip Reset: Normally high, low on power-up.

56KRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin B10).
DSP56002 Reset: Normally high, low on power-up.

Interrupt Signals (See Theory of Operation: Interrupt Timing)

HNMI — (U38 pin 3) V40's NMI line: Normally low. When DIOIMSK/ is high, it is pulsed high on digital I/O errors such as as loss-of-lock

PROGINT5 — (U49 pin 2) V40's INTP5 line: Periodic high-going pulse
Pulse width=10mS (approx.)
Period=20ms

PROGINT7 — (U49 pin 6) V40's INTP7 line: Periodic high-going pulse
Pulse width=11ms (approx.)
Period=40 ms

WDKICK/ — (U48 pin 5) Watch Dog Timer Kick Pulse:
Pulsewidth=150nS
Period=1mS

Encoder Signals

ASNB, ASNA — (U73 pins 3 and 2 respectively)
Adjust Soft Knob Lines B and A: As ADJUST is rotated clockwise, the following patterns should rotate in relative order:
High, High
High, Low
Low, Low
Low, High

SSNB, SSNA — (U73 pins 5 and 4 respectively)
Select Soft Knob Lines B and A: As ADJUST is rotated clockwise, the patterns described above should rotate in relative order.

LED/Switch Scanning Signals

LHRCOL/, RHRCOL/ — (U65 pins 14 and 13 respectively)
Left and Right Headroom LED Column Strobes: Square Wave with a 4mS period.

SWC0/, SWC1/, SWC2/ — (U68 pins 19, 18, 17 respectively)
Switch & LED Column Strobes: Low-going pulse, Pulse width=2 mS, Period=6mS

LDRW0/, LDRW1/, LDRW2/ — (U68 pins 16, 15, 14 respectively)
LED Row Strobes: Reload P0.0 Prime Blue.
Observe the following on U68 pin 16:
Low-going pulse, Pulse width=2mS, Period =6mS

Press "Edit" Button.
Observe the following on U68 pin 15:
Low-going pulse, Pulse-width=2mS, Period=6mS

Press "Register" Button.
Observe the following on U68 pin 14:
Low-going pulse
Pulse width=2mS, occasionally 4mS when tempo light blinks
Period=6mS

Restoring Factory Settings

The following procedure restores the PCM 81 factory default settings. This may be necessary due to memory problems, or following internal battery replacement.

This procedure will destroy any user settings or registers. Save setups and registers on a Memory Card to reload after this proceudre is completed.

1. Set the INPUT GAIN switch on the rear panel of the PCM 81 to the OUT position.
2. Set the front panel INPUT control fully counterclockwise.
3. Press **Down** until the display reads: **System Edit Mode/1.0/Go**
4. Turn SELECT until the display reads: **System/Initialize/1.8 (Press STORE)**
5. Press **Store** and verify that the display flashes the following message: **Are you sure? (Press STORE)**
6. Press **Store** and verify that the display flashes the following message for about 1/2 second: **Restoring Original Factory Settings...** then the message: **Loading Effect ...** then the display: **Chorus+Rvb/P0 0.0/Prime Blue**
7. Turn off the PCM 81 and detach the power cord.
8. Remove the 4 phone plug cables from the PCM 81.

The following procedure will restore the factory defaults without destroying the user registers, but may leave erroneous data in RAM.

1. Press **Control**, then use the ▲ and ▼ buttons to display: **Row 4 Setup.**
2. Turn SELECT until the display reads: **4.1 Load.**
3. Turn ADJUST counterclockwise to display: **Factory Settings.**
4. Press **Load.** The display should show: **Setup restored.**

5

Theory of Operation

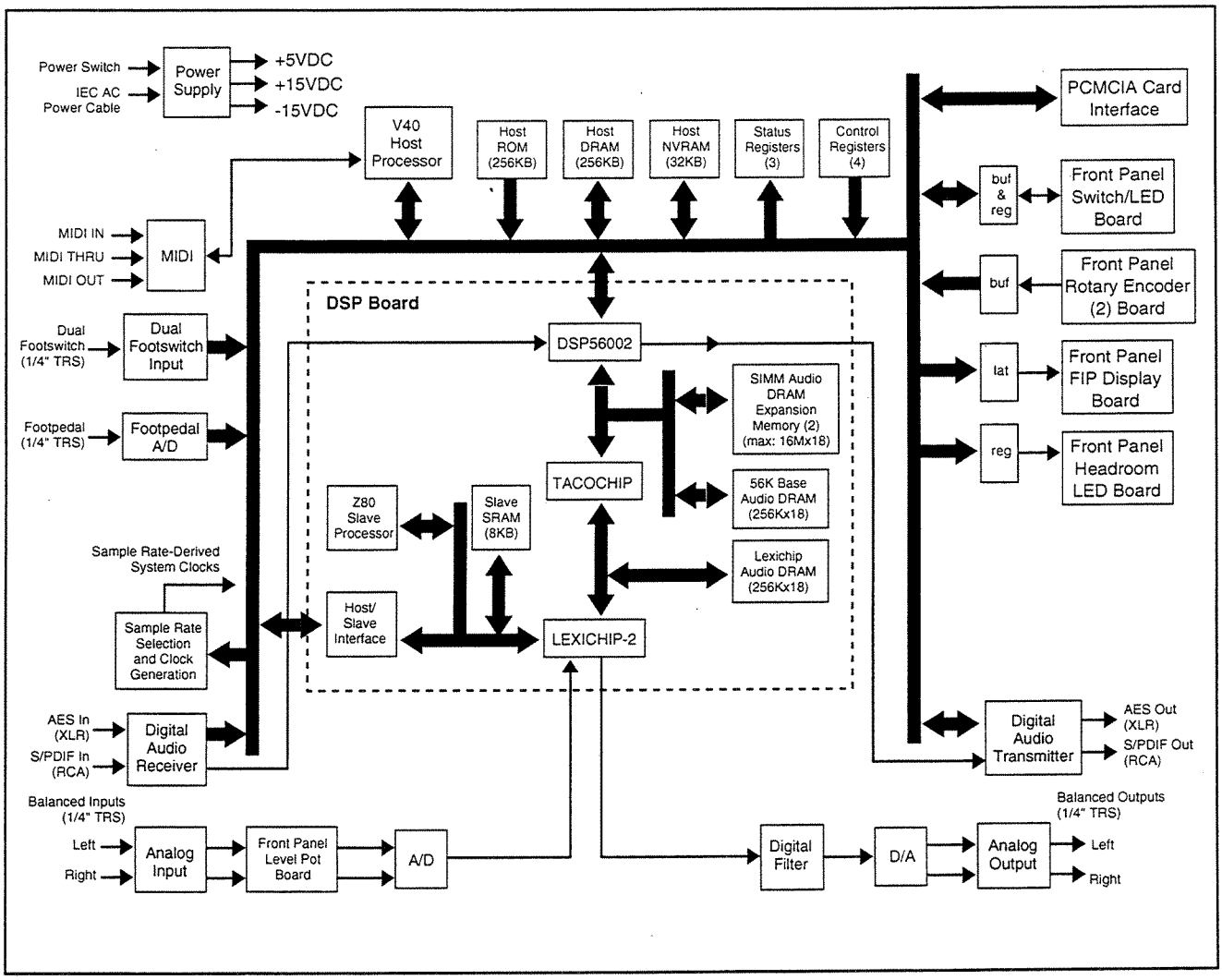
Architectural Overview

The PCM 81 digital hardware utilizes multiple microprocessors and digital signal processors to perform digital audio effects which are controlled via the front-panel interface, and the MIDI serial interface.

The PCM 81 features five major circuit sections: Host, DSP (Digital Signal Processing), Digital I/O, Analog Conversion, and Power Supply sections. A 10 MHz NEC uPD70208, also known as the V40, provides host microprocessor functions. The host processor circuit manages the user interface including the FIP display, softknobs, switchboard, status and headroom LEDs, MIDI, the footswitch and footpedal, and digital I/O circuitry. It is also responsible for program-load and parameter-passing to the DSP circuitry on the DSP board. The DSP board is responsible for the digital effects processing of the PCM 81. It has a unique tightly-coupled multi-DSP engine featuring three ASICs (Application Specific Integrated Circuits): Lexicon's proprietary Lexichip-2 and Tacochip, and a Motorola DSP56002. A slave microprocessor, the Zilog Z-80, provides independent housekeeping functions for the Lexichip-2. The analog conversion circuitry handles A-to-D conversion and D-to-A conversion as well as a high performance analog interface to the balanced-line jacks on the rear-panel. The digital I/O circuitry implements S/PDIF and AES/EBU digital audio I/O.

The PCM 81 is physically sectioned into two major circuit boards, five minor circuit boards and a power supply module. The two major circuit boards are the Host Board and the DSP Board. The host processor, digital I/O and analog conversion circuitry reside on the Host Board while the DSP circuitry resides on the DSP Board which connects to the Host Board directly via a 72-pin connector. Smaller boards which are connected to the Host Board include the Front-Panel Switch Board, Front-Panel Encoder Board, Front-Panel Headroom Indicator LED Board, Front-Panel Input Level Pot Board, and the Intelligent FIP Display Module. The Power Supply Module supplies +5VDC, +15VDC, and -15VDC.

Block Diagram



Host Processor Circuitry

The Host Circuit is responsible for management of front-panel controls and displays, MIDI interface, Tap/Tempo/LFO functions, and download and real-time control of DSP code. There are 256K bytes of ROM, 256K bytes of DRAM, and 32K bytes of battery backed-up SRAM. The 32K bytes of SRAM are for non-volatile system parameter and user register storage.

The main processor of the host circuit is the NEC V40 (uPD70208) (U34). The V40 CPU has several on-chip peripherals including an 8-level priority interrupt controller, DMA controller, timers, and a serial port. The 8-level interrupt controller allows for management of several time-critical periodic tasks in order to meet the real-time requirements of the PCM 81. The DMA controller allows DSP-code download to happen in the background without significant impact on system performance. The timers provide MIDI UART clock generation, and timing references for tempo and LFO functions. The serial port is used to implement the MIDI interface.

In summary, the main host responsibilities are:

- Management of the user-interface:
  Intelligent front panel display FIP
  Front-panel switches
  Switch status LEDs
  Headroom LEDs
  Foot controller pedal jack via 8-bit A/D
  Footswitch jack
- Processing data and instructions to and from the MIDI UART (internal)
- Maintenance of non-volatile SRAM for storage of user registers
- Transparent refresh of Host DRAM.
- Providing download/upload to/from PCMCIA card interface
- Loading of slave Z80/Lexichip program code and data
- Controlling slave Z80/Lexichip reset and interrupt functions.
- Loading of DSP56002 program code and data
- Controlling DSP56002 reset, interrupt, and DMA functions
- Selecting sampling rate to be 44.1 kHz, 48 kHz or PLL frequency
- Management of channel status and reset functions for digital I/O interface
- Controlling audio muting hardware
- Management of user-defined control patching and LFO functions
- Management of Tap key and Tempo functions

Clocks

A 16 MHz crystal (Y3) is used to generate an 8 MHz clock used as the internal processor clock. This clock is also sourced from the V40 (HCLK) to clock external control logic: a hex flip-flop (74HC174) at U46 and a GAL20V8 at U40. HCLK is also inverted by a 74AC00 (U42) to source HCLK/. HCLK/ clocks a hex flip-flop (74AC174) at U47 and a GAL16V8 on the DSP board.

Bus Interface

The V40's 8-bit data bus is bidirectionally buffered by a 74HC245 (U35). Since twelve of the twenty V40 address lines are multiplexed with data and processor status, two 74HC573s (U36, U41) are used to latch and buffer sixteen of them (HA<19:0> less HA<11:8>). HA<11:8> are sourced directly from the V40.

Host Bus Status lines (HBS<2:0>), Host Memory Read Line (HMRD/), Host Memory Write Line (HMWRB/), and the Host Refresh Request Lines (HREFREQ/) are sourced to the GAL20V8 for memory interface logic.

Interrupts

The host processor has nine interrupts: one non-maskable interrupt (NMI) and eight maskable priority interrupts (INTPx). The priority ordering of the eight priority interrupts is preset as follows: INTP0 (highest) to INTP7 (lowest).

	Non-Maskable Interrupt
NMI	Digital Audio Receiver Error Condition
	Maskable Interrupts
INTP0	Timer 0 (LFO Interrupt) (Periodic: 1 msec) (Internal) (Highest Priority)
INTP1	MIDI Port Transmit/Receive (Internal)
INTP2	Timer 2 (Front Panel Display Interrupt)
INTP3	DSP56002 DMA Transaction Complete
INTP4	DSP Interrupt (Z80 or DSP56002)
INTP5	Programmable Interrupt P5 (Patch Calculations Process)
INTP6	Programmable Interrupt P6 (reserved for future enhancement)
INTP7	Programmable Interrupt P7 (Front Panel Interface Process) (Lowest Priority)

INTP0 and INTP1 are sourced internal to the V40. INTP2 is sourced from the V40's Timer 2. INTP3 is sourced by the V40's DMA controller Transaction Complete Flag ("TC/"). INTP4 is sourced externally by an interrupt sourced either by the Z80 or the DSP56002 on the DSP board. The interrupt can be identified by reading 56KINT and SHINT in Status Register 1. (U33 pins 3 and 2.) 56KOVRL/, a parallel control bit toggled by the DSP56002, is the source of the interrupt. It is gated by a 74HC08 AND gate with FINTMSK/ to generate 56KINT. (56KINT is enabled when FINTMSK/ is high, and disabled when it is low.) Note that, as the interrupt 56KOVRL/ is the inverted PC4 bit of the DSP56002, the default state of PC4 should be high. For the DSP56002 to interrupt the host, PC4 should be set low until the host sends a interrupt-acknowledge message via the host port to reset the bit high. INTP5, INTP6 and INTP7 are sourced by software-programmable bits in Control Register 1 (U49 pins 2, 5 and 6). The interrupts are rising-edge triggered.

When probing with an oscilloscope, the following should be observed on each of the V40's interrupt pins, while running the program **P0 0.0 Prime Blue**:

NMI	(U34 pin 66)	Normally low. (When DIOIMSK/ is high, it is pulsed high on digital I/O error such as loss-of-lock)
INTP0		Not accessible (Internal to V40)
INTP1	(U34 pin 37)	Not accessible (Internal to V40) (Externally grounded)
INTP2	(U34 pin 38)	Periodic low-going pulse (Pulse-width=250ns, Period=2ms)
INTP3	(U34 pin 39)	Periodic low-going pulse (Pulse-width=125ns, Period=3.6ms (approx.)
INTP4	(U34 pin 40)	Non-periodic
INTP5	(U34 pin 41)	Periodic high-going pulse (Pulse-width=10ms (approx.), Period 20ms)
INTP6	(U34 pin 42)	Reserved for future enhancement
INTP7	(U34 pin 43)	Periodic high-going pulse (Pulse-width=11ms (approx.), Period 40ms)

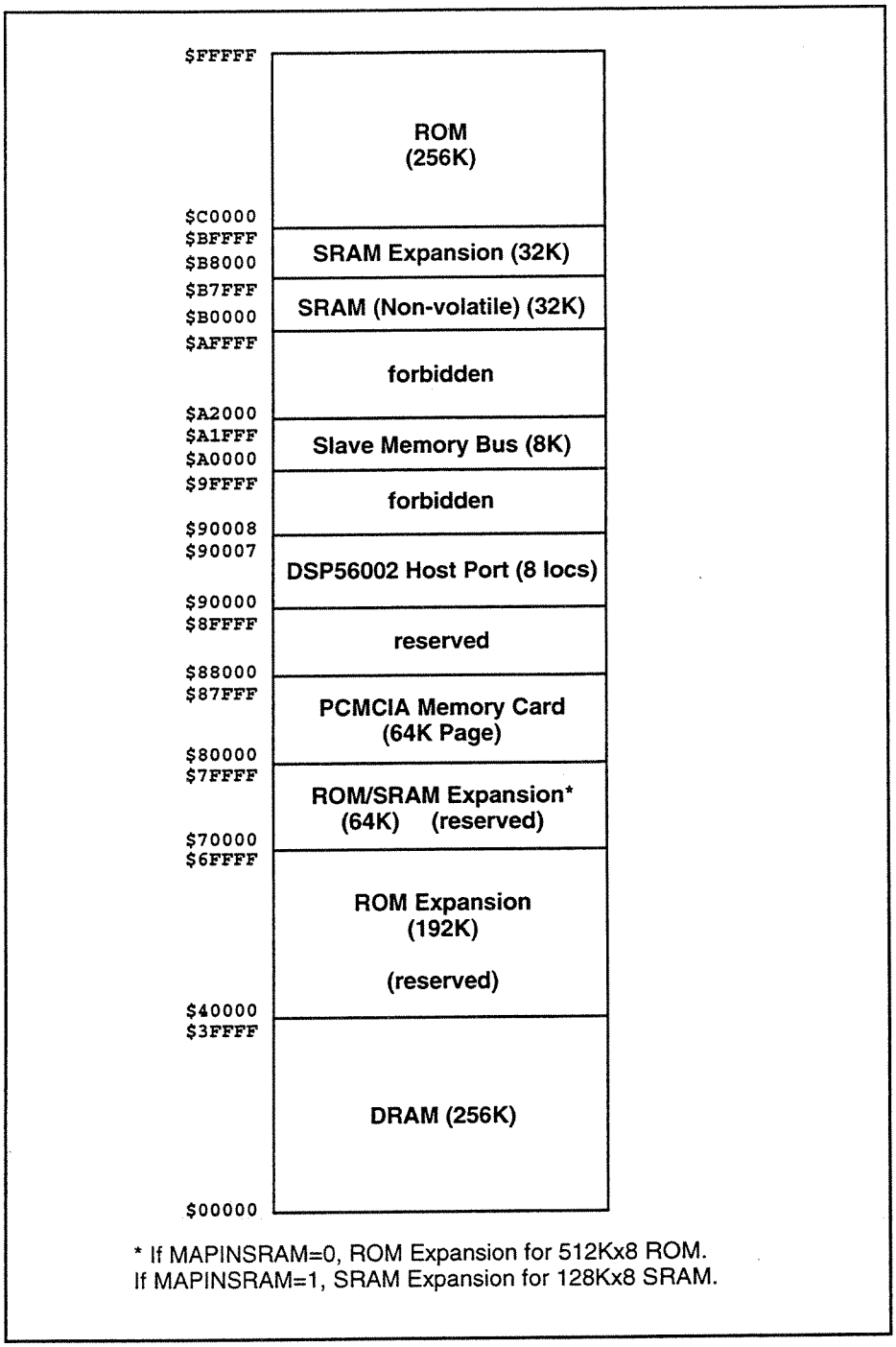
On-Chip Peripherals

V40 on-chip peripherals include:

- Clock generator
- Bus interface
- Bus arbitration
- Programmable wait-state generator
- DRAM refresh controller
- 3 16-bit timer/counters:1 for MIDI UART clock, 1 for 2ms display interrupt tick, 1 for 1ms interrupt tick
- Asynchronous serial I/O controller (for MIDI)
- 8-input interrupt controller
- 4-channel DMA controller (Only one used – for DSP56002 host port transactions)

Host Memory

A GAL20V8 (U40) provides memory decoding for ROM, SRAM, DSP56002 Host port, Slave Z80 RAM Access, and DRAM. Following is the Host V40 memory map:



Memory Address Map

ROM

A 27C020/27C2001 (U55) which is a 2-megabit EPROM in a 256Kx8 configuration is installed.

The ROM enable signal (HROMEN/) is sourced by the GAL20V8 (U40) to enable the ROM when the memory address range is $C0000 to $FFFFF. (If a 512Kx8 ROM is used, the lower 256KB is mapped to $40000 to $7FFFF, and the higher 256KB is mapped to $C0000 to $FFFFF. Note that the upper 64K of the lower 256KB is displaced by SRAM if a 128KB SRAM is used and the control bit MAPINSRAM is asserted.)

Dynamic RAM (DRAM)

256Kx8 Dynamic RAM is provided. Two 44256 (256Kx4) parts at locations U50 and U51 in 20-pin ZIP packages are used to implement high and low nibble. U51 implements the low nibble. Refresh is taken care of by the V40 automatic refresh cycle which needs to be set up by software. Host address bits 17-0 are multiplexed to provide 9 row and 9 column address bits.

DRAM control is implemented by a GAL20V8 (U40) and a 74HC174 (U47). The GAL generates two signals DMEMOP/ and SELCA. DMEMOP/ is asserted for both read and write accesses to the DRAM. This signal is clock-delayed by U47 to generate HRAS/, the row address strobe. PTHRAS/ (pre-terminated version of HRAS/) is clock-delayed once again to generate HCAS/, the column address strobe. SELCA goes to 74AC157 multiplexers (U56, U57, U58) to source row and column address lines. When SELCA is asserted high, address lines HA<19:10> are selected to source the column address to HDRA<9:0>. When SELCA is not asserted (low), address lines HA<9:0> are selected to source the row address to HDRA<9:0>. During DRAM access, HMRD/ distinguishes between reads and writes. When HMRD/ is asserted low, it is a read operation. Otherwise it is a write operation.

The timing of the Host DRAM interface is shown in detail in later in this chapter.

Non-Volatile Battery Backed-Up Static RAM

A battery backed-up 32Kx8 Static RAM (U54) is provided to implement non-volatile storage. It is primarily used for system control parameter and user register storage. The 32-pin SRAM socket is factory shipped with a 28-pin 32Kx8 SRAM, installed with pin 1 of the IC aligned to pin 3 of the 32-pin socket.

The following table outlines the memory mapping for various configurations. The signal NVRAMEN is asserted by the GAL20V8 depending of the address lines and the control signal MAPINSRAM. MAPINSRAM, when asserted, allows the full use of 128Kx8 SRAMs. However, the lower 64KB of SRAM displaces the upper 64K portion of the reserved ROM expansion space. As current software only supports the 32Kx8 SRAM, MAPINSRAM should never be asserted.

RAM Type	MAPINSRAM	Memory Size	Address Range
32K x 8	0	32KB	$B0000-$B7FFF
128K x 8	0	64KB	$B0000-$BFFFF (upper 64KB only)
128K x 8	1	128KB	$70000-$7FFFF (lower 64KB)
			$B0000-$BFFFF (upper 64KB)

NVRAMEN is inverted by a 74AC00 (U61) NAND gate to yield QNVRAMEN/ which is an asserted-low signal going to the chip enable of the SRAM. QNVRAMEN/ is also qualified by PWR_OK which is source from the +5V Monitor (MC34164-U53). When power is going down, PWR_OK gets asserted and QNVRAMEN/ is gated off. The 74AC00 is powered by VRAM which is the battery backup voltage. This ensures that as power goes down, that the CE1/ pin of the RAM tracks Vcc as required by the SRAM manufacturer for reliable data retention. When the unit is on, VRAM should be at 5V. When the unit is on, VRAM follows the voltage from the backup lithium battery (3V) (BAT1).

Battery Backup

The Battery Backup circuitryis designed to protect data in the non-volatile SRAM. It is triggered (controlled) by the +5V Monitor, U53. To ensure the lowest possible leakage current during power on, two transistors (Q8 and Q9) are used to switch between backup operating modes.

A buffer (HC08), guaranteed to operate down to 2V is used to drive Q8. R205 ensures that the transistor stays off while the HC08 Vcc is less than 2V.

D19 is a Schottky diode to minimize the forward voltage drop while power is off. R209 protects the battery in case the diode should fail.

The battery low indicator is set to trigger at approximately 2.1-2.5V. If the battery is low, the status line BATLOW is asserted.

PCMCIA Memory Card

A PCMCIA memory card slot (J23) provides removable user register storage, and capability for algorithm and host software updates. Up to 1 MB of memory on a PCMCIA card is accessable. The host has a 64K window into the card memory space. The PCMCIA card enable signal CARDEN/ is asserted by the HOST GAL20V8 (U40) whenever the address accessed is the range $80000-$8FFFF. The PCMCIA interface in the PCM 81 is designed to handle all cards with an access time of 250nS or faster. The selected 64KB page within the 1MB of card space is set by 4 bits in Control Register 3. This allows up to 16 pages (16x64KB=1MB). The location within the page is selected by the 16 LSBs when the card is selected. The 4-bit page register CA<19:0>, set by Control Register 3 <3:0>, extends the card addressing capability to 1MByte. When the CREG/ control bit (Control Register 3 bit 7) is asserted low, the card's configuration register is selected instead of normal memory access.

Three 71HC541 octal buffers provide address line buffering (U59, U60) and control line buffering (U71). All three are enabled by software when doing card operations, and are disabled otherwise. They are enabled by de-asserting (setting high) DISCARD/ (Control Register bit 6.)

When DISCARD is asserted high:

- Address lines are pulled-down to ground via R187-202.
- CCE1/, COE/, and CWE/ are pulled-up to CVCC via R228, 227, 225.
- CARDENB/ is pulled to a high by R223, disabling the bidirectional data buffer (U70).

A bidirectional data buffer 74HCT245 (U70) is used to isolate the card data lines from the host data bus HD<7:0>. The signal HMRD/ determines the direction. When low, data is enabled from the card data bus CD<7:0> to HD<7:0>. When high, data is enabled from HD<7:0> to CD<7:0>.

Software detects whether or not there is a card installed by reading CARDDET/ (Status Register 0 bit 4). This signal is asserted low when both ends of the PCMCIA card are plugged in, ensuring that the card is not powered-up or accessed until fully plugged in. The end-pin signals: CDET1/ and CDET2/ are pulled high when their respective pins are not inserted. These pins are grounded and, when they are inserted into J23, the corresponding lines are pulled low. A 74AC32 (U72) provides this logic by ANDing CDET1/ and CDET2/ to assert CARDDET/ (low).

Software reads the PCMCIA card write protection switch by reading CWRPROT (Status register 0 bit 5). CWRPROT is a buffered version of CWP via U71. Both CWRPROT and CWP are pulled-up to CVCC. When no card is inserted, CVCC will dischage to ground. Therefore, CWRPROT is not valid unless the card is fully inserted and enabled by setting DISCARD/ high.

The three remaining sections of the 74AC32 (U72) are used to produce a gated version of HMWR/ called PREBCWE/ . This signal gives an earlier rising edge to give the PCMCIA card the proper data setup time. PREBCWE/ is buffered by U66 to source CWE/ (the write enable that goes directly to the card).

The timing of the PCMCIA Card interface is shown in detail later in this chapter. Note that one wait state (generated by the V40 preset by software) is inserted for all card access.

Two status lines (CARDBVD<2:1>) from an inserted SRAM PCMCIA card indicate the condition of its battery. These are read by the host from Status Register 0 bits 3:2 respectively. Both signals are kept asserted when the battery is in good condition. A replacement warning condition is signaled by CARDBVD1 asserted and CARDBVD2 not asserted. In that case, data integrity on the card is still assured. If CARDBVD1 is not asserted, with CARDBVD2 either asserted or not asserted, the battery is no longer servicable and data is lost.

The following summarizes PCMCIA card control bits via Control Register 3:

Control Register 3 (I/O location=$0006)

7	6	5	4	3	2	1	0
CREG/	**DISCARD/**	AESINSEL	MAPINSRAM	**CA19**	**CA18**	**CA17**	**CA16**

The following outlines the PCMCIA card status via Status Register 0

Status Register 0 (I/O location=$0000 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	SINGOUT/	**CWRPROT**	**CARDDET/**	**CARDBVD2**	**CARDBVD1**	spare	FOOTSWR

Host-to-Slave Z80/Lexichip Interface

The host has direct access to the DSP board's Slave Z80 8K SRAM. The Z80, in turn, is responsible for loading and modifying Lexichip program code internal to the chip. The address range for host access to the Slave Z80 SRAM is $A0000-$A1FFF. This memory address range is decoded by the HOST GAL20V8 (U40) to assert SBUSEN/ (low). (This corresponds to the Z80's local address range of $0000-$1FFF.)

Host-to-DSP56002 Interface

There are two methods of Host to DSP56002 communication: Register access using the HA<2:0> address lines, and DMA (direct memory access).

Register access is mapped to host memory addresses $90000-90007. (These locations are duplicated in the whole range between $90008 and $97FFF.) This memory address range is decoded by the HOST GAL20V8 (U40) to assert DSPHEN/ (low). This signal goes directly to the DSP56002 on the DSP board.

The signals HREQ, HACK/, and HMRD3Q synchronize DMA transfers. The signal HREQ from the DSP56002 (on the DSP board) to the host board is clock-delayed by a 74AC174 (U47) to source HREQQ to the DMA request 0 input on the V40. The V40 in turn sources the DMA acknowledge signal HACK/ back to the DSP56002. The signal HMRD3Q gates off HACK/ to source the actual acknowledge line that goes to the DSP56002 (QHACK/) to provide adequate data hold time. This gating is done on the DSP board by a 74AC32. The signal host V40 signal HTC/ is pulsed upon the DMA-cycle's full completion.

Host I/O

I/O Address Map

Two 74HC138s (U62 and U63) provide I/O decoding for writeable and readable registers. The 74AC00 (U42) provides decode for the 8-bit ADC used to read the foot controller jack. The 74HC174 (U46) provides various HCLK delayed signals for I/O interface control. Host I/O address mapping is summarized as follows:

READS:

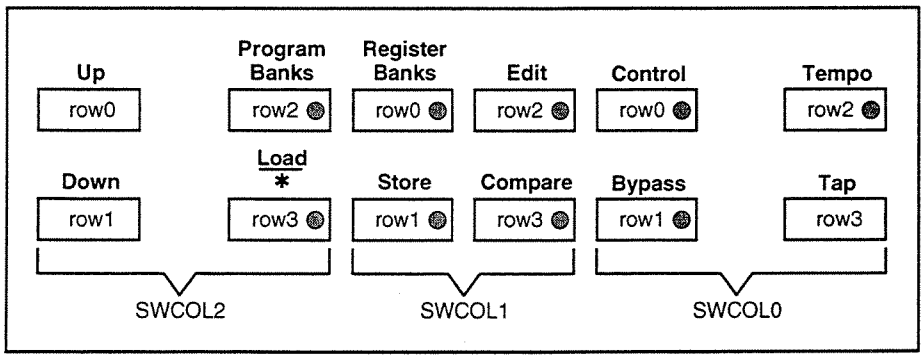
Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0010 (H)	Footcontroller A/D Conversion Data
xxxx xxxx xxx0 111x (B)	$000E (H)	Watchdog Timer Kick
xxxx xxxx xxx0 110x (B)	$000C (H)	Switch Matrix Row and Soft Knobs
xxxx xxxx xxx0 101x (B)	$000A (H)	Clear Slave-to-Host Interrupt
xxxx xxxx xxx0 100x (B)	$0008 (H)	Clear Lexichip Overload Flag
xxxx xxxx xxx0 011x (B)	$0006 (H)	(unused)
xxxx xxxx xxx0 010x (B)	$0004 (H)	Status Register 2
xxxx xxxx xxx0 001x (B)	$0002 (H)	Status Register 1
xxxx xxxx xxx0 000x (B)	$0000 (H)	Status Register 0

WRITES:

Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0010 (H)	Foot Controller A/D Conversion Start
xxxx xxxx xxx0 111x (B)	$000E (H)	Front Panel Display FIP
xxxx xxxx xxx0 110x (B)	$000C (H)	Switch/Status LED Matrix Cols/Rows
xxxx xxxx xxx0 101x (B)	$000A (H)	Set Host-to-Slave Interrupt
xxxx xxxx xxx0 100x (B)	$0008 (H)	Headroom LED rows
xxxx xxxx xxx0 011x (B)	$0006 (H)	Control Register 3
xxxx xxxx xxx0 010x (B)	$0004 (H)	Control Register 2
xxxx xxxx xxx0 001x (B)	$0002 (H)	Control Register 1
xxxx xxxx xxx0 000x (B)	$0000 (H)	Control Register 0

Front Panel Switches

The front-panel switches are arranged on the front-panel board as shown below.



Switches are arranged in a 4 row x 3 column matrix in which each column of 4 rows are read by:

1. Asserting one bit of the Switch Column (SWCOL<2:0>/) field of the SWITCH/ LEDs MATRIX REGISTER (74HC574,U68).
2. Then reading the Switch Row (SWROW<3:0>) field of the the Switch Matrix Input Buffer (74HC541, U73).

The control register and the Switch Column Matrix Buffer are outlined follows:

Switch/LED Matrix Register (I/O location=$000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	LDRW2	LDRW1	**LDRW0/**	**SWC2/**	**SWC1/**	**SWC0/**

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

7	6	5	4	3	2	1	0
SWROW3	**SWROW2**	**SWROW1**	**SWROW0**	SSNB	SSNA	ASNB	ASNA

Soft Knobs

Two 36-position 2-bit gray-code encoded knobs with detents are used to implement the SELECT and ADJUST Soft Knobs. The 2-bits of each (available by reading the Switch Matrix/Soft Knobs Input Buffer) are assigned as follows:

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

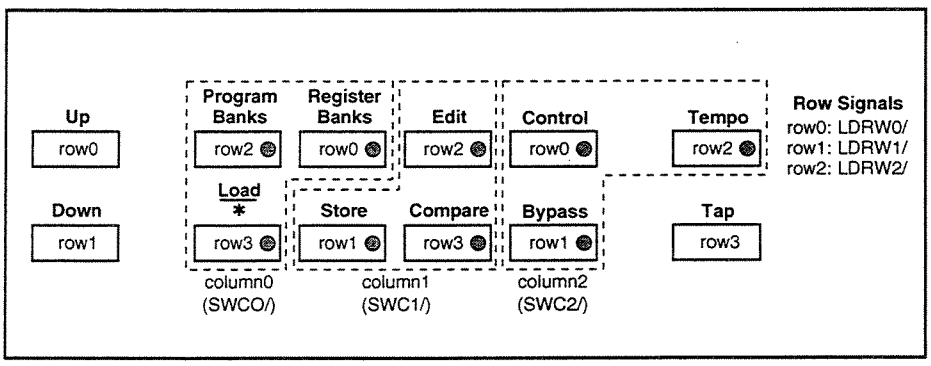
7	6	5	4	3	2	1	0
SWROW3	SWROW2	SWROW1	SWROW0	**SSNB**	**SSNA**	**ASNB**	**ASNA**

The encoded bits for the SELECTSoft Knob are SSNB and SSNA. The encoded bits for the ADJUST Soft Knob are ASNB and ASNA. As each knob is rotated clockwise, the sequence for each pair (SSNB:SSNA, and ASNB:ASNA) should be: LL, LH, HH, and HL, etc. in a rotating sequence. This can be observed at the inputs of the Soft Knobs Input Buffer (U73) pins 5 & 4, and 3 & 2 respectively.

Front Panel LEDs

Switch-Status LEDs

On the front-panel board, green LEDs are physically embedded in each of 9 switch button-caps. These LEDs are matrix-driven determined by 6 register bits consisting of 3 columns and 3 rows. The columns are the same as those that drive the switch columns (SWCOL<2:0>). The LED matrix columns and rows are determined by 6 bits of a 74HC574 Octal Register (U68). During operation, each column should individually be asserted for 2ms of a 6ms period. Transistors Q12, Q13, and Q14 source the needed current for each column. R248, R251 and R253 pull down each column when any respective transistor is off. Any LED within a column can be lit by asserting the corresponding rows (LEDROW<2:0>) (asserted-low). When LED(s) are on, peak current through R254, R255, and R256 should be about 20 mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The front panel switches and LEDs are arranged as shown below.



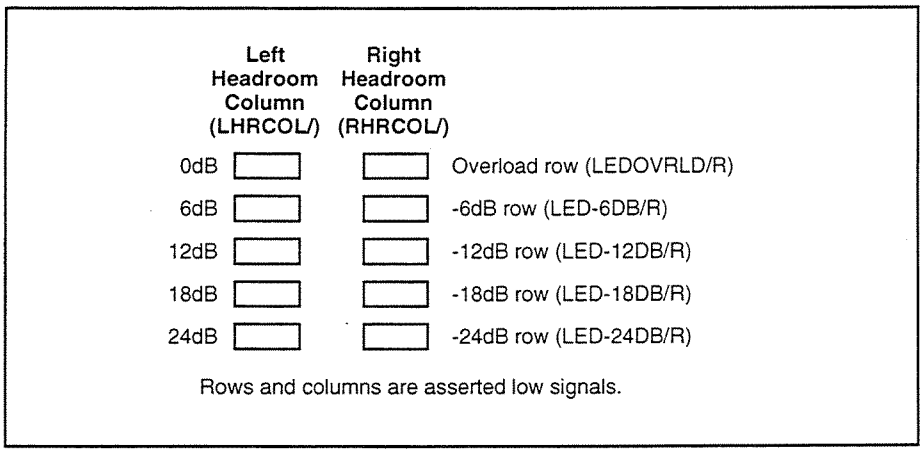
Status LED Column Grouping and Row Assignments

Switch/LEDs Matrix Register (I/O location = $000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	**LDRW2/**	**LDRW1/**	**LDRW0/**	**SWC2/**	**SWC1/**	**SWC0/**

Headroom Indicator LEDs

The Headroom LEDs are matrix-driven determined by 2 columns of 5 rows. The columns and rows are determined by 7 bits of a 74HC574 Octal Register (U65). During operation, each column should individually be asserted for 2ms of a 4ms period. The two columns are LHRCOL/ for the left input level, and RHRCOL/ for the right input level. Transistors Q10 and Q11 provide the necessary current to drive each column's LEDs. R235 and R237 pull down each column when its respective transistor is off. LEDs within a column can be lit by asserting the corresponding rows (LED-24DB/R, LED-18DB/R, LED-12DB/R, LED-6DB/R, LEDOVRL/R). When LED(s) are on, peak current through R238-242 should be about 10.4mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The headroom indicator LEDs are arranged as shown below.



Headroom Indicator LEDs

Column and row control bits are in the headroom LED register. They are summarized as follows:

HeadroomLED Register (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HIOUTLVL	**RHRCOL/**	**LHRCOL/**	**LEDOVRLD/**	**LED-6DDB/**	**LED-12DB**	**LED-18DB**	**LED-24DB**

Front Panel Display

The front panel alphanumeric display is a Futaba M202SD01HA, an intelligent vacuum fluorescent display module with 2 rows of 20 characters each. The module has its own display controller and is connected to the host system bus via an 8-bit data latch (U66). The display data write signal, DISPDWR/, is sourced from the I/O write decoder (74HC138 (U62)). It is inverted by a 74HC04 (U44) to be the latch signal DISPDWR for the 74HC573 (U66) which is the display data latch. When the signal is asserted,. data from the host (HD<7:0>) flows through to source the display connector, then the display. When the signal is de-asserted, the latch is closed, and data should be held. This provides proper hold time for the display. DISPDWR/ goes to the display directly. DISPBSY is a handshake signal that, when asserted high, indicates that the display is busy. When the signal is low, it indicates that the display is ready to accept the next character or command. DISPBSY is monitored by the host via Status Register 1 bit 7 (U33 pin 9).

Display Data Buffer Latch (I/O location = $000E Write-Only)

7	6	5	4	3	2	1	0
DISPD7	DISPD6	DISPD5	DISPD4	DISPD3	DISPD2	DISPD1	DISPD0

For more information, including the character set codes and cursor commands, see the Futaba Dot Matrix VFD Module M202SD01HA Instruction Manual.

Footpedal ADC

An Analog Devices ADC0804 (U37) performs 8-bit A-to-D conversion for the footpedal input. Note that this input (J8) can also be used as a footswitch input in addition to the dual footswitch input jack (J9).

Conversion is started by an I/O write to location $0090. Conversion data is ready after the ADCDONE/ is asserted low (Status Register 0 bit 7). Conversion data is read by an I/O read from location $0090. ADCEN/, the enable for both reads and writes, is sourced by a 74AC00 (U42) via a series-terminating resistor.

Footswitches

The stereo 1/4" jack at J9 provides input for two footswitches. The primary switch should be wired from the tip to the sleeve. (This is the circuit that is used on a mono-plug footswitch.) The secondary switch should be wired from the ring to the sleeve. Each one can be normally-open or normally-closed. The two inputs can also accept a 0-5V voltage level. FB15-16 and C111-112 provide RFI isolation of the footswitches to prevent any high frequency signals from entering or exiting the box. R100, R102, D15-16 provide current limiting and overvoltage protection. R99 and R101 pull the inputs high when the circuit is open. FOOTSWT and FOOTSWR and the respective signals that go to Status Register 0 bits 7 and 0 for host processor monitoring.

MIDI

The MIDI interface in the PCM 81 complies with the MIDI specification. MIDI is implemented using the on-chip serial port of the V40 with buffering between it and the rear-panel 5-pin DIN jacks (J13-J15).

MIDI IN is accepted from J15. A 6N138/139 (U24) provides opto-isolation to source the buffered MIDI signal MIDIIN. This buffered signal goes to the RxD input of the V40 (U34 pin 34).

The unbuffered MIDIOUT signal is sourced from the TxD output of the V40 (U34 pin 35). It is then buffered by a 74HC14 schmitt trigger inverter (U25) and a 2N3904 transistor (Q5) before going to the MIDI OUT jack (J13).

MIDI THRU is sourced by a 74HC14 (U25) and a 2N3904 transistor (Q6) which is a buffered version of the MIDI input (MIDIIN). The MIDI THRU output is provided at the rear panel via J14. W4 provides selection between normal MIDI THRU operation of J14, and a special test mode. For normal operation, W4 should have a jumper shunt on pins 1 and 2. For testing, the jumper may be put on 2 and 3 to have the MIDI THRU jack duplicate the function of the MIDI OUT jack.

Analog I/O (Host Control Interface)

The following describes analog I/O control signals from the host. For further information, see Analog Circuitry.

ADCAL/ is a host control signal going to the A-to-D converter (ADC) and to the D-to-A converter (DAC). ADCAL/ must be asserted low during power-up to calibrate the ADC and DAC, then brought high for normal operation. ADCAL/ must be brought low whenever the sample rate changes to maintain proper operation of the converters.

Control Register 1 (I/O location = $0001 Write-Only)

7	6	5	4	3	2	1	0
FIMTMSK/	DIOMSK/	LEDSEN	**ADCAL/**	**Spare**	PRGINTP7	PRGINTP6	PRGINTP5

The MUTE/ signal when asserted (low) opens the analog output relays to prevent any audio glitches from reaching the analog outputs during power-up and power-down. Also, the MUTE/ signal, when asserted-low gates off analog input, analog output, and digital input serial streams. This gating is done by three sections of a 74HC08 AND gate (U45). When the MUTE/ signal is de-asserted (high), the analog output relay is closed, and the serial audio streams are enabled, allowing audio to pass through.

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	**MUTE/**	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

When the control signal HIOUTLVL is asserted (high), the +4 dBu setting for analog output level is selected. When HIOUTLVL is not asserted (low), the -10 dBu setting for analog output level is selected.

Headroom LED Register 1 (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HIOUTLVL	RHRCOL/	LHRCOL/	LEDOVRLD/	LED-6DB	LED-12DB	LED-18DB	LED-24DB

Digital I/O

The host is responsible for managing the channel status of the Crystal Semiconductor CS8412 digital audio receiver, and the Crystal Semiconductor CS8402 digital audio transmitter. Status Register 2 and Control Register 2 contain bits to monitor and set channel status bits received and transmitted respectively. More details on Digital I/O are given later in this chapter.

System WordClock Source Selection

The user can select from among three different wordclocks (sample-rates): 44.1kHz, 48kHz and External. An 11.2896 MHz crystal (Y2) is used to derive the 44.1kHz wordclock, and a 12.2880 MHz crystal (Y1) is used to derive the 48.0kHz wordclock. (Both crystal circuits use a 74HCU04 (U22,U21) as crystal drivers operating the crystal in its parallel resonance mode.) An on-chip PLL on the CS8412 (U15) digital audio receiver is used to derive External wordclock.

The following table outlines the options for the wordclock source under host control. Note that appropriate digital I/O bits need to be set accordingly.

CTRL2<7> SRSSEL1	CTRL2<6> SRSSEL0	Wordclock Source
0	0	Internal 44.1kHz
0	1	Internal 48kHz
1	0	External Sync from Digital Input
1	1	Disabled (DC tied low)

A 74HC253 (U23) multiplexer controls selection of sources. The multiplexer's output is 256FS. A 74AC74 dual flip-flop (U27), two 74HC161 counters (U28,U29), and a 74HC175 quad flip-flop (U26) divide down 256FS to other various wordclock-dependent clock signals. The following is a summary of these clock signals and their functions:

256FS	Other Variations:	PT256FS, 256FSA
	Frequency:	256 x selected wordclock frequency (50% duty cycle) @44.1 KHz = 11.2896MHz; @48.0kHz = 12.2880MHz
	Function:	a. Goes to 74AC74 (U27) to divide clock down further. b. Goes to the A/D and D/A converters (U10, U8) as their master input clock. c. Goes to DSP board connector (J16) for future functions.
128FS	Other Variations:	PT128FS
	Frequency:	128 x selected wordclock frequency (50% duty cycle) @44.1kHz: 5.6448MHz; @48.0kHz: 6.1440MHz

	Function:	a. Goes to 74AC74 (U27) to divide clock down further. b. Goes to CS8402 digital audio transmitters (U17, U18) as their master clock.
64FS	Other Variations:	PT64FS, 64FSB, 64FS/, 64FSA (inverted)
	Frequency:	64 times the selected wordclock frequency (50% duty-cycle) @44.1kHz: 2.8224MHz; @48.0kHz: 3.0720MHz
	Function:	a. Goes to two 74HC161s (U28, U29) and a 74HC175 (U26) to divide the clock down further. b. Goes to AK5391 ADC (U10), CS4390 DAC (U8) and the Lexichip-2 on the DSP board via connector J16 for analog I/O audio data bit clocking. c. Goes to CS8412 digital audio receiver (U15) and CS8402 digital audio transmitters (U17, U18) and the DSP56002 on the DSP board via connector J16 for digitial I/O audio data bit clocking.
AIOFRAME	Frequency:	2 times the selected wordclock frequency (High going pulse once every 32 64FS bit clocks.)
	Function:	Goes to the Lexichip-2 and DSP56002 on the DSP board to mark the start of a sample frame. (2 frames/Wordclock period.)
WC/	Other variations:	WCA/, CHSEL (inverted)
	Frequency:	User-selected Wordclock frequency of 44.1kHz, 48kHz, or External.
	Function:	a. The falling edge of WC/ (or the rising edge of CHSEL) denotes the beginning of a sample period. b. Goes to Lexichip-2 and DSP56002 on the DSP board via connector J16 to interrupt or reset the processors to the first instruction of the sample-period's instruction sequence. c. WCA/ goes to the ADC and DAC to indicate, when low, that the serial audio data frame corresponds to the right channel. Otherwise it corresponds to the left channel.
TACOSWAP	Frequency:	1/2 that of the selected wordclock frequency.
	Function:	Swaps memory banks in the TACOCHIP to swap data betwen the Lexichip and the DSP56002 buffers at the beginning of every wordclock period.

System Reset Circuitry

PCM 81 reset circuitry consists of four functional blocks, three of which join together and generate the Master Reset (MRST/) signal. The Watchdog Timer, the +5V Monitor, the reset delay circuitry and the Reset Register. The reset circuitry has no provision for early detection of power failure. Therefore, if the +5V Monitor detects less than 4.3V, the hardware will immediately force reset.

After a successful power on and a delay of approximately 0.75 sec., the Host CPU reset, the Reset Register reset, and the UART reset are released. The outputs of the Reset Register, except the Host Master Reset (HMRST), are left in an active state. It is, therefore, the responsibility of the software to release reset for other devices after the reset cycle. The Host can assert Host Master Reset, causing the Watchdog Timer circuitry to create a reset pulse to prevent reset latchup.

Watchdog Timer

The main component of the Watchdog timer circuitry is a Monostable Multivibrator, U48 (74HC4538). The HC4538 has a very well defined trigger input. They are all edge sensitive and have hysteresis. This design takes advantage of that and the retrigger capability of the multivibrator. Kicks from the Host ensure that the Q output of the first device stays high, provided that the kicks occur in shorter intervals than the pulse width. If a kick does not happen within the required time period, the first device will time out and its output will change state from high to low, triggering the second device, which will generate a pulse which will cause C182 to discharge, resetting the system. After the reset pulse disappears, C182 will start charging, as during the power on cycle. The output or the +5V Monitor is also connected to the second MMV, through an AND gate, to ensure an instant reset pulse when power is interrupted. The HMRST signal is connected to the second device's positive edge input, thereby triggering a reset pulse when HMRST is asserted.

As the Watchdog timer circuitry is inactive after power on until it is kicked, the software has to deliver the first kick to activate the timer.

+5V Monitor: The +5V monitor U53 (Motorola MC34164) is a Micropower Undervoltage Sensing Circuit which triggers at +4.33V (+5V increasing) and +4.27V (+5V decreasing). It has an Open Collector output. This device is used to control the Battery Backup and Reset circuitry. The combination of R183 and R184 is selected to ensure minimum VIH when C182 is fully discharged and the +5V monitor's output transistor is turned off.

All control registers are initialized with their outputs in a low state. Control Register 0 contains all other sub-system resets including resets for the digitial I/O circuitry (DIORST/), and for the DSP56002 (56KRST/), Z80 (SLVRST/), and LEXICHIP-2 (LEXRST/) on the DSP board. HMRST is a control register bit which will, when set, reset the entire unit. When the unit is reset via HMRST, the control register itself will be cleared after a delay.

Other initialization related control bits include FRCMOD and MUTE/. FRCMOD must be set when the 56KRST/ line is released high to put the DSP56002 into its proper mode of operation (Mode 5). FRCMOD must be released after reset to allow proper interrupt operation to the DSP56002. MUTE/, like the other control bits, powers up in the low state. This enables all muting circuitry, including holding the audio output relays in an open state. The MUTE/ signal, when asserted, isolates the outputs (both digital and analog) from any power-on/power-off glitches.

The following summarizes the bits involved reset and initialization in Control Register 0:

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	MUTE/	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

Status Bits Summary

Host Status Register 0 (I/O location = $0008 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	Spare	CWRPROT	CARDDET/	CARDBVD2	CARDBVD1	spare	FOOSWR

FOOTSWT	Footswitch Jack Tip Input Level.
CWRPROT	PCMCIA Card Write Protect.
CARDDET/	PCMCIA Card Detect (Asserted-Low).
BVD2	PCMCIA Card Battery Voltage Detect Bit 2
BVD1	PCMCIA Card Battery Voltage Detect Bit 1
FOOTSWR	Footswitch Jack Ring Input Level

Host Status Register 1 (I/O location = $0002 Read-Only)

7	6	5	4	3	2	1	0
DISPBSY	LWAITY/	BATLOW	LEXOVRL/	56KOVRL/	FPLOCK/	56KINT	SHINT

DISPBSY	Front-Panel Display Busy Flag.
LWAITY/	Lexichip Wait (asserted low)
BATLOW	Battery-Low Condition for Non-Volatile SRAM.
LEXOVRL/	Lexichip Overload Bit (Asserted-Low)
56KOVRL/	DSP56002 Overload Bit (Asserted-Low)
FPLOCK/	DSP56002 PLL Lock Condition (Asserted-Low)
56KINT	DSP56002 Interrupt.
SHINT	Slave (Z80) to Host Interrupt.

Host Status Register 2 (I/O location = $0006 Read-Only)

7	6	5	4	3	2	1	0
ADCDONE/	ERF	F2/IGC	FI/ORG	F0/C3/	E2/C2/	E1/C1/	E0/C0/

ADCDONE/	Footpedal ADC done. (Asserted-low)

The following bits are explained in more detail in the Digital I/O Receiver section.

ERF	Digital I/O Receiver Error Flag.
F2/IGC	Digital I/O Receiver Frequency Reporting Bit 2/ Ignorant Category Bit.
F1/ORG	Digital I/O Receiver Frequency Reporting Bit 1/ Original Bit
F0/C3/	Digital I/O Receiver Frequecy Reporting Bit 0 / CS3/
E2/C2/	Digital I/O Receiver Error Condition Bit 2 (asserted high)/ CS2/ (asserted low)
E1/C1/	Digital I/O Receiver Error Condition Bit 1 (asserted high)/ CS2/ (asserted low)
E0/C0/	Digital I/O Receiver Error Condition Bit 0 (asserted high/ CS2/ (asserted low)

Control Bits Summary

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTVLD	MUTE/	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

HMRST	Host Master Reset.
OUTVLD	Digital Output Valid Bit.
MUTE/	Mute Analog I/O (asserted low)
DIORST/	Digital I/O Circuitry Reset (asserted low)
FRCMOD	Force DSP56002 Mode (during 56KRST/ release) (asserted high)
56KRST/	DSP56002 Reset (asserted low)
LEXRST/	Lexichip-2 Reset (asserted low)
SLVRST/	Slave Z80 Reset (asserted low)

Control Register 1 (I/O location = $0002 Write-Only)

7	6	5	4	3	2	1	0
FINTMSK/	DIOIMSK/	LEDSEN	ADCAL/	Spare	PRGINTP7	PRGINTP6	PRTGINTP5

FINTMSK/	DSP56002 Interrupt Mask (Asserted-Low)
DIOIMSK/	Digitial Input Interrupt Mask
LEDSEN	Front-Panel LEDs enable
ADCAL/	A-to-D Converter Calibrate (asserted low)
PRGINTP7	Programmable Interrupt Priority 7
PRGINTP6	Programmable Interrupt Priority 6
PRGINTP5	Programmable Interrupt Priority 5

Control Register 2 (I/O location = $0004 Write-Only)

7	6	5	4	3	2	1	0
SRSSEL1	SRSSEL0	DIOCSSEL	OUTCS15/	OUTCS3/	OUTCS2/	FC1	FC0

The following bits are explained in more detail later in this section.

SRSSEL1:0	Wordclock Source Selection Bits 1:0
DIOCSSEL	Digital I/O Receiver Channel Status Select.
OUTCS15/	Digital I/O Transmitter Channel Status Bit 15 Output (asserted low)
OUTCS3/	Digital I/O Transmitter Channel Status Bit 3 Output (asserted low)
OUTCS2/	Digital I/O Transmitter Channel Status Bit 2 Output (asserted low)
FC1:0	Digital I/O Transmitter Frequency Control Bits 1:0.

Control Register 3 (I/O location = $0006 Write-Only)

7	6	5	4	3	2	1	0
CREG/	DISCARD/	AES INSEL	MAPINSRAM	CA19	CA18	CA17	CA16

CREG/	PCMCIA Register Select (Asserted-Low)
DISCARD/	Disable PCMCIA Card Drivers (Asserted-Low)
AES INSEL	Select AES/EBU Digital Audio Input (otherwise S/PDIF Input is selected)
CA<19:16>	PCMCIA Card Address <19:16> (Page Address)

DSP Board Circuitry

The PCM 81's DSP board is Lexicon's proprietary digital signal processing module. With the exception of the SIMM expansion memory, it does not contain any servicable parts. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair.

DSP56002 Audio DRAM

In addition to the DSP56002's internal RAM, SIMM sockets are provided for expansion audio. The default, on-board 256Kx18-bits DRAM (HM5143280/ uPD42480, U2) may be used, or installable SIMM memory modules (J1, J2) may be used to boost the audio memory to 1MBx18, 4MBx18, or 16MBx18. Upgrading DRAM size may be desirable for applications such as sampling. Note that, when enabled, expansion memory does not add to, but replaces on-board memory.

To select the on-board memory, W1 must have its jumper shunt between pins 2 and 3 (only). To enable SIMM memory instead, W1 must have its jumper shunt between pins 1 and 2 (only). W1 selects to which memory the RAS/ DRAM control line goes. When one line is not connected, R2 and R1 provide pull-up to disable the respective RAS/ line.

Expansion Memory Requirements: 1MBx9, 4MBx9, or 16MBx9 30-pin SIMMs. Modules must be "true parity" (9-bit) type, *not* logical parity (8-bit +parity generator).

Digital I/O

Digital Audio I/O Circuitry

The PCM 81 supports both S/PDIF (IEC-958) consumer and AES/EBU professional digital audio formats. Two RCA jacks (J12) are provided on the rear panel for the S/PDIF interface. The white jack is the input, the red jack is the output. Male and female XLR connectors are used for the AES/EBU interface. Sample rates of 48, 44.1 and 44.056kHz are supported.

Digital Audio Receiver

The S/PDIF input is terminated with a 75Ω resistor per IEC 958 specifications and 33 pF caps for RFI suppression. The input signal passes through a 0.01uF DC blocking cap to a 74HCU04 (U19) configured as an amplifier to insure its levels exceed the threshold of the CS8412 receiver. BAV99 diodes provide overvoltage protection for the 74HCU04.

The AES/EBU input is terminated by a 1:1 transformer and an 110Ω resistor. The input signal goes to a 75ALS180 differential receiver (U14) which features a TTL-compatible output.

A 74HC4053 multiplexer (U16) selects the appropriate digital audio input. When AES_INSEL is high, the AES/EBU input is chosen; when low, S/PDIF is selected. The output of the mux is AC-coupled to the input of the CS8412 digital audio receiver (U15). Note that the meaning of the Channel Status bits decoded by the CS8412 change depending on whether the digital audio format is professional or consumer.

The CS8412 locks onto the frequency of the incoming S/PDIF signal with its internal PLL. R105 and C117 provide the time constant for the PLL Filter. C115, C116, and R104 provide power supply isolation and bypass capacitance for the CS8412's PLL circuitry and other analog circuitry. The output of the PLL, the MCK pin, sources the 256FS master clock. When external lock is selected by the 74HC253 Multiplexer (U23), this serves as a master clock for all digital audio clocking. This clock has 256 pulses per wordclock period.

The CS8412 has individual output pins for the more popular channel status bits. The function of Host Status Register 2 bits 5:0 is determined by DIOCSSEL (Control Register 2 bit 5). If DIOCSSEL is high, Status Register 2 bits 5:0 are channel status bits. When DIOCSSEL is high DIOCSSEL/ should be low clearing the output of the 74HC74 (U39) that sources the CS12 pin of the CS8412. This ensures that the channel status corresponds to sub-frame 1 (as opposed to sub-frame 2). If DIOCSSEL is low, those bits become Error Condition and Frequency Reporting bits. In either case, Status Register 2 bit 6 indicates an digital audio receiver error condition detected by the CS8412. This is outlined in the following table:

Host Status Bit	DIOCSSEL	Function		
STAT2<0>	0	E0	Error Condition bit 0	
STAT2<1>	0	E1	Error Condition bit 1	
STAT2<2>	0	E2	Error Condition bit 2	
STAT2<3>	0	F0	Frequency Reporting bit 0	
STAT2<4>	0	F1	Frequency Reporting bit 1	
STAT2<5>	0	F2	Frequency Reporting bit 2	
STAT2<6>	X	Error Flag		
STAT2<0>	1	C0/	Professional (low)	Consumer (high)
STAT2<1>	1	C1/	Non Audio	Non Audio
STAT2<2>	1	CB	EMO Emphasis	C2/ Copy Inhibit
STAT2<3>	1	CC	EM1 Emphasis	C3/ Emphasis
STAT2<4>	1	CD	C9/ Channel Mute	ORIG Original Copy
STAT2<5>	1	CE	CRCE/ CRC Error	IGCAT Ignorant Category

The Error Flag signal is gated by the Digital I/O Interrupt Mask (DIOIMSK/) with a 74HC08 AND gate (U45). The signal, after being buffered by a 74HC32 OR gate (U38), sources the V40's Non-Maskable Interrupt (HNMI). (The other input to U38 should always be low.) When DIOIMSK/ is high, ERF can trigger the V40's NMI. At that time, the type of error condition can be determined by reading the Error Decode bits. (When doing so, DIOCSSEL, Control Register 2 bit 5, must be set low.) When an error occurs, the corresponding error decode is latched. Since only one error can be indicated at any given time, there is a priority associated with each error code. Validity has the lowest priority while No-Lock has the highest priority. The error code is cleared by bringing the SEL pin of the CS8412 (U15) high for more than eight MCK cycles. From the V40's perspective, this is done by keeping DICSSEL high for 12 T-states or 3 instructions cycles. The following table describes the error conditions:

E2	E1	E0	Error	Comments
0	0	0	No Error	
0	0	1	Validity Bit High	Validity bit for a previous sample was high since the last clearing of the error codes
0	1	0	Confidence Flag	The received data eye opening is less than half a bit period, indicating a poor transmission link
0	1	1	Slipped Sample	A stereo sample has been dropped or re-read due to differences in internal vs. external sample rates
1	0	0	CRC Error (Pro only)	N/A
1	0	1	Parity Error	Incoming sub-frame does not have even parity as specified by digital audio interface standards
1	1	0	Biphase Coding Error	Biphase coding violation occurred
1	1	1	No Lock	PLL is not locked on incoming data stream. Lock is lost after not receiving 4 consecutive frame preambles

The frequency reporting bits are status bits from the CS8412 (U15) that indicate the sample rate of the incoming digital input. When digital input is selected, the system sample-rate should lock to the sample-rate of the incoming signal. In this case, one of three sample-rates is supported: 44.056kHz, 44.1kHz and 48kHz. (32kHz is accepted and will be locked to, but none of the DSP algorithms support it.) The frequency reporting bits' status is the result of a measurement by an internal circuit that uses a 6.144MHz clock as a reference. This reference is supplied by a 74HC74 (U39) that divides down the output of the 12.288 MHz crystal oscillator circuit. If all three frequency reporting bits are zero, it indicates that the incoming sample-rate is out-of-range. Note that the No-Lock condition, indicated by the Error Decoding bits, is a separate condition from being out-of-range. In either case, audio is muted. The CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition. To meet the Level 2 (Normal Accuracy Mode) specification, of the EIAJ CP-340 standard, only the 400 ppm tolerance is acceptable. Otherwise, the PCM 81 should be considered out-of-lock or going-out-of-lock. The decoding of the frequency reporting bits are summarized in the following table:

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz +4%
0	1	0	44.1kHz +4%
0	1	1	32kHz +-4%
1	0	0	48kHz +-400ppm
1	0	1	44.1kHz +-400ppm
1	1	0	44.056kHz +-400ppm
1	1	1	32kHz +-400ppm

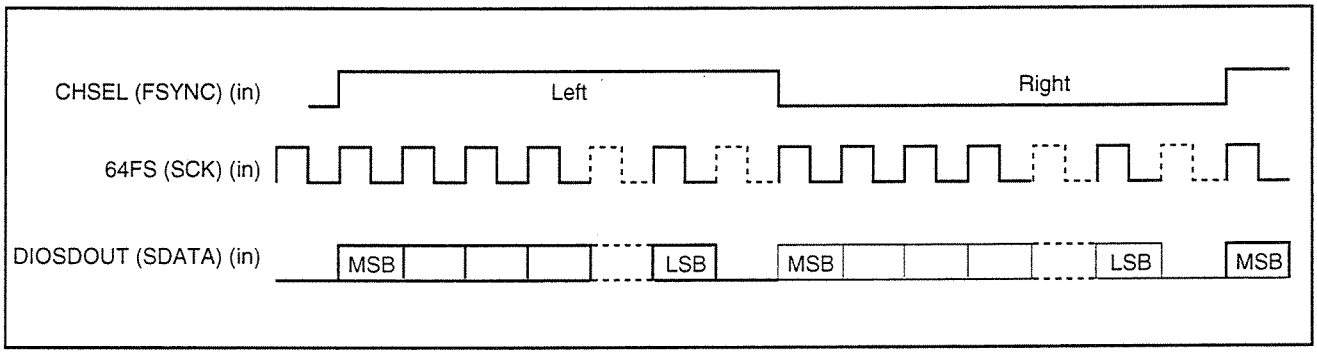
Digital Audio Transmitter

Two independent CS8402 digital audio transmitter ICs are used to implement the digital audio outputs. One CS8402 (U18) is wired for consumer format and dedicated to the S/PDIF output, while the other CS8402 (U17) is wired for professional format and dedicated to the AES/EBU output. The PCM81 cannot support the professional format on the S/PDIF output or the consumer format on the AES/EBU output.

For S/PDIF, the TXP output of U18 goes through a resistive voltage divider to provide a 1 volt peak-to-peak output waveform with a 75Ω output impedance per IEC 958 specifications. A 33pF capacitor is placed across the output to suppress RFI.

The TXP and TXN outputs of U17 are AC-coupled to a transformer per AES/EBU specifications. After the transformer, the output signal passes through a filter composed of 22Ω resistors and a 150pF capacitor. This filter suppresses RFI by limiting the rise and fall times of the signal while maintaining the required 110Ω output impedance.

Both CS8402s are hard-wired for the identical serial audio input format as shown:



CS8402 Audio Serial Port Format

Each CS8402 outputs the appropriate Channel Status for the professional (U17) and consumer (U18) digital audio formats. Most of the status bits are set in control register 2 as shown below:

Digital Audio Transmitter Control Bits

Host Control Bit	Function	
CTRL2<0>	FC0	Frequency Control bit 0
CTRL2<1>	FC1	Frequency Control bit 1
CTRL2<2>	CS2/	Copy Inhibit Out (asserted low)
CTRL2<3>	CS3/	Emphasis Out (asserted low)
CTRL2<4>	C15	Generation Status (asserted low)

The professional Emphasis Status bits (AES_EM0, AES_EM1) are set by gating CA[16:17] from control register 3 with LEDSEN. The CS8402 uses AES_EM0 and AES_EM1 to encode the professional channel status bits C2, C3, and C4. Their encoding and definition is shown in the following table.

Professional Emphasis Encoding

AES_EM1	AES_EM0	C2	C3	C4	Function
0	0	1	1	1	CCITT J.17
0	1	1	1	0	50/15 us
1	0	1	0	0	No emphasis
1	1	0	0	0	Not indicated

Frequency control bits FC0 and FC1 specify the sample rate channel status for both consumer and professional formats. Some glue logic (U38, U44) is required to interface FC0 and FC1 with the professional audio transmitter. The following table outlines the function of the frequency control bits.

Sample Frequency Encoding

FC1	FC0	C24 (cons)	C25 (cons)	Function	C6 (pro)	C7 (pro)
0	0	0	0	44.1 kHz	1	0
0	1	0	1	48 kHz	0	1
1	0	1	1	32 kHz*	1	1
1	1	0	0	44.1k-CD/48k* (consumer/pro)	0	1

*Not supported

CS8402 is reset by the host control bit DIORST/. This signal is asserted low on power-up and, therefore, will not pass through audio until the host releases this signal after DSP code is loaded. In that case, the CS8402's internal transmit timing counters are not enabled until eight and one-half 64FS clocks after the first active edge of FSYNC after DIORST/ is released. On a power-fail condition (which happens on power-down and brown-out conditions), DIORST/ should be asserted. When DIORST/ is asserted, the differential line drivers of the CS8402 are set to ground. Though this cuts off the digital output mid-stream, it should not send speaker-damaging signals to the box receiving the PCM 81's digital output. It is up to the receiving box to handle a lost digital input gracefully. (In the PCM 81, the CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition.)

Analog Circuitry

Analog Inputs

Two combination XLR with 1/4" tip/ring/sleeve phone jacks (J1,2) are provided for balanced or unbalanced sources. Balanced sources should be connected so the hot (+) side goes to pin 2 of the XLR connector or the tip of the phone plug. Unbalanced signals may be applied to either pin 2 (tip) or pin 3 (ring). 150pF ceramic caps and ferrite beads are included for RFI suppression.

Input Amplifier

Three op amp stages (U1-3) are configured as an instrumentation amplifier for each analog input. A 2-pole double-throw switch (SW1), located on the rear panel, changes the input gain from 0dB to 20dB. 4.99kΩ, 0.1% resistors are used to insure a minimum common mode rejection ratio of 54dB. Nonpolar 10uF capacitors block any DC bias on the incoming signals from affecting the performance of the input stage while the 49.9 kΩ resistors provide 100kΩ input impedance. Overvoltage protection for the op amp is provided by the series 100Ω resistors and BAV99 diodes.

The outputs of the input amplifiers go through another set of DC blocking caps before going to the input level pot (R201) on a separate PC board. The caps serve to prevent any DC offset due to the op amps' bias currents from affecting the quietness of the level pot or introducing bias in the A/D conversion.

A/D Conversion

After the input level pot, the left and right signals return to the main board and pass through 220Ω resistors in series with the non-inverting inputs of a dual op amp (U13). These resistors protect the inputs of the op amp from high-level signals. This op amp has a gain of 10.8dB and drives the hot (+) side of the A/D converter and an inverting stage (U12) through a DC blocking capacitor. The dual op amp (U12) not only inverts the signals for the cold (-) side of the A/D converter, but also provides a 2.5 volt bias for the differential signal. The bias voltage is created by a voltage divider (R85,87) which is applied to the non-inverting inputs of the inverter. The bias voltage appears at the (+) side of the A/D as well. 200kΩ resistors to ground (R261,262) reduce the bias voltage slightly on the (+) side in order to maximize performance of the A/D converter. The signals pass through a one-pole low pass filter before the A/D input which limits aliasing during conversion. Both op amps operate off ±5 volt rails to insure signal levels do not exceed the maximum specified for the converter.

Conversion is performed by a stereo monolithic 24-bit Delta-Sigma AK5391 A/D converter (U10). This device uses a dual-bit sampler operating at 128x the sample rate and a noise shaping filter. This filter pushes the granularity noise beyond the audio spectrum. A digital decimation filter removes this high frequency noise and reduces the word rate to 24 bits. A differential architecture on the converter's front-end improves noise rejection. The AK5391 has independent power supply pins for the analog and digital sections. The digital side runs off +5VD which is filtered through a ferrite bead and 10uF tantalum cap in parallel with a 0.1uF ceramic cap. The analog section is powered by the separately regulated +5VA and includes 10uF tantalum and 0.1uF ceramic bypass capacitors.

The AK5391's serial data interface operates in slave mode and requires a master clock (256FSA), bit clock (64FSA), and left/right framing signal (WCA/). Serial data (AIOSDIN) is MSB first and left-justified within the frame. Sample rates of 44.1 and 48kHz are supported in the PCM 81. An active low, calibration signal (ADCAL/) is asserted during power up and whenever the sample rate is changed. This initializes the converter's offset calibration cycle. Data from the converter is discarded for the first 200ms after ADCAL/ goes high due to the calibration process.

D/A Conversion

The CS4390 D/A converter (U8) is a Delta-Sigma (single-bit) type operating at 128x oversampling with 24-bit resolution. The CS4390 includes a switched-capacitor analog low pass filter located before the analog outputs. This type of filter reduces the effect of jitter on the incoming data from increasing THD at the analog outputs. The CS4390 requires +5 volts for both analog and digital supplies. +5VD is filtered through a ferrite bead and 10uF tantalum capacitor with a 0.1uF ceramic cap for the digital supply; this voltage passes through a 5.1Ω resistor with separate tantalum and ceramic bypass capacitors for the analog supply.

The CS4390's serial data interface operates in slave mode and requires a master clock (256FSA), bit clock (64FSA) and framing signal (WCA/). Serial data (DIOSDOUT) is MSB first and left-justified within the frame. The CS4390 will mute its analog outputs whenever MUTE/ is asserted.

The CS4390 provides differential outputs for the analog signals which go into active 3-pole low pass filters (U6,7). Each filter has a Butterworth response to insure flatness in the passband, with a gain of 1.9dB and -3dB point at 37kHz. The filter topology includes two op amp stages. The first stage converts the differential signal into a single-ended one while incorporating the first two poles of the filter. The third pole is developed in the second stage. The outputs from the first stage pass through 47uF capacitors in order to remove the 2.2 volt DC bias from the D/A converter's outputs.

Output Level Switching

Two J108 FETs (Q1,2) provide the ability to attenuate the output signals by 14dB by controlling the gain of an inverting op amp (U7). The FETs act like switches which change the input impedance to the inverter, thereby changing the gain. The gain is +10.3dB when the FETs are turned on, -3.7dB when the FETs are off.

The FETs are controlled by a 2N3906 transistor (Q3). When HIOUTLVL is high, Q16 turns off. A negative voltage is applied to the gates of the FETs, which turns them off. In this case the input resistance to the inverting stage is 11.8kΩ. With HIOUTLVL low, Q16 turns on. A small positive voltage is applied to each gate by the voltage divider, R61 and R62, thereby turning the FETs on. This action changes the input impedance by placing the 2.94kΩ and 11.8kΩ resistors in parallel, reducing the input resistance to approximately 2.36kΩ.

Balanced Output Amplifiers

Two dual op amps are employed as output amplifiers (U4,5). The circuit topology provides unity gain whether the outputs are driving balanced or single-ended loads. 4.99kΩ resistors with a 0.1% tolerance are used to insure the output levels are matched. 220 uF non-polar capacitors eliminate DC offsets from the outputs while BAV99 diodes and series 51Ω resistors provide overvoltage and short circuit protection.

Analog Outputs

Output connectors include two XLR (J3,7) and two 1/4" tip/ring/sleeve phone jacks (J5,6). Balanced outputs should be connected so the hot (+) side goes to pin 2 of the XLR connector or the tip of the phone plug. Unbalanced loads may be accommodated by grounding the unused pin [either pin 2 (tip) or pin 3 (ring)]. Ferrite beads and 100pF capacitors are included for RFI suppression.

Output muting is accomplished by miniature relays (RY1,2) controlled by MUTE. When MUTE/ is low, Q4 turns off, breaking the current path to the relay coils, thereby shorting the analog outputs to ground. Likewise, when MUTE/ is high, Q1 turns on, activating the relays and connecting the stereo output signals to the output jacks.

Power Supply

A universal input switching power supply produces the voltages required by the PCM 81 circuits. It operates over an input voltage range of 90-264 VAC at 50 or 60Hz. The supply is capable of producing +5 VDC @ 3 Amps, +15 VDC @ 2 Amps and -15 VDC @ 0.35 Amps. The +5 Volt supply is used for all of the digital circuitry, while the ±15 Volt supplies are required for the analog circuitry.

The AC voltage is terminated by a 2-pin connector located towards the rear of the unit. A 6-pin connector at the opposite end of the supply accommodates the DC output voltages and returns. A cable assembly with a ferrite sleeve brings the supply voltages over to the main board. +5 Volt and digital ground connections to the main board are made near the power supply, while the ±15 Volt and analog ground terminate near the analog I/O jacks.

The power supply is not field serviceable. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair. A 3.15 Amp fast-acting fuse is incorporated on the supply module's AC input side. Always replace with a fuse of identical rating.

The ±15 Volt rails pass through a π filter to reduce high frequency noise before they are distributed to any analog circuitry. After this filter, the ±15VA rails go two voltage regulators. These regulators (U9,11) are used to produce ±5VA for the op amps that drive the A/D converter's analog inputs as well as the +5 volt analog supply required by the A/D converter.

The +5 Volt supply passes through low and high frequency bypass capacitors (C177-179) upon entering the main board. +5VD is distributed to the appropriate circuitry after passing through these capacitors.

Signal Names

16FS	Digital Audio Clock (16x Wordclock).
64FS, 64FSD	Digital Audio Clock (64x Wordclock)
64FSA	Analog Clock (64x Wordclock)
128FS	Digital Audio Clock (128x Wordclock)
256FS	Digital Audio Clock (256x Wordclock)
256FSA	Analog Clock (256x Wordclock)
56KINT	Interrupt from DSP56002
56KOVRL/	DSP56002 Interrupt from DSP to host
56KRST/	DSP56002 Reset Line
-15VA	-15 Volts Analog
-5VA	-5 Volts Analog
+5VA	+5 Volts Analog
+5VD	+5 Volts Digital
+15VA	+15 Volts Analog
ADCAL/	ADC Calibration Enable
ADCDONE/	Footpedal ADC Conversion Done Signal
ADCEN/	Foot Controller ADC Enable
AES_INSEL	Digital Audio input Select (1=AES,0=S/PDIF)
AES_EM<1:0>	AES Digital Output Emphasis Status Bits
AIOFRAME	Analog I/O Framing Signal
AIOSDIN	Analog I/O Serial Data Input
ASNA	Adjust Soft Knob A
ASNB	Adjust Soft Knob B
BATLOW	Battery Low Signal
BVD<2:1>	PCMCIA Battery Voltage Status
CA<19:0>	PCMCIA Card Address
CARDET/	Card Detection
CARDEN/	PCMCIA Card Slot Enable
CARDENB/	Buffered Card Enable
CD<7:0>	PCMCIA Card Data
CDET1/	PCMCIA Card Detect 1
CDET2/	PCMCIA Card Detect 2
CCE1/	PCMCIA Card Enable 1
CCE2/	PCMCIA Card Enable 2
CLOVRL/	Clear Lexichip Overload Line
COE/	PCMCIA Card Output Enable
CSHINT/	Clear Slave-to-Host Interrupt
CTRL3..0WR/	Control Register 3 thru 0 Write Enable
CVCC	PCMCIA Card Vcc
CWE/	PCMCIA Card Write Enable
CWP	PCMCIA Card Write Protect
CWRPROT	PCMCIA Card Write Protect
DIOCSSEL/	Digital I/O Channel Status Select
DIOIMSK/	Digital I/O Interrupt Mask
DIOINT	Digital I/O Interrupt
DIORST/	Digital I/O Reset
DIOSDIN	Digital I/O Serial Data Input
DIOSDOUT	Digital I/O Serial Data Output
DISCARD	Disable PCMCIA Card
DISPBSY	Display Busy
DISPD<7:0>	Display Data Bus
DISPDWR	Display Data Write
DISPDWR/	Display Data Write Enable
DISPTST/	Display Test Mode
DMEMOP/	DRAM Memory Operation
DSPHEN/	DSP Host Enable
ERF	Digital Input Error Flag
E0/C0/	Error/Channel Status Bit 0
E1/C1/	Error/Channel Status Bit 1
E2/C2/	Error/Channel Status Bit 2

FC<1:0>	Digital Output Sample Frequency Status Bits
FINTMSK/	DSP56002 Interrupt Mask
FOOTSWR	Footswitch Jack Ring Input
FOOTSWT	Footswitch Jack Tip Input
FPASNA	Front-Panel Adjust Soft Knob A
FPASNB	Front-Panel Adjust Soft Knob B
FPLOCK/	DSP56002 PLL Lock Status
FPSSNA	Front-Panel Select Soft Knob A
FPSSNB	Front-Panel Select Soft Knob B
FRCMOD	DSP56002 Force Mode Line
F0/C3/	Digital Input Frequency Reporting Bit 0 / Channel Status Bit 3
F1/ORG	Digital Input Frequency Reporting Bit 1 / Original Bit
F2/IGC	Digital Input Frequency Reporting Bit 2 / Ignorant Catagory
GTAIOSDIN	Gated AIOSDIN
HA<19:0>	Host Address Bus
HACK/	Host DMA Acknowledge
HAD<7:0>	Host Multiplexed Address/Data Lines
HASTB	Host Address Strobe
HASTBQ	Clock-Delayed version of HASTB
HBEN/	Host Bus Enable
HBR/W	Host Bus Read-Not Write
HBS<2:0>	Host Bus Status
HBSQ0	Clock-Delayed Host Bus Status 0
HBSQQ0	Double Clock-Delayed Host Bus Status 0
HBW/RQ	Clock Delayed version of Host Bus Write-Not Read
HCAS/	Host DRAM Column Address Strobe
HCLK	Host Clock
HD<7:0>	Host Data Bus
HDRA<9:0>	Host DRAM Address Lines
HIORD/	Host IO Read Enable
HIOUTLVL	High Output Level Enable
HIOWR/	Host IO Write Enable
HMRD/	Host Memory Read
HMRDQ/	Clock-Delayed version of HCB-HMRD/
HMRD2Q	Double Clock-Delayed version of HCB-HMRD
HMRD3Q	Triple Clock-Delayed Host Memory Read
HMRST	Host Master Reset Control Bit
HMWR/	Host Memory Write
HMWRB/	Host Memory Write Buffered
HRAS/	Host DRAM Row Address Strobe
HREFREQ/	Host Refresh Request
HREQ	Host DMA Request Line
HREQQ	Host DMA Request
HRLEDWR/	Headroom LEDs Write Enable
HROMEN/	Host ROM Enable
HWAIT/	Host Wait Enable
LARWR/	LEDs Row and Column / Switch Column Register Write Enable.
LED-6DB/	Headroom LED -6dB Row Line
LED-12DB/	Headroom LED -12dB Row Line
LED-18DB/	Headroom LED -18dB Row Line
LED-24DB/	Headroom LED -24dB Row Line
LEDOVRLD/	Headroom LED Overload Row Line
LEXRST/	Lexichip Reset
LHRCOL	Left Headroom Column Strobe
LEDROW<2:0>/	LED Row Lines
LEDSEN	LED Buffers Enable
LIN	Left Analog Audio Input (post level control)
LOGICHI	LogicHigh

LOUT	Left Analog Audio Output (from DAC)
LOVLDP/	Lexichip Overload Pulse
LWAITY/	Lexichip Wait Line
MAPINSRAM	Map In SRAM.
MIDIIN	MIDI Input Serial Data
MIDIINTHRU	Buffered MIDI Input for MIDI THRU
MIDIOUT	MIDI Output Serial Data
MIDITHOUT	MIDI Output for THRU Jack Testing
MIDITHRU	MIDI THRU
MRST/	Master Reset
MUTE/	Analog Output Mute
NVRAMEN	Non-Volatile RAM Enable
OUT_USER	Digital Output User Bits
OUTCS<15,3,2>	Output Channel Status Bits 15, 3 and 2
OUTVLD	Digital Output Validity Bit
PGDIOSDOUT	Pre-Gated DIOSDOUT
PREBCWE/	Pre-Buffered Version of Card Write Enable
PRGINT<7:5>	Programmable Interrupts 7 thru 5
PWR_OK	Power OK
RHRCOL	Right Headroom Column Strobe
RIN	Right Analog Audio Input (post level control)
ROUT	Right Analog Audio Output (from DAC)
ROWRD/	LEDs Row Read Enable
SBUSEN/	Slave Bus Enable
SELCA	Select DRAM Column Address Enable
SHINT	Slave-to-Host Interrupt
SHSINT/	Set Slave-to-Host Interrupt
SLVRST/	Slave Reset
SRSSEL<1:0>	Wordclock Source Select Lines
SSNA	Select Soft Knob A
SSNB	Select Soft Knob B
STAT2..0RD/	Status Register Read Enable 2 thru 0
SWCOL<2:0>	Switch Column Strobe Bits
SWROW<3:0>	Switch Row 3 thru 0
TACOSWAP	Tacochip Swap Signal
VRAM	Non-Volatile SRAM Power
VREFADC	Footpedal ADC Voltage Reference
WC/	Word Clock
WCA/	Analog Wordclock
WDKICK/	Watchdog Timer Kick

Parts List

POWER CORDS

PART NO.	DESCRIPTION	QTY	REFERENCE
680-09149	CORD,POWER,NA/IEC,SVT,VW-1,10A	1	N.AMER
680-08830	CORD,POWER,IEC,6A,2M,EURO	1	
680-10093	CORD,POWER,IEC,5A,2M,UK	1	
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1	
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1	
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1	
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1	
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1	

SHIPPING MAT'LS

PART NO.	DESCRIPTION	QTY	REFERENCE
541-00781	BUMPER,FEET,3-M #SJ5018	4	
730-11361	BOX,21.5X5.38X20,BLANK	1	OUTER BOX
730-11364	INSERT,FOAM,ENDCAP,1UX9&12	2	
730-11444	INSERT,CORR,ACC,21X4.5	1	POWER CORD
730-11459	BOX,21X5X19,LEXICON	1	INNER BOX

MECH/CHASSIS

PART NO.	DESCRIPTION	QTY	REFERENCE
430-09785	DISPLAY,VF,20X2 CHAR,5X7DOT	1	
510-09985	CONN,MEM CARD,68 PIN,EJECTOR	1	HOST BD (J23)
530-02488	TIE,CABLE,NYL,.14"X5 5/8"	1	PS TO HOST CABLE
530-09382	CLIP,WIRE HRNS,.15DIA,ADH BAK	2	PS TO HOST CABLE
530-09979	CLAMP,CABLE,.169",ZN	1	AC INPUT CABLE
550-03827	BUTTON,.346RD,BLK	1	PWR SW
550-09087	KNOB,15MM,6MM/FLAT,BLK	1	LVL POT
550-09759	BUTTON,.20X.50,BLK	3	
550-09760	BUTTON,.20X.50,BLK,W/LENS	9	
550-09767	KNOB,21MM,6MM/FL,BLK/BLK	2	ENCODERS
550-12351	CAP,SW,7.5MMRDX22.5MML,BLK	1	LVL SW
630-02737	WSHR,FL,#8CLX.02TH,BLK,NYL	4	FP TO CHASSIS
630-03669	SPCR,#4CLX3/8,3/16RD,NYL	2	PWR SW SUPPORT
630-09709	SPCR,PCB/FOOT,.188,NYL	1	HOST BD
640-01706	SCRW,4-40X3/8,PNH,PH,ZN	4	FP SW BD TO INSERT(2); AC CONN TO CHASSIS(2)
640-02034	SCRW,4-40X5/8,PNH,PH,ZN	2	MEMCD TO HOST BD
640-02736	SCRW,8-32X3/8,BH,SCKT,BLK	4	FP TO CHASSIS
640-03957	SCRW,6-32X3/16,TH,PH,BLK	16	COVERS TO CHASSIS AND INSERT
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	6	DSP TO HOST BD (4); HDRM BD TO INSERT (2)
640-07696	SCRW,M3X8MM,PH,PNH,ZN	2	DSPLY TO INSERT
640-09758	SCRW,M3X16MM,PH,FH,ZN	2	PWR SW TO CHASSIS

PART NO.	DESCRIPTION	QTY	REFERENCE
640-09987	SCRW,6-32X5/16,PNH,PH,SEMS,ZN	14	PS TO CHASSIS&BRKT (4); HOST BD TO CHASSIS, INSERT & PS BRKT (9); AC CLAMP TO CHASSIS (1)
640-11284	SCRW,M3X8MM,FH,PH,BZ	4	J1,2 (Use 641-11466 w/ 510-13799)
641-09699	SCRW,TAP,AB,#2X5/16,PNH,PH,ZN	3	MIDI CONN TO CHASSIS
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	13	J3,7,10,11 (12) (Use J1,2 w/ 510-13799) RCA CONN TO CHASSIS (1)
643-01728	NUT,6-32,KEP,ZN	2	CHASSIS GND (1); AC CABLE CLAMP (1)
643-01732	NUT,4-40,KEP,ZN	6	AC CONN TO CHASSIS (2); FP TO INSERT (2); MEMCD CONN TO HOST (2)
644-01735	WSHR,FL,#6CLX3/8ODX1/32THK	1	CHASSIS GND
644-07893	WSHR,FL,.427IDX.550X.035THK,ZN	2	FP ENCODER TO INSERT
650-05899	POPRVT,5/32X1/4,REG PROT HD,AL	3	PS BRKT TO CHASSIS
680-11709	CABLE,AC PWR,SHLD,14",P1=N	1	AC CONN TO PWR SUP AND PWR SWITCH
700-09856	CHASSIS,INSERT,FP,PCM-80	1	
700-09859	BRACKET,PWR SUP,PCM-80	1	
700-12646	CHASSIS,WRAP,PCM81/91	1	
700-12647	COVER,TOP/BOTTOM,PCM81/91	2	
701-09860	BRACKET,POT,SHIELD,PCM-80	1	INPUT LVL POT
702-09858	COVER,PROTECTIVE,TOP,PS,PCM-80	1	
702-09861	COVER,PROTECTIVE,BOT,PS,PCM-80	1	
702-12640	PANEL,FRONT,PCM81	1	
703-09862	LENS,DISPLAY,PCM-80	1	
703-12644	PANEL,OVLY,REAR,PCM81/91	1	
710-10190	PC BD,MEMCD CVR,PCM80&1/90&1	1	
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1	CHASSIS GND
740-08558	LABEL,TUV CERTIFIED,BAYERN	1	TOP COVER
740-11482	LABEL,WARN/APP,FCC/C-UL/CE,PRO	1	TOP COVER
740-12629	LABEL,PRODUCT ID,PCM81	1	TOP COVER
750-11396	PWR SUP,+5V@3A,+/-15V,40W	1	

HOST BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	10	R114,117,119,204,235, 237,257-260
202-09871	RESSM,RO,5%,1/10W,1K OHM	23	R95,105,132,150,154,158-160,169, R171,185,203,205,209,230,234 R236,248-253
202-09873	RESSM,RO,5%,1/10W,10K OHM	52	R25,26,38,39,63,131,140-142,153,155 R167,186-202,207,208,210-223,232, R233,243-247
202-09894	RESSM,RO,5%,1/10W,1M OHM	3	R52,65,143
202-09899	RESSM,RO,5%,1/10W,47 OHM	21	R76,125,130,135,136,139,144-149, R156,157,161-166,172
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	8	R62,183,224-229
202-10558	RESSM,RO,5%,1/10W,47K OHM	3	R99,101,113
202-10559	RESSM,RO,5%,1/10W,100 OHM	10	R173-182
202-10569	RESSM,RO,5%,1/10W,10 OHM	5	R104,129,133,134,151
202-10570	RESSM,RO,5%,1/10W,120 OHM	2	R100,102
202-10571	RESSM,RO,5%,1/10W,100K OHM	1	R97
202-10572	RESSM,RO,5%,1/10W,200K OHM	2	R261,262

PART NO.	DESCRIPTION	QTY	REFERENCE
202-10573	RESSM,RO,5%,1/10W,470K OHM	2	R168,170
202-10574	RESSM,RO,5%,1/10W,10M OHM	2	R123,127
202-10585	RESSM,RO,5%,1/4W,51 OHM	8	R27,28,40,41,77,79,82,84
202-10586	RESSM,RO,5%,1/4W,100 OHM	4	R1,2,9,10
202-10835	RESSM,RO,5%,1/4W,470 OHM	2	R124,128
202-10889	RESSM,RO,5%,1/10W,75 OHM	2	R137,138
202-10891	RESSM,RO,5%,1/10W,270 OHM	5	R238-242
202-10943	RESSM,RO,5%,1/10W,22K OHM	1	R206
202-10948	RESSM,RO,5%,1/10W,390 OHM	1	R231
202-11071	RESSM,RO,5%,1/4W,75 OHM	1	R112
202-11072	RESSM,RO,5%,1/4W,220 0HM	8	R92,93,98,115,116,118,120,121
202-11683	RESSM,RO,5%,1/10W,5.1 OHM	1	R75
202-12365	RESSM,RO,5%,1/4W,110 OHM	1	R103
202-12366	RESSM,RO,5%,1/4W,22 OHM	4	R106-109
202-12368	RESSM,RO,5%,1/4W,120 OHM	6	R94,96,122,254-256
202-12369	RESSM,RO,5%,1/10W,36K OHM	4	R61,64,152,184
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	2	R85,87
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	4	R55,56,69,70
203-11727	RESSM,RO,1%,1/10W,562 OHM	4	R3,8,11,13
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	4	R57,59,71,73
203-12167	RESSM,RO,1%,1/10W,374 OHM	1	R110
203-12363	RESSM,RO,1%,1/10W,90.9 OHM	1	R111
203-12372	RESSM,THIN,1%,1/10W,4.99K OHM	2	R89,91
203-12373	RESSM,THIN,1%,1/10W,7.68K OHM	2	R54,68
203-12374	RESSM,THIN,1%,1/10W,8.06K OHM	4	R58,60,72,74
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	6	R78,80,81,83,88,90
203-12720	RESSM,THIN,1%,1/10W,2.94K OHM	2	R51,66
203-12721	RESSM,THIN,1%,1/10W,11.8K OHM	2	R53,67
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	4	R5,7,14,16
203-12723	RESSM,THIN,1%,1/10W,102 OHM	2	R34,47
203-12724	RESSM,THIN,.1%,1/10W,4.99K OHM	28	R4,6,12,15,17-24,29-33,35-37, R42-46,48-50
240-00613	CAP,ELEC,22uF,25V,RAD	1	C182
240-00614	CAP,ELEC,47uF,16V,RAD	4	C39,48,84,87
240-06096	CAP,ELEC,10uF,25V,RAD,NON-POL	6	C3,4,11,12,92,93
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	5	C100,103,108,177,208
240-12725	CAP,ELEC,220uF,25V,NONPOL,20%	4	C23,24,31,32
241-09366	CAPSM,TANT,10uF,25V,20%	4	C25,30,33,38
241-09798	CAPSM,TANT,10uF,10V,20%	14	C57,59-61,63,68,70-72,75,86,115 C159,160
244-00662	CAP,MYL,.1uF,5%,RAD	1	C196
244-04960	CAP,MYL,1uF,5%,RAD	2	C195,206
244-06173	CAP,MYL,4700pF,5%,RAD	4	C45,46,54,55
244-06176	CAP,MYL,.047uF,5%,RAD	1	C117
244-06177	CAP,MYL,.33uF,10%,RAD	2	C172,173
244-10423	CAP,MYL,.22UF,10,RAD	5	C95,97,98,101,178
245-09291	CAPSM,CER,470pF,50V,NPO,5%	2	C109,110
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	97	C5,8,13,16,17,22,26,29,34,37,41,42 C47,50,51,56,58,62,64-67,69,73,74 C76-78,83,85,88,91,113,114,116,119 C122-126,130,131,136-138,141, C144-152,155-157,161-171,174-176, C180,181,183-194,197-205,207
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	4	C118,120,128,158
245-10561	CAPSM,CER,100pF,50V,COG,5%	12	C80,81,89,90,104-107,132-135
245-10562	CAPSM,CER,150pF,50V,10%	12	C1,2,9,10,94,96,99,102,111,112, C121,179

PART NO.	DESCRIPTION	QTY	REFERENCE
245-10588	CAPSM,CER,33pF,50V,COG,10%	5	C127,139,140,142,143
245-10977	CAPSM,CER,330pF,50V,NPO,5%	4	C43,44,52,53
245-11591	CAPSM,CER,560pF,50V,COG,5%	2	C40,49
245-11594	CAPSM,CER,2200pF,50V,COG,5%	2	C79,82
245-11625	CAPSM,CER,33pF,50V,COG,5%	13	C6,7,14,15,18-21,27,28,35,36,129
245-12070	CAPSM,CER,15pF,50V,COG,10%	2	C153,154
270-00779	FERRITE,BEAD	18	FB1-6,9-20
270-06671	FERRITE CHOKE,2.5 TURN	2	FB7,8
300-01030	DIODE,1N4004 AND 4005	5	D9-13
300-10509	DIODESM,1N914,SOT23	1	D18
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	12	D1-8,14-17
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	1	D19
310-10422	TRANSISTORSM,2N4403,SOT23	7	Q9-15
310-10510	TRANSISTORSM,2N3904,SOT23	5	Q4-8
310-10565	TRANSISTORSM,2N3906,SOT23	1	Q3
310-12196	TRANSISTORSM,J108,N-CH,SOT23	2	Q1,2
330-04572	IC,DIGITAL,74HCT245	1	U70
330-04674	IC,DIGITAL,74HC4538	1	U48
330-05901	IC,DIGITAL,74HC253	1	U23
330-09239	ICSM,DIGITAL,74HC74,SOIC	2	U20,39
330-09796	ICSM,DIGITAL,74AC00,SOIC	2	U42,61
330-09845	ICSM,DIGITAL,74AC174,SOIC	1	U47
330-09877	ICSM,DIGITAL,74HC174,SOIC	1	U46
330-09884	ICSM,DIGITAL,74AC32,SOIC	1	U72
330-09885	ICSM,DIGITAL,74AC74,SOIC	1	U27
330-09891	ICSM,DIGITAL,74AC157,SOIC	3	U56-58
330-10372	ICSM,DIGITAL,74HC574,SOIC	2	U65,68
330-10522	ICSM,DIGITAL,74HC04,SOIC	1	U44
330-10523	ICSM,DIGITAL,74HCU04,SOIC	3	U19,21,22
330-10524	ICSM,DIGITAL,74HC08,SOIC	3	U43,45,52
330-10525	ICSM,DIGITAL,74HC14,SOIC	1	U25
330-10526	ICSM,DIGITAL,74HC32,SOIC	1	U38
330-10527	ICSM,DIGITAL,74HC138,SOIC	2	U62,63
330-10532	ICSM,DIGITAL,74HC175,SOIC	1	U26
330-10533	ICSM,DIGITAL,74HC245,SOIC	1	U35
330-10536	ICSM,DIGITAL,74HC273,SOIC	4	U31,32,49,69
330-10537	ICSM,DIGITAL,74HC541,SOIC	7	U30,33,59,60,67,71,73
330-10589	ICSM,DIGITAL,74HC161,SOIC	2	U28,29
330-12069	ICSM,DIGITAL,74HC573,SOIC	3	U36,41,66
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	7	U1-3,6,7,12,13
340-10567	ICSM,LIN,MC34164,+5V MON,SOIC	1	U53
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	1	U64
340-11575	ICSM,LIN,7805,+5V REG,TO263	1	U11
340-11576	ICSM,LIN,7905,-5V REG,TO263	1	U9
340-12367	ICSM,LIN,OP275,DU OP AMP,SOIC	2	U4,5
345-12038	ICSM,INTER,75ALS180,DR/RC,SOIC	1	U14
345-12059	ICSM,INTER,CS8402A,XMTR,SOIC	2	U17,18
345-12060	ICSM,INTER,CS8412,RCVR,SOIC	1	U15
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	1	U16
350-04710	IC,SRAM,43256,150NS,LPS	1	U54
350-09749	IC,GAL,20V8,PCM-80,HOST,V1.00	1	U40
350-10374	ICSM,DRAM,256KX4,80NS,SOJ	2	U50,51
350-12630	IC,ROM,27C040,PCM81,V1.00	1	U55
355-04283	IC,CONV,ADC0804	1	U37
355-12333	ICSM,DAC,CS4390,24BIT,STR,SSOP	1	U8
355-12349	ICSM,ADC,AKM5391,24BIT,STR,SOP	1	U10

PART NO.	DESCRIPTION	QTY	REFERENCE
365-09774	ICSM,uPROC,uPD70208(V40),8MHz	1	U34
375-02247	IC,OPTO-ISOLATOR,6N138	1	U24
390-12144	CRYSTALSM,16.000MHz,PAR,18pF	1	Y3
390-12361	CRYSTALSM,11.2896MHz,PAR,HC49	1	Y2
390-12362	CRYSTALSM,12.288MHz,PAR,HC49	1	Y1
410-03584	RELAY,2P2T,LOW LEVEL,DIP,12V	2	RY1,2
453-03993	SW,PBPP,2P2T,PCRA,2.5MM TRAV	1	SW1
460-04598	BATTERY,LITH,3V,FLAT	1	BAT1
470-07652	XFORMER,PULSE,AES,1:1	2	TX1,2
490-02356	CONN,JUMPER,.1X025,2FCG	5	W1-3; W4 PINS 1 & 2; W7 PINS 2 & 3
510-02899	CONN,POST,100X025,HDR,3MC	2	W4,7
510-03961	CONN,POST,100X025,HDR,2MCG	3	W1-3
510-06568	CONN,POST,079,HDR,6MC	1	J21
510-07785	CONN,RCA,PCRA,1FCGX2,VERT	1	J12
510-09765	CONN,POST,079,HDR,10MC	1	J22
510-09773	CONN,MEM CARD,PC,68PIN,CONTACT	1	J23
510-09783	CONN,POST,100X025,36X2MCG,ELEV	1	J16
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	3	J13-15
510-10880	CONN,XLR/JACK,3FC,1/4"TRS,PCRA	2	J1,2 (Replacement part: 510-13799; use screw: 641-11466)
510-10881	CONN,XLR,3MC,PCRA,PLASTIC CMPT	3	J3,7,11
510-10884	CONN,JMP,.6X2.5mm,7FC,TRAP	2	J18,19
510-11086	CONN,XLR,3FC,PCRA,LATCH,SMALL	1	J10
510-12636	1/4"PH JACK,PCRA,3C,SW-TR,G,NR	4	J5,6,8,9
520-04425	IC SCKT,24 PINX.3",PC,LO-PRO	1	U40
520-09736	IC,SCKT,32 PIN,PC,TIN,LO-PRO	2	U54,55
620-10413	LUG,#4,INT STAR,RCA GND	1	J12
635-09770	SPCR,SWAGE,4-40X7/8,1/4RD,BR	4	HOST TO DSP BD
680-09757	CABLE,XITION/SCKT,20C,6"	1	DISPLAY TO HOST-J20
680-12718	CABLE,HSG/ST&T,6C,26/8.5,SLV	1	PWR SPLY TO HOST-J4,17
710-12620	PC BD,HOST,PCM81/91	1	

DSP BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-09794	RESSM,RO,5%,1/10W,0 OHM	1	R5
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	5	R62-66
202-09871	RESSM,RO,5%,1/10W,1K OHM	1	R2
202-09873	RESSM,RO,5%,1/10W,10K OHM	6	R1,57,59,60,71,75
202-09894	RESSM,RO,5%,1/10W,1M OHM	1	R51
202-09897	RESSM,RO,5%,1/10W,470 0HM	23	R3,4,6-9,16,21,40,45,53-56,58,68-70 R74,78,84,86,88
202-09899	RESSM,RO,5%,1/10W,47 OHM	52	R10-15,17-20,22-26,28-39,41-44,46-50 R52,61,67,72,73,76,77,79-83,85,87,89, R90
202-10890	RESSM,RO,5%,1/10W,220 OHM	1	R27
241-09798	CAPSM,TANT,10uF,10V,20%	5	C1,8,14-16
245-09869	CAPSM,CER,.001uF,50V,Z5U,20%	28	C5,6,9,10,12,17,18,21,22,26,28,30,32 C34,35,37,38,43,45,49,51,52,54,56 C63-65,68
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	1	C13
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	34	C2-4,7,11,19,20,23-25,27,29,31,33 C36,39,42,44,46,48,50,53,55,57-62 C66,67,69-71

PART NO.	DESCRIPTION	QTY	REFERENCE
245-09895	CAPSM,CER,10pF,50V,COG,10%	2	C40,41
245-09896	CAPSM,CER,2200pF,50V,X7R,20%	1	C47
270-09799	FERRITESM,CHIP,600 OHM,1206	1	FB1
330-09350	IC,DIGITAL,LEXICHIP 2	1	U22
330-09351	IC,DIGITAL,TACOCHIP	1	U10
330-09796	ICSM,DIGITAL,74AC00,SOIC	1	U23
330-09797	ICSM,DIGITAL,74AC04,SOIC	1	U18
330-09845	ICSM,DIGITAL,74AC174,SOIC	1	U28
330-09877	ICSM,DIGITAL,74HC174,SOIC	2	U29,34
330-09884	ICSM,DIGITAL,74AC32,SOIC	1	U21
330-09885	ICSM,DIGITAL,74AC74,SOIC	1	U20
330-09886	ICSM,DIGITAL,74HC373,SOIC	1	U24
330-09887	ICSM,DIGITAL,74HCT374,SOIC	3	U1,8,12
330-09888	ICSM,DIGITAL,74ACT153,SOIC	4	U5,7,11,13
330-09889	ICSM,DIGITAL,74ACT04,SOIC	1	U19
330-09890	ICSM,DIGITAL,74AC541,SOIC	1	U30
330-09891	ICSM,DIGITAL,74AC157,SOIC	4	U26,32,37,38
330-09893	ICSM,DIGITAL,74ACT157,SOIC	1	U9
350-09745	ICSM,GAL,16V8,PCM-80,LEX,V1.00	1	U33
350-09746	ICSM,GAL,16V8,PCM-80,56K,V1.00	1	U14
350-09747	ICSM,GAL,16V8,PCM-80,SLV1,V1.0	1	U31
350-09748	ICSM,GAL,16V8,PCM-80,SLV2,V1.0	1	U25
350-10373	ICSM,DRAM,256KX16,80NS,SOJ	1	U17
350-10374	ICSM,DRAM,256KX4,80NS,SOJ	1	U16
350-11238	ICSM,SRAM,8KX8,25NS,SOJ	1	U35
350-12384	ICSM,DRAM,1MX4,60NS,SOJ	2	U2,3
350-12637	ICSM,DRAM,1MX16,70NS,SOJ	1	U4
365-09870	ICSM,uPROC,56002,DSP,QFP	1	U15
365-09883	ICSM,uPROC,Z80,CMOS,10MHz,QFP	1	U36
390-09791	CRYSTAL,25.8MHz	1	Y1
510-09784	CONN,POST,100X025,36X2FCG,TEMP	1	J2
710-12740	PC BD,DSP,PCM81	1	

POT BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
200-09761	POT,RTY,PC,10KAX2,6MMFL,16,20L	1	R201
680-10885	CABLE,RIB,24-26G,7CX.1,1.5",NW	1	J104
710-09813	PC BD,POT,PCM80&1/90&1	1	

HEADROOM BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
430-03896	LED,GRN,RECT,.197X.079	6	D103-105,108-110
430-03897	LED,YEL,RECT,.197X.079	2	D102,107
430-03898	LED,RED,RECT,.197X.079	2	D101,106
680-10886	CABLE,RIB,24-26G,7CX.1,5.5",NW	1	J101
710-09838	PC BD,HDRM,PCM80&1/90&1	1	

SWITCH BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
300-01029	DIODE,1N914 AND 4148	3	D112,115,119
430-09818	LED,GRN,T1,LITON,20DEG,12MCD	9	D111,113,114,116-118,120-122
453-09771	SW,PB,1P1T,6MM SQX7MM H,160GF	12	SW2-13
680-09763	CABLE,079,SCKT/SCKTRA,10C,2.0"	1	J102
710-09836	PC BD,SW,PCM80&1/90&1	1	

ENCODER BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-00514	RES,CF,5%,1/4W,100 OHM	4	R202-205
245-03610	CAP,CER,.01uF,100V,Z5U,AX	4	C200-203
452-09762	SW,RTY,ENCODER,36 POS,VERT MNT	2	SW14,15
680-09764	CABLE,079,SCKT/SCKTRA,6C,2.0"	1	J103
710-09837	PC BD,ENC,PCM80&1/90&1	1	

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Schematics and Assembly Drawings