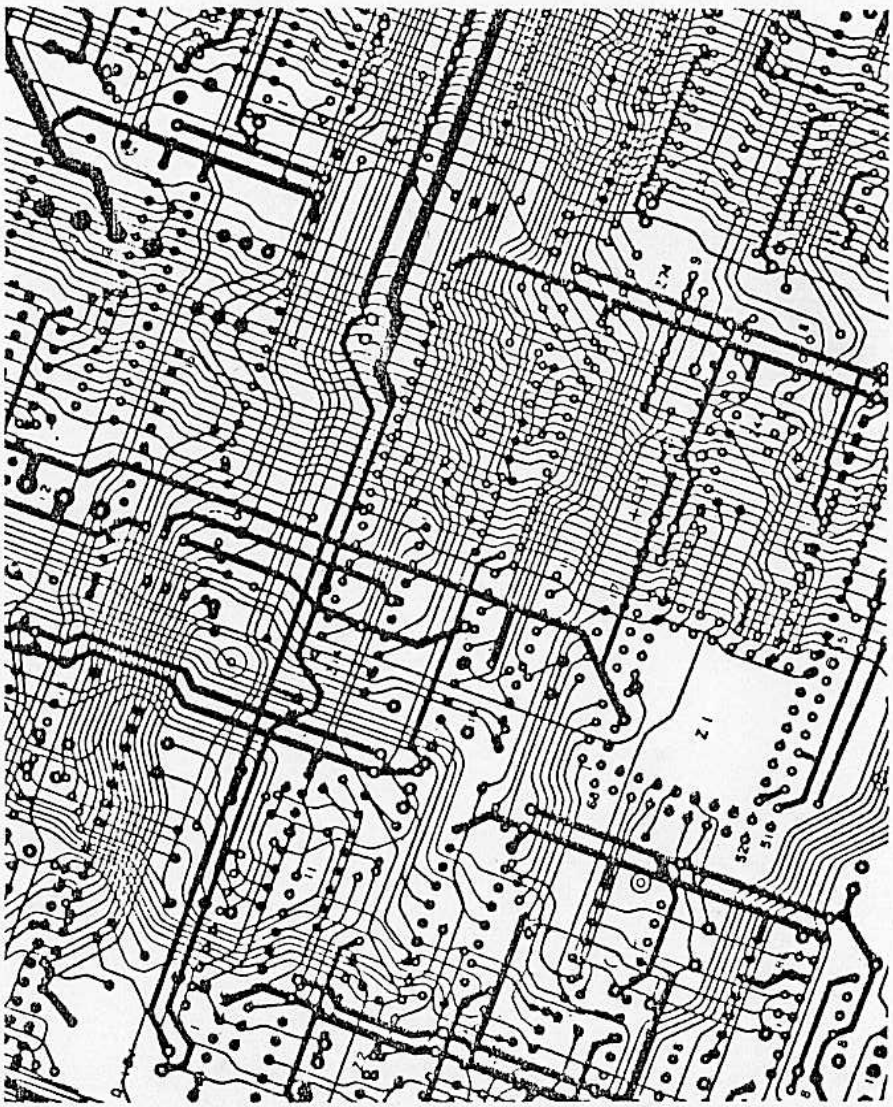
Fender®

CHROMA™ Polaris™

Service Manual



POLARIS SERVICE MANUAL

PART NUMBER 309006201

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SECTION 1: SYSTEM OVERVIEW

GENERAL DESCRIPTION:

The Chroma Polaris is a hybrid, combining the rich sounds of an analog synthesizer with the nearly limitless control capabilities of a digital computer. The latest microchips are evident in both domains: Curtis CEM 3374 dual VCO's and 3372 VCF/VCA's in the analog channels and the very powerful Intel 80186, 16-bit microprocessor in the digital computer.

It features a 61 note velocity sensitive keyboard, storage for 132 different programmed sounds and an on board polyphonic single track sequencer with a minimum note capacity of 650, internally expandable to more than 9000. In addition to a host of other features, the Polaris provides a parallel Chroma port and a serial MIDI interface.

SYNTHESIZER ARCHITECTURE:

There are 6 voices in the synthesizer. Each voice may be divided into 2 major parts: signal processing and modulation. The signal processing elements, which generate and shape the sound of each note, are implemented in the hardware. The modulation sources generate the signals that control the signal processing elements and are implemented in the software.

EACH VOICE CONSISTS OF THE FOLLOWING SIGNAL PROCESSING ELEMENTS:

2 OSCILLATORS: Each oscillator can be transposed in semitones over a wide range, and oscillator 2 can be detuned up to a semitone sharp. Vibratos and trills can be applied to the oscillators via the Mod Lever, with an adjustable depth. Delayed vibratos and trills can also be directly applied to the oscillators. The depth of this type of modulation is adjustable independently for the two oscillators, and can have positive or negative polarity. Oscillator 2 can be synchronized to oscillator 1, and oscillator 2 can be modulated by the main envelope, especially useful with sync.

2 WAVESHAPERS: Two basic shapes are available, Pulse and Saws. The pulse width is adjustable from 0% to 100%, and can be modulated by either the sweep or the main envelope. A simple sawtooth shape can be obtained by selecting the Saws shape and setting the pulse width to either extreme. An oscillator can be turned off by selecting the Pulse shape and setting the width to either extreme.

SYNTHESIZER ARCHITECTURE (CONTINUED)

RING MODULATOR: When this function is selected, the signals from thetwo oscillators are replaced by the digital cross-product of the two pulse signals. In this mode, the Saws/Pulse selections have no effect, but the pulse width controls do.

NOISE GENERATOR: This is a pink noise source that feeds into the filter. It can be turned on or off.

FILTER: This is a four-pole low-pass filter with resonance that can be adjustable from none at all to self-oscillation. It is modulatable by the sweep (delayed vibrato or trill), the main envelope, the foot pedal and the keyboard. All modulations may be positive or negative.

AMPLIFIER: The volume is controlled by its own dedicated envelope and its own volume control parameter. In addition, the foot pedal can modulate the volume with an adjustable depth.

THESE SIGNAL PROCESSING ELEMENTS ARE CONTROLLED BY A NUMBER OF MODULATION SIGNALS:

SWEEP GENERATOR: This generates either sine waves or square waves over a wide range of frequencies. In sine wave mode, all generators free-run asynchronously. In square wave mode, all generators run at the same rate, and each is synchronized to key depressions. The square wave shape is unipolar. The sweep rate can be modulated by the foot pedal to any degree in either direction. In addition, there is an adjustable delay that can be applied to the sweep.

ENVELOPE: The main envelope is an ADSDR type that can be used to modulate the pitch of oscillator 2, the pulse width of either oscillator, or filter cutoff. A switch allows it to be made touch-sensitive or not. The envelope operates in four phases. During the attack phase the envelope rises to its peak value and switches to its decay phase. It decays at an adjustable rate to the sustain level which is a percentage of its peak value. It then switches to the sustain decay phase during which it decays toward zero. When the note is released, the envelope is forced into its release phase. The two decays and the release can be set to infinity, if desired. A conventional ADSR shape can be approximated by setting the sustain decay time to infinity.

VOLUME ENVELOPE: This is an ADR type envelope that controls the volume only. A switch allows it to be made touch-sensitive or not. The decay and release can be set to infinity, which is useful for drone effects.

SYNTHESIZER ARCHITECTURE: (CONTINUED)

MOD LEVER: The left lever is dedicated to controlling the amount of sweep modulation (vibrato or trill) applied to the oscillators. Its depth is adjustable in both directions. Note that the sweep signal applied through the mod lever to the oscillators is not the delayed sweep.

BEND LEVER: The right lever is dedicated to the pitch bend function. Both depth and polarity are adjustable.

PEDAL: The foot pedal puts out a unipolar signal that can modulate pitch, filter cutoff, volume, sweep rate and sweep depth into the oscillators, all with adjustable depths. As with the mod lever, the sweep signal applied through the pedals to the oscillators is not the delayed sweep.

KEYBOARD: The keyboard is of course the main source of pitch information to the oscillators. Changes from note to note can be instantaneous or can be slurred by the glide control. The glide time is adjustable from 0 to 10 seconds. The keyboard pitch can also be used to modulate the filter cutoff. The depth of this modulation is adjustable over a wide range and allows no tracking, unison tracking, undertracking or reverse tracking. A special control transposes the keyboard an octave up without affecting notes already sounding. This effectively makes the keyboard an octave longer.

SECTION 2: COMPUTER TUTORIAL

This section is provided as a brief explanation of microprocessors. It is hoped that the reader already has some familiarity with the topic.

BINARY NUMBERS

All digital circuits encode information as binary numbers. The binary number system is a method of representing numbers using only the digits 0 and 1. Its advantage is that 0's and 1's are easy to represent electronically by two voltages, while representing decimal digits would require discriminating among ten different voltage levels.

In the decimal number system each digit has a "weight". The rightmost digit has a weight of 1 and each succeeding digit to the left has a weight that is ten times that of its neighbor. Thus, the number 123 equals, of course, (1 x 100) + (2 x 10) + (3 x 1). In the binary number system each digit or "bit" has a weight that is only two times that of its neighbor. Thus, the binary number 10101 equals (1 x 16) + (0 x 8) + (1 x 4) + (0 x 2) + (1 x 1), or 21.

When writing numbers we usually write only as many digits as are necessary to represent the number. When a number is represented by something mechanical or electronic, though, it is usually represented by a fixed number of digits. For instance, if your car has 123 miles on it, the odometer will read 00123. Computer numbers generally have a fixed number of bits depending upon the number of parallel lines or serial time-slots used to carry the number. Most computers are capable of processing information 8 bits at a time; this size number is called a "byte". A binary number that is 16 bits long is often called a "word". A binary number that is 32 bits long is often called a "double word" or a "long word".

If a decimal number has "n" digits, it can represent numbers from 0 up to ten to the nth power minus one. For instance, a five-digit odometer can represent numbers from 0 to 99999. If a binarynumber has "n" bits it can represent numbers from 0 up to two to the nth power minus one. A byte, therefore, can represent numbers from 0 to 255, while a word can represent numbers from 0 to 65535. Any attempt to represent a number larger than the available number of digits causes "wraparound", just as an odometer rolls over from 99999 back to 0.

It is often necessary to refer to a particular bit within a binary number. For this purpose, bits are always numbered from right to left starting with 0. Thus a byte starts on the left with bit 7 and ends on the right with bit 0. The purpose of this numbering is that the weight of bit n is two to the nth power. For instance, the leftmost bit in a byte, bit 7, has a weight of

BINARY NUMBERS: (CONTINUED)

2^7, or 128. Bit 0 is also called the "least significant bit" or "lsb", while the leftmost bit is called the "most significant bit" or "msb".

In a binary word or double word each byte can be referred to by number. A 16-bit word contains two bytes; byte 0 is the "least significant byte" or "LSB" while byte 1 is the "most significant byte" or "MSB". Note that these abbreviations use capital letters. In a double word, byte 0 is the LSB and byte 3 is the MSB.

If you examine the following table of powers of two, you will notice that some of the numbers are close to a power of ten. This gives rise to the shorthand notation of using the letters K or M as abbreviations for "kilo" and "mega". Normally, these prefixes mean exactly one thousand and one million; when applied to binary numbers, they actually refer to multiples of 1024 and 1048576. Thus, powers of two can be written in the following shorthand:

power	value	power	value	shorthand	power	value	shorthand
0	1	10	1024	1K	20	048576	1M
1	2	11	2048	2K	21	2097152	2M
2	4	12	4096	4K	22	4194304	4M
3	8	13	8192	8K	23	8388608	8M
4	16	14	16384	16K	24	16777216	16M
5	32	15	32768	32K	25	33554432	32M
6	64	16	65536	64K	26	67108864	64M
7	128	17	131072	128K	27	134217738	128M
8	256	18	262144	256K	28	268435476	256M
9	512	19	524288	512K	29	537870952	512M

One final observation on binary numbers: the lsb tells whether the number is odd or even. If the bit is a 0, the number is even; if it is a 1, the number is odd.

HEXADECIMAL NUMBERS

Binary numbers, while easy for an electronic circuit to manipulate, are hard for a human to read and write because they have so many digits. For instance, one million in binary is 11110100001001000000. However, converting between binary and decimal is not very easy to do manually, so computer numbers are generally written in a third number system, called "hexadecimal".

Hexadecimal, usually abbreviated "hex", means "base 16". Each digit has a weight that is sixteen times the digit to the right, which means that a total of 16 different symbols are needed to write hex numbers. Hex notation uses the ten decimal digits plus

HEXADECIMAL NUMBERS: (CONTINUED)

the six letters A through F for this purpose. Thus, one would count in hex: 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, etc. The digits A through F are equivalent to the decimal quantities 10 through 15, while 10 in hex is equivalent to 16 in decimal.

The purpose of hex notation is that it takes very few digits to represent a number and yet it is easy to convert to and from binary. Since sixteen equals two to the fourth power, each hex digit is equivalent to exactly four bits. Thus, one million in hex is F4240, which is (15 x 65536) + (4 x 4096) + (2 x 256) + (4 x 16) + (0 x 1). You will note that each hex digit corresponds to a group of four bits in the binary equivalent 1111,0100,0010,0100,0000.

The range of values represented by a byte is 0 to 255 in decimal. In hex, the range is 00 to FF. The range of values represented by a word (16 bits) is 0000 to FFFF. The range of values represented by a double word is 00000000 to FFFFFFFF. In hex notation multiple F's appear frequently as they represent "all ones".

COMPUTER PRINCIPLES

System components

A computer is a digital device that sequentially inputs data from and outputs data to external devices, including memory. All data operated on by the computer is represented by binary numbers. In addition the specific operations performed by the computer are selected by the computer's "program", which is a set of instructions also represented as binary numbers. Thus, a computer memory chip can hold both data to be operated on and instructions that tell the computer what operations to perform.

In systems where the computer performs a dedicated function there are two kinds of memory: RAM (random-access memory), which is the kind of memory that can be written into as well as read from, generally holds data only. ROM (read-only memory) or EPROM (erasable programmable ROM) cannot be written into by the computer, and so is used to hold information that never changes, including the computer's program.

In order for a computer to do anything useful it must be connected to devices other than memory. The devices that connect a computer to the outside world are called "input devices" and "output devices", or "input/output devices", often abbreviated "I/O devices". The specific nature of the I/O devices in a system depends upon the purpose of the system. A personal

COMPUTER PRINCIPLES: (CONTINUED)

computer might have a video interface chip for controlling a screen, keyboard scanning hardware for connecting to a typewriter keyboard, and a floppy disk controller for mass storage. A musical instrument, on the other hand, might have an analog to digital converter for measuring the position of various controls, a digital to analog converter and a bank of sample and hold circuits to generate analog control voltages, a keyboard scanner, and a number of latches to drive LEDs.

Since a computer is a sequential digital circuit it needs a timing source or clock. Frequently a computer chip will have an on-chip oscillator, so all that is needed is an external crystal. Other computer chips require a separate crystal, RC or LC oscillator circuit. Computer clocks generally run at several megahertz and all timing in a computer system is some subdivision of the clock frequency.

Computers usually need some means for an external device to force the computer to do something other than what it is already doing. The most obvious example is the "reset" signal that keeps the computer from doing anything until the power supply has had time to stabilize. Another example is the "non-maskable interrupt" signal, which is often used by a power-fail sensing circuit to allow the system to shut down gracefully. During normal operation, though, one or more "maskable interrupts" are often needed. These signals cause the computer to temporarily drop whatever it is doing and switch to a different program, presumably a program that services the device that generated the interrupt. When the service program is complete, the computer resumes the interrupted program where it left off. These interrupts are called "maskable" because they can be temporarily disabled, or "masked", when the computer is executing a critical section of its program that should not be interrupted.

Computer Memory

A memory chip can store a large number of bits. The bits are arranged into an array that has a specific length and width. The width of a memory chip is the number of bits that can be read or written at a time; most memory chips are either 1, 4 or 8 bits wide, the smaller widths usually arranged in parallel to make larger widths. The length of a memory chip is the number of different "locations" in the memory chip. For instance, a 2764 EPROM has 65536 bits, arranged in an 8192 x 8 array; the 2764 has 8192 locations, each containing eight bits or one byte.

Memory chips almost always have widths and lengths that are powers of two. The length determines the number of bits needed to select any of the locations in the chip. The 2764, with 8192 locations, requires 13 bits. Each location is numbered, starting with 0, and these numbers are called "addresses". In hex the

COMPUTER PRINCIPLES: (CONTINUED)

range of addresses in a 2764 would be written 0000 to 1FFF. Thus, in addition to representing data and instructions, numbers can be used to represent the addresses of data and instructions.

A computer communicates with its memory by using two buses and some control signals. A bus is a set of parallel lines that connects multiple components in parallel, used to carry a binary number. The two buses used by a computer are the "address bus" and the "data bus".

A computer reads from its memory by placing an address on the address bus (which goes to the memory chip) and then generating a pulse on a control line called the "read strobe". The memory chip responds to this strobe by placing the data from that location onto the data bus (which goes back to the computer).

A computer writes to its memory by placing an address on the address bus and the data to be written on the data bus. It then generates a pulse on a control line called the "write strobe". The memory chip responds to this strobe by recording the state of the data bus in the specified location.

Memory Address Decoding

Usually, a computer will be connected to more than one memory chip. In this case, the most significant bits of the address bus connect to one or more decoder chips, such as the 74LS138, and the outputs of the decoder chips go to the "chip select" inputs on each memory chip. Only the least significant bits of the address bus connect directly to the memory chips. For instance, if a system required eight 2764 EPROMs, their address inputs might connect to the least significant 13 address bus lines, A0 through A12. Then address lines A13, A14 and A15 would be decoded by a 74LS138 to generate the chip select signals to each memory chip. When the read strobe pulse is generated only the memory chip whose chip select is active would respond.

In the above case, each memory chip would occupy a different range of system addresses. Locations 0000 through 1FFF within each chip would correspond to the following system addresses:

0000 through 1FFF -- chip #0	8000 through 9FFF -- chip #4
2000 through 3FFF -- chip #1	A000 through BFFF -- chip #5
4000 through 5FFF -- chip #2	C000 through DFFF -- chip #6
6000 through 7FFF -- chip #3	E000 through FFFF -- chip #7

COMPUTER PRINCIPLES: (CONTINUED)

Data Bus Width

Some computers have 8-bit data buses. In such systems all memory and I/O devices are connected to the same 8 lines. Many modern computers, though, have 16-bit or 32-bit data buses. In these systems it is still necessary to be able to manipulate data in byte-sized chunks.

In a 16-bit system half the memory chips are connected to each half of the data bus and the lsb of the address bus is used to select which half of the data bus data is to be transferred on. Therefore, all even-addressed bytes would be contained in memory chips on the lower half of the bus and all odd-addressed bytes would be contained in memory chips on the upper half of the bus. Such a system can access an entire 16-bit word at a time for speed where appropriate, yet can still access individual bytes. In a 16-bit system the address bus is shifted one place to the right before connecting to the memory chips; that is, address bit 1 goes to A0 on the memory chips, bit 2 goes to A1, bit 3 goes to A2, etc.

In a 32-bit system one quarter of the memory chips are connected to each quarter of the data bus and the two lsbs of the address bus select which section of the bus is to be used. Such a system can access an entire 32-bit double word at a time, or a 16-bit word, or an individual byte. In a 32-bit system the address bus is shifted two places to the right before connecting to the memory chips; that is, address bit 2 goes to A0 on the memory chips, bit 3 goes to A1, bit 4 goes to A2, etc.

Input/Output Device Addressing

Input and output devices are communicated with in the same way that memory is communicated with. The only differences are that there are generally only a small number of addresses needed to select from among the I/O devices and that writing to an I/O location and reading from the same I/O location may have totally unrelated effects. Typically each I/O device has one or more input location associated with it and/or one or more output location associated with it.

If an I/O device has only one location associated with it, it receives the read and/or write strobe signal along with a chip select signal from an address decoder. If an I/O device has more than one location associated with it, it also receives one or more lsbs of the address to select from among the different locations used by the I/O device. In an 8-bit system address bits starting with bit 0 would be used for this purpose. In a 16-bit system I/O devices are still usually only 8 bits wide, so

COMPUTER PRINCIPLES: (CONTINUED)

address bits starting with bit 1 would be used to select the locations within each device and all locations within the I/O device would be even or odd, depending upon which half of the data bus they were connected to.

In some computers I/O devices are connected to the computer so that they appear to be memory locations. That is, the same instructions that read from and write to memory are used to input from and output to I/O devices. In other computers a separate set of instructions is used to access I/O devices and an external signal indicates whether the address on the address bus refers to a memory location or an I/O location. In the latter case, the computer has two separate "address spaces" that have nothing to do with each other. As far as the hardware is concerned, though, the signal that differentiates between memory and I/O operations can be thought of as just one more address bit.

Direct Memory Access

High-speed I/O devices such as disk controllers and high-speed serial interfaces usually require that a large number of bytes be input to or output from memory in a completely sequential manner. That is, the first byte must be read from location n, the second from location n+1, the third from location n+2, etc. If the I/O is slow enough, the computer can uses an interrupt program to perform this kind of operation and still have plenty of time left over for other things. If the I/O gets up above 20 or 30 kilobytes per second, the computer spends practically all its time performing what amounts to a very simple operation.

In systems where the I/O is too fast to use interrupts, special hardware, called a "direct memory access controller" or "DMA controller", is often included to allow an external device to momentarily take over the address and data buses, and read or write a byte directory from or to memory. This only uses a microsecond or so for each byte transferred, compared to twenty or thirty microseconds needed by an interrupt program. Some computers include this function on the computer chip itself, making it invisible to the service technician. In such a system the DMA request input to the computer looks just like an interrupt request; the only difference is that the DMA request only causes one or two bus cycles to be inserted into the flow of things.

SECTION 3: CIRCUIT DESCRIPTIONS

MAIN BOARD:

The Polaris Main Board includes the bulk of the circuitry in the Polaris, including the computer and synthesizer circuits. The sections of this board will be described pretty much in the order in which they appear on the schematics.

Computer

The Polaris' computer is Z1, an Intel 80186. This is a fast 16-bit microprocessorwhich includes a number of useful peripheral functions on the same chip, where the service technician doesn't have to worry about them. The main timing source is crystal Y1, which is connected to the oscillator pins on the computer and must be twice the desired system clock frequency, either 12MHz or 16MHz depending upon the speed 80186 used. The 80186-6 uses a 6MHz clock and must be used with a 12MHz crystal; initially, production units are being built this way. The 80186-3 uses an 8MHz clock and should be used with a 16MHz crystal; eventually, production units may be shipped this way, if the -3 version of the computer comes down in price.

The computer communicates with external devices, including its memory, over a 16-bit wide multiplexed address/data bus. This bus comes off the computer on pins AD0 through AD15. The 16 lsbs (least significant bits) of the address appear on these pins at certian times, and data appears on these pins at other times.

Data can flow over the bus one word (16 bits) at a time, in which case the entire bus is used, or one byte (8 bits) at a time, in which case one half of the bus (either the upper or lower) is used. A line called BHE/ (bus high enable) works with address bit 0 to indicate which halves of the bus are used:

BHE/	A0	access type
1	0	even-addressed byte on low half of bus
0	1	odd-addressed byte on high half of bus
0	0	even-addressed word on both halves of bus

(Odd addressed words are accessed one byte at a time in two operations.) Note that address bit 0 could have been called BLE/ (bus low enable), as its function is perfectly symmetrical with the function of BHE/.

The computer communicates with external devices by "running bus cycles". A bus cycle is a sequence of events that causes an external device to be selected and causes data to be transferred. A bus cycle goes like this:

The computer indicates the direction of the transfer using the DT/R/ (data transmit/receive) line. This line is intended for controlling the direction of external bus transceivers such as

MAIN BOARD: (CONTINUED)

Z17.

The computer identifies the device it wishes to communicate with by putting out an address. This involves the following:

The ALE (address latch enable) signal is raised. This causes latches Z14 and Z15 to "open up", so that the signals on their inputs will appear at their outputs.

The computer places the 16 lsbs of the address on pins AD0 through AD15. The 4 msbs of the address appear on four other pins that aren't used, so they aren't shown in the schematic. BHE/ is also driven.

The computer internally decodes the msbs of the address into a number of chip select signals. These include I/O device chip selects PCS0/ through PCS6/, RAM chip selects MCS0/ through MCS3/, and EPROM chip select UCS/. One of these is activated. An additional chip select, LCS/, is not used, and so is not shown in the schematic.

ALE is lowered, latching the 16 lsbs of the address. These bits remain stable at the outputs of Z14 an Z15 for the rest of the cycle.

Since the address has now been latched, the address is removed from lines AD0 through AD15.

If the operation is a memory write or an output, data is placed on the AD0 through AD7 lines, and/or the AD8 through AD15 lines.

Either the RD/ (read strobe) or WR/ (write strobe) line is activated, depending upon the direction of the transfer. This strobe initiates the data transfer. At about the same time, DEN/ (data enable) goes active. This signal is intended to enable external bus transceivers such as Z17.

If the operation is a memory read or an input, the selected device puts its data on the AD0 through AD7 lines, and/or the AD8 through AD15 lines.

After a certain amount of time the read or write strobe pulse is terminated. Normally, the width of this pulse is two clocks (333ns at 6MHz, 250ns at 8MHz), but certain I/O accesses take extra clocks. DEN/ is also deactivated.

The device driving the data bus (either the computer, the memory, or an input device) turns off its bus drivers.

MAIN BOARD: (CONTINUED)

At this point, the bus is ready for another bus cycle. Frequently, another cycle follows immediately at a maximum rate of one cycle every four clocks. If the computer does not need to access memory or an I/O device immediately, though, one or more idle clocks will be inserted between bus cycles.

The computer accepts two external signals from the power supply. DC OK connects (through two inverters) to the RES/ input to the computer. When the +5V supply is out of regulation, this line holds the computer in a reset state. AC OK connects (through an inverter) to the NMI/ input to the computer. When AC OK goes low, indicating that the power switch has been turned off, this generates a "non-maskable interrupt" to the computer. This causes the computer to drop whatever it is doing and execute a special program that mutes the master volume VCA and then halts.

The computer accepts a number of other signals from other devices on the Main Board via the 4x4 jumper platform. A high-level signal on one of the interrupt inputs INT0 through INT3 causes the computer to temporarily drop whatever it is doing and execute a short program to service the device that generated the interrupt signal. Normally, the interrupt program performs an input or output operation that cancels the interrupt request. If a hardware problem prevents the interrupt request from being cancelled, the computer will get interrupted over and over again.

A high-level signal on one of the DMA request inputs DRQ0 or DRQ1 causes the on-chip DMA controller to interleave two bus cycles between the cycles used by the computer. If the DMA controller is inputting data, the first cycle will be an input and the second cycle will be a memory write. If the DMA controller is outputting data, the first cycle will be an output and the second cycle will be a memory read. The input or output cycle normally clears the source of the DMA request.

A few miscellaneous gates are also associated with the computer. Z19A, Z20A and Z20D split chip select UCS/ into two chip selects, UCS0/ and UCS1/, depending upon the state of an address bit. The particular address bit used for this purpose is jumper-selectable, depending upon the size of EPROM installed for Z12 and Z13. Z21A through D split the read and write strobes into two pairs of strobes, one pair for each half of the data bus. RD/ and WR/ are gated with A0 to generate RD LO/ and WR LO/, which are the strobes for all devices on the lower half of the data bus, including all even-addressed memory. RD/ and WR/ are also gated with BHE/ to generate equivalent strobes for the upper half of the data bus, which contains only odd-addressed memory.

SECTION 3: CIRCUIT DESCRIPTIONS

MAIN BOARD: (CONTINUED)

Memory Array

The memory consists of up to six pairs of byte-wide memory chips. Since the chips are 8 bits wide and the data bus is 16 bits wide, memory chips are always used in pairs. Sockets Z2 through Z9 are used for CMOS RAM, and are provided with read and write strobes, battery backed up power, and isolation transistors on the chip selects. Sockets Z10 through Z13 are used for EPROM and are provided with read strobes only, no battery backup, and no isolation transistors on the chip selects.

The system supports two types of RAM chips, 6116s, which are 2Kbyte chips, and 6264s, which are 8Kbyte chips. When the larger chips are used, the write strobes go to pin 27 on the chips and the two jumpers between the rows of chips connect address bit 12 to pin 21. When the smaller chips are used, they are installed such that socket pins 1, 2, 27 and 28 are empty. The two jumpers steer the write strobes to socket pin 21 (which is chip pin 23). Five configurations are allowed:

total size	chip size	chip type	chip count	where installed
16K	2K	6116	8	Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9
16K	8K	6264	2	Z2, Z3
32K	8K	6264	4	Z2, Z3, Z4, Z5
48K	8K	6264	6	Z2, Z3, Z4, Z5, Z6, Z7
64K	8K	6264	8	Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9

As long as the jumpers are positioned according to the size of the chips, the software can determine how much memory is present in the system.

The isolation transistors on the chip selects to the CMOS RAMs are cascode transistors whose bases are powered from the DC OK signal. During normal operation these act as saturated switches that pass the chip select signals to the RAM chips. When DC OK is inactive, though, the chip select signals don't reach the RAM chips. For instance, when the power is off the emitters and bases of these transistors are all at 0V, so the transistors are off; the collectors are pulled up to the battery backup power supply by the pullup resistors.

The system supports two types of EPROM chips, 2764s, which are 8Kbyte chips, and 27128s, which are 16Kbyte chips. The jumper by Z19A, located near the left rear corner of the board, determines

MAIN BOARD: (CONTINUED)

the number of addresses occupied by each pair of chips. Four configurations are allowed:

total size	chip size	chip type	chip count	where installed
16K	8K	2764	2	Z12, Z13
32K	8K	2764	4	Z10, Z11, Z12, Z13
48K	8K	2764	2	Z10, Z11
	16K	27128	2	Z12, Z13
64K	16K	27128	4	Z10, Z11, Z12, Z13

Changing Memory Chips

Memory chips must be changed with the power off, obviously. CMOS RAM chips, though, must also be changed with the battery disconnected. You should unplug J15 from the main board before changing any CMOS RAM chips; it is not sufficient to remove a battery from the holder, as the capacitor on the holder retains its charge for a minute or more.

Note also that if you change EPROMs to a different software revision, the memory locations used for different purposes usually change, so all software adjustments will probably need to be redone and the programs and sequences reloaded. As a matter of courtesy to your customers, you should always save all programs and sequences on cassette before working on the instrument and reload them when you are finished.

Battery Backup Power Supply

When the DC OK signal is active, indicating that the +5V digital supply is within regulation, Q5 is turned on. This turns on Q6, connecting the +5V BAT rail to the +5V digital supply. Capacitor C1 limits the rate at which the power can switch. Since the battery voltage is only about +3V, CR1 will be reversed biased.

When the DC OK signal is inactive, Q5 and Q6 are off and the +5V BAT rail is connected to the battery through CR1. This diode is a germanium diode because of its low forward voltage drop. When the power is off, transistor Q6 is in an unusual state: its collector is more positive than its emitter. A transistor, though, can be operated upside-down. When it is, its emitter acts as a collector and its collector acts as an emitter. R12 connects the base to the "emitter" holding the upside-down transistor off.

MAIN BOARD: (CONTINUED)

Data Out Buffer

The data bus is split into two buses, the "data in/out bus" (lines DI0 through DI7) and the "data out bus" (lines D00 through D07). The data out bus is driven by bus driver Z16 whenever the computer is writing or outputting; it connects to all output devices that present a significant load to the bus. The data in/out bus is connected directly to the computer and goes to all input devices and all bidirectional devices, including the even addressed memory chips. (It also goes to one output device.) Thus, devices like memories, which don't have very strong bus drivers, don't have to drive a heavily loaded bus.

Panel Buffer

J10 provides a data bus and control signals to the control panel. In the Polaris it is a 26-pin connector, although the board is laid out to accept a 34- or 40-pin connector, in case more lines are needed in another application. The data bus to the control panel is a bidirectional bus, isolated by transceiver Z17. This chip is only enabled when PCS3/ is active, indicating that a device on the control panel is being addressed. Bus driver Z18, which is also enabled by PCS3/, places address bits 1 through 6 onto lines A0 through A5 and places the RD LO/ and WR LO/ strobes onto the RD/ and WR/ lines to the panel. The STB (signal is an active-high OR of the two strobes, the SEL/ signal is a buffered PCS3/, and the R/W/ (read/write) is a version of DT/R/ gated with PCS3/.

J10 also carries a DC OK signal, power (including battery power), and some analog signals.

Strobe Decoders, Miscellaneous I/O

Sheet two of the schematic includes some miscellaneous decoding and I/O chips.

Z29 is an 8-to-1 multiplexer that acts as eight single-bit input ports. When PCS1/ is active, a RD LO/ strobe will cause one of the eight inputs to this chip to be placed on data bus bit DI0. The particular input selected depends upon address bits A1, A2 and A3. Input 0 is the end of conversion signal from the analog to digital converter. Inputs 1 and 2 are the two footswitch inputs. Input 3 comes from the timer interface circuit. Input 4 is a status signal from the MIDI/Triad interface. Inputs 5 and 6 are not used. Input 7 comes from a jumper that is used to tell the software whether the system is running at 6MHz or 8MHz.

MAIN BOARD: (CONTINUED)

Z30 is an 8-bit addressable latch that acts as eight single-bit output ports. When PCS1/ is active, a Wr LO/ strobe will cause the bit on D00 to be written to one of the eight outputs of this chip. The particular output selected depends upon address bits A1, A2 and A3. Output 0 controls the cassette motor control relay. Output 1 is not used in the Polaris. Output 2 ultimately controls the serial output data to the cassette or sync output. Output 3 selects the cassette and sync output level. Outputs 4 and 5 enable the sample and hold circuits. Outputs 6 and 7 switch the cassette input and output into or out of the audio output.

Z28 is a dual 4-bit strobe decoder. When PCS0/ is active, a RD Lo/ strobe will be steered to one of four places, depending upon address bits A1 and A2. Except for the RD ADC/ output, these strobes are not actually used to read data into the computer. Instead they are used only to set or clear flip-flops, and the garbage read in on the bus is ignored. When PCS0/ is active, a WR LO/ strobe will be steered to one of four different places, depending upon the same address bits. The START ADC/ output is not actually used to write anything, so the data written is ignored.

Z27 is an 8-bit strobe decoder. When either RD LG/ or WR LO/ occurs, pin 6 will go high. If PCS4/ is active, one of the eight outputs will generate a strobe pulse, depending upon address bits A1, A2 and A3. Some of these are write strobes and some are read strobes, but there is no confusion because the software never attempts to input from an output location or output to an input location. The WR RXDIS/ and WR RXEN/ lines are not actually used to write anything. Instead they are used to clear and set a flip-flop, so the data written is ignored.

Outputs 6 and 7 from Z27 are not directly connected. Instead, the I/O locations represented by these strobes are decoded by Z85D. If address bits A2 and A3 are both high, indicating that output 6 or 7 is selected, the MIDI interface UART, Z87, is selected, and A1 selects one of two registers inside that chip.

Footswitches

The footswitches are momentary switches to ground, either normally open or closed. (Their state is sensed on power-up.) The RC network on these inputs filters the switch bounce and the Schmitt trigger inputs of Z46C and D square up the signal again. This eliminates the need for software debouncing.

MAIN BOARD: (CONTINUED)

Keyboard

When PCS2/ is active, a WR LO/ strobe will cause the four bits on data bus lines D00 through D01 to be latched by Z33. This four bit number is decoded by Z35 and Z36 into 16 lines, KS0A to KS7B, one of which will be activated at any one time. Each line selects a bank of eight keyswitches; the state of the selected bank appears on KD0 through KD7. If a particular switch is open, the corresponding ID line will be pulled high by its pullup resistor. If a particular switch is closed, the corresponding KD line will be pulled low through a diode on the keyboard itself. When PCS2/ is active, a RD LO/ strobe causes the state of the selected bank to be gated onto data bus lines DI0 through DI7.

Motor Control

When the MOTOR/ line from Z30-4 is low, relay K1 is energized. When the line is high, the relay is released. CR2 protects against inductive kick-back from the relay coil.

Channel Control

Z31 is another addressable latch. When PCS5/ is active, a WR LO/ strobe causes the bit on D00 to be written into one of the eight outputs, depending upon address bits A1, A2 and A3. Six of these select whether each synthesizer channel routes its output to the main output of the autotune timer. The remaining two are used to generate pulses for the click circuits.

Z32 is an 8-bit strobe decoder. When PCS6/ is active, a WR LO/ strobe is steered to one of seven places, depending upon A1,A2, and A3. Six of these strobes go to latches in each synthesizer channel, allowing data to be written to each channel. The seventh strobe goes to a latch that holds the number of the currently selected sample and hold.

Chroma Interface

The Chroma Interface consists of two independent, symmetrical parallel ports, one for input and the other for output. When the WR CHROMA/ strobe (from Z27) happens, a byte of data is latched into Z22 and delivered to the CO0 to CO7 lines. The strobe also clocks a 1 into flip-flop Z26A, pulling down the CO FULL/ line. Transistor Q7 simply isolates this line when the power is shut off, just like the isolation transistors on the CMOS RAM chip select lines. This output is an open-collector and is pulled up by a resistor in the receiving device. Typically, this signal

MAIN BOARD: (CONTINUED)

interrupts the device at the other end, which reads in the byte and generates a pulse on CO ACK/. This pulse clears flip-flop Z26A, causing CHROMA OUT REQ to go high. This interrupts the Polaris' computer so that it can output the next byte.

When a byte is received on the CI0 through CI7 lines from an external device, that device pulls CI FULL/ low. Z26B acts as an inverter, causing CHROMA IN REQ to go high. This interrupts the Polaris' computer so that it can read in the byte. When the RD CHROMA/ strobe (from Z27) happens, the byte is placed on data bus lines DI0 through DI7. The strobe is also sent out over the CI ACK/ line, which normally causes the device at the other end to negate the CI FULL/ line. It also normally interrupts the device at the other end so that it can transmit the next byte. The CI ACK/ line also has an isolation transistor so that it will not be held active when the power is shut off.

MIDI Interface

Z83 and associated gates act as a clock divider. TheCLKOUT signal comes from the computer and is either 6MHz or 8MHz. This is divided by either 6 or 8, depending upon the jumper on Z83-9, to produce a 1MHz clock on Z83-12. This is further divided to 500KHz on Z83-11. When the WR RATE/ strobe (from Z27) happens, the bit on D00 is written into flip-flop Z25B and this determines which clock, the 1MHz or the 500KHz, gets through Z23B and C (open-collector NAND gates). The selected clock is applied to the RxC (receive clock) and TxC (transmit clock) inputs on Z87.

Z87 is a UART (universal acynchronous receiver/transmitter) that communicates information serially at a baud rate (number of bits per second) that is 1/16th of its clock rate. Thus, the baud rate is either 31.25K or 62.5K. This chip is outputted to or inputted from whenever PCS4/ is active and A2 and A3 are both 1. The chip is controlled by doing an output with A1 low and its status is sensed by doing an input with A1 low. A byte of data is given to the chip for transmitting by doing an output with A1 high and a received byte as inputted from the chip by doing an input with A1 high. The DR/T/ signal (the inversion of DT/R/) tells the chip whether an access is an input or an output.

Transmitted data comes from Z81D to output pin J11-6. This a current loop output whose return path is on J11-4. Received data comes in as a current in J11-1, through opto-isolator Z86, and out J11-3. The output of the opto-isolator goes to the RxD (receive data) pin on the UART.

Flip-flop Z47B and open-collector NAND gates Z23A and Z23D allow the output to be driven by either the TxD (transmit data) pin on

MAIN BOARD: (CONTINUED)

the UART or by a copy of the received data. The first mode is called OUT mode and the second is called THRU mode. Generating a WR THRU/ strobe (from R27) causes Z47B to be set, putting the output in THRU mode. Activating the RTS/ output from the UART forces the output into OUT mode. The RTS/ output is a general purpose bit controlled by writing to the UART's control register.

Flip-flop Z47A controls the DCD/ (data carrier detect) input to the UART. When low, the UART receiver is enabled. When high, the UART receiver is held reset. This flip-flop is manipulated by generating WR RXDYS/ and WR RXEN/ strobes (from Z27). In the Polaris it is left set, so that the receiver will be enabled.

When a byte of data is received, the IRQ/ output from the UART goes low. This is an open-drain output pulled up by R95. When this goes low, U REQ (UART request) goes high. This is jumpered into the DRQ0 input to the computer. The computer's DMA controller reads in the byte from the UART's data register, causing IRQ/ to go high and U REQ to go low again until the next byte is received.

When a byte of data is to be transmitted, the computer writes it to the UART data register. No interrupt or DMA request is needed to tell the computer that the UART is ready for output. Instead, the computer checks the status of the UART to see if it can accept a byte of data whenever the computer is interrupted by its timer. The timer interrupt occurs at 2400Hz, so the status is checked plenty often enough.

Counter Z84 and sections of Z82, Z85, and Z47 are not used in the Polaris. The purpose of these circuits is to support a proprietary interface protocol under development at Fender.

Timer Interface, Serial I/O

Timer 1 inside the computer is used to measure the period of a number of input frequencies. The WR TSEL/ strobe (from Z28B) causes a four-bit number to be written into latch Z39. If the msb of this number is 0, data selector Z38 will be enabled, and the other three bits will select one of the inputs to appear at Z73-5 anl Z42-6. If the msb of this number is 1, Z38 is turned off and switch Z48D is turned on, causing the state of the SERIAL IN line, buffered and inverted by Z46B, to appear at the same point. Input 0 on data selector Z38 comes from the SYNTH ZCD line, buffered by Z46A, and the remaining 7 inputs come from successive outputs of a binary counter driven by the same signal. Thus, depending upon the number in latch Z39, any of nine signals can appear at Z73-5 and Z42-6:

MAIN BOARD: (CONTINUED)

0000 -- SYNTH ZCD	0100 -- SYNTH ZCD / 16
0001 -- SYNTH ZCD / 2	0101 -- SYNTH ZCD / 32
0010 -- SYNTH ZCD / 4	0110 -- SYNTH ZCD / 64
0011 -- SYNTH ZCD / 8	0111 -- SYNTH ZCD / 128

1000 -- SERIAL IN

The first eight are used during autotune, so that the period of a signal can be accumulated over multiple cycles if the frequency is high. The last is used during cassette operations and for sync input.

The input thresholds of Z46A are normally 1V and 2V. R21 injects current into an internal node that shifts these thresholds so that they are roughly centered around ground. The SYNTH ZCD signal is a high-level analog signal that comes back from the synthesizer voice being tuned, so Z46A acts as a Schmitt trigger zero-crossing detector. The capacitor simply makes the chip less sensitive to noise pickup.

Z46B works the same way, although the resistor connected to its internal node can be switched in and out by Z48A, under control of the SER LEVEL line (from Z30). Thus, the input threshold can be adapted for use with audio signals centered around 0V or digital signals centered around 1.5V.

Whatever input signal is selected is fed into Z73C and Z42B, C and D. These gates act as an exclusive-or gate, selecting either the input signal or its inversion depending upon the state of flip-flop Z43A. Whichever polarity is selected is fed into the clock input of Z43B, so that when a positive edge occurs, Z43B will be set. When this flip-flop is set, three things happen:

The T REQ (timer request) line goes high, interrupting the computer.

The T GATE (timer gate) line goes low, stopping Timer 1 inside the computer so that the computer can read it.

Z43A is toggled, causing the opposite polarity of the input signal to be routed into Z43B.

Once the computer has read and reset Timer 1, it generates a CLR T REQ/ strobe (from Z28A). This does three things:

The T REQ line goes low, removing the interrupt request.

The T GATE line goes high, allowing Timer 1 to run.

Z43B is made ready to detect another edge.

MAIN BOARD: (CONTINUED)

Thus, this circuit can measure the time between zero-crossings of any signal. This can be used to measure pulse width or frequency of a synthesizer signal or receive information from a cassette.

When the SERIAL IN line is being used as a sync input, the circuit is used somewhat differently. Since sync pulses are much slower, only the occurrence of the interrupts are monitored and the actual period measurements are discarded. Since only one polarity of sync input is important, the computer arbitrarily sets or resets Z43A after each sync pulse, so that only the desired polarity edge will be looked for. The computer does this by generating SET POL/ or CLR POL/ strobes (from Z28A).

The cassette and sync systems also require output. All output is quantized to a 2400Hz clock, appearing on the SER OUT CLK line. The pulses on this line coincide with timer interrupts inside the computer. The timer interrupt program calculates the correct state of the serial output and puts the bit onto the SER OUT line (from Z30). The next SER OUT CLK clocks this into Z52A, cleaning up the timing. The output of Z52A is attenuated to a low level audio signal and fed into opamp buffer Z40. If the SER LEVEL signal is low, switch Z48C will be off and the op-amp will function as a simple voltage follower, so the SERIAL OUT line will have a low-level audio signal on it. If the SER LEVEL signal is high, switch Z48C shorts the negative input to the opamp to ground, causing it to function as a comparator. The low-level signal is thus converted to a very high-level signal that is roughly RS-232C compatible.

The SERIAL IN and SERIAL OUT lines can be mixed into the audio output via the DATA AUD line. This line is a separate audio path to the Output Board and is used for all signals other than the synthesizer outputs. If the SER OUT MUTE line (from Z30) is low, the serial output data will pass through Z42A, Z73F and Z73D, and get mixed into the DATA AUD line. If the SER IN MUTE/ line (also from Z30) is high, the serial input audio signal will pass through Z48B and get mixed into the DATA AUD line. CR3 and CR13 protect the CMOS switch from excessive input levels.

Click Generator

The metronome click is generated by raising HI CLICK (from Z31) for a few microseconds and then lowering it again. The duration of the pulse is controlled by the software and determines the ultimate volume of the click. This pulse injects a transient into hi-Q bandpass filter Z41A, giving the click a pleasing pitch.

The switch press click and error burp sounds are generated in the

MAIN BOARD: (CONTINUED)

same manner by the LO CLICK signal. Bandpass filter Z41B is tuned to a lower frequency. The burp sound is simply a number of clicks in rapid succession.

Analog to Digital Converter

The analog ground and +5V supplies connect to the ADC GND and ADC REF lines at the A/D converter circuit, thus providing a common reference for the A/D and all analog inputs. The A/D chip expects an analog input in the range of 0V to two times its reference voltage, so the reference is divided down to +2.5V with trimmer R45.

The A/D chip is a self-clocked device that has its own on-chip RC oscillator, using the CK0 and CK1 pins. A conversion is performed by presenting a stable analog input, generating a WR/ strobe (from START ADC/, from Z28B), and waiting for the INTR/ output (to EOC/, to Z29) to go low, which takes about 100 or 200 microseconds. When it goes low, the converted number can be read by applying a RD/ strobe (from RD ADC/, from Z28A). In the Polaris the conversions are initiated by the timer interrupt program at a fixed 2400Hz rate. Every tick of the timer the interrupt program checks EOC/, reads in the completed conversion using RD ADC/, selects a new analog input by writing a byte to a device on the control panel, and starts the new conversion by strobing START ADC/.

Digital to Analog Converter

This circuit is a 14-bit precision multiplying D/A converter with bipolar output. The nominal output range is roughly -5V to +5V when presented with a +3V reference input. The 14-bit number is output to the D/A converter in two operations. The LSB is written using the WR DAC L/ strobe and the MSB is written using the WR DAC H/ strobe (both from Z28B). Trimmer R46 is used to adjust the offset voltage of Z58 so that it is within 200uV of 0V, necessary to maintain the accuracy of the D/A converter chip.

Sample and Hold Control

Each sample and hold circuit in the synthesizer channels is assigned a six-bit number. The 3 msbs identify one of the six channels and the 3 lsbs identify one of the six sample and holds within that channel. Actually, one channel has a seventh sample and hold used for master volume. A sample and hold is selected by writing a number into latch Z63 using the WR SH SEL/ strobe (from Z32). The three lsbs go in parallel to all six synthesizer

MAIN BOARD: (CONTINUED)

channels, but the three msbs are decoded by Z60 and Z61 into individual strobes for each channel. When the SH DISABLE line (from Z30) goes low, the selected output of Z61, one of the lines SLOW0/ through SLOW5/, will go low. In addition, if the SH LAG line is low at the same time, the selected output of Z60, one of the lines FAST0/ through FAST5/, will go low.

Z62 is a multiplexer that selects the reference input to the D/A converter. When one of the oscillator pitch or filter cutoff sample and holds is selected, the SHA0 line will be low, so diodes CR8 and CR9 will be turned off. In this state the temperature compensation line from the selected synthesizer channel, which is nominally at around +2.5V, is used as the D/A converter reference. If any other sample and hold is selected, SHA0 will be high, causing either Z62-2 or Z62-4 to be selected, providing a fixed +3V reference to the D/A converter.

Noise Generator

This circuit is a digital noise generator that generates a pseudo-random sequence of bits at about 100KHz that repeats about every 1.3 seconds. This bit stream sounds like white noise and is filtered into something more like pink noise and buffered.

Synthesizer Data Bus Buffer

Z49 is a bus driver that isolates the data bus that goes to the synthesizer voice from the main data bus, for noise considerations. It is enabled whenever PCS6/ is active and address bits 2 and 3 are not both 1. In other words, it is active whenever Z32 is generating one of the strobes WR SYN 1/ through WR SYN 6/.

Synthesizer Voices

Sheet four of the schematic details a single synthesizer voice. This circuit is repeated six times.

The DAC line from the D/A converter contains all the control voltages for all channels, time-multiplexed. This goes to ZX01 and ZX02 in each voice. These are the sample and hold switches. When the selected channel's SLOW(N)/ line goes low, the switch inside of ZX01 selected by SHA0 through SHA2 is turned on, connecting the DAC line to one of the 0.033uF capacitors. These capacitors connect through 1Mohm resistors to 0.0068uF capacitors atthe input to the FET-input op-amp buffers in ZX03 and ZX04. This RC network causes changes in any particular control voltage

MAIN BOARD: (CONTINUED)

to be smoothed out, rather than being sudden steps. The time constant of the RC networks is somewhere around 8ms.

If a sudden change in a control voltage is needed, the selected channel's FAST(N)/ line goes low at the same time as the SLOW(N)/ line. The DAC voltage is thus delivered equally to both capacitors and the smoothing effect is overridden.

Voice 5 has an additional sample and hold consisting of capacitor C12 and buffer Z503C, used for the master volume. In the other voices the input to ZX03C is shorted to ground.

ZX05A and B is a dual oscillator chip. Each half accepts a low-level pitch control voltage (scaled at roughly 18mV/octave) on pin 7 or 12, generates a triangle wave on the capacitor connected to pin 6 or 13, a buffered triangle wave on pin 5 or 14, and a buffered sawtooth on pin 2 or 17. Pins 8 and 11 are reference current inputs to the exponential converters inside the chip. Pins 4 and 15 are internal reference voltages that require external bypassing. Pins 1, 9 and 18 are supply pins. Pin 10 is the temperature compensating voltage generated by the chip; this voltage is nominally +2.5V, but is proportional to the temperature of the chip. Pin 16 is a soft sync input, which isn't used, and pin 3 is a hard sync input, which forces ZX05A to the beginning of a cycle whenever a negative pulse is applied. This pulse is derived by differentiating the sawtooth from the other side of the chip through a tiny capacitor (CX23). Switch ZX08B grounds this signal, preventing or allowing the sync.

The sawteeth are converted into pulses by comparators ZX06A and ZX06B. The pulse width is determined by a control voltage in the nominal range of -4V to +4V. The comparators have a bit of positive feedback to keep them from oscillating. The pulse outputs are mixed in with the pulse control voltage to yeild a DC-free signal. If switch ZX07A or ZX08A is on, the sawtooth signal will be mixed in as well. ZX07C switches in the noise signal as well and ZX07B replaces the upper oscillator signal with the digital ring modulation of the pulses from the two oscillators. The ring modulator is made from one exclusive-or gate from either Z70 or Z71 (located in the area between channels 3 and 4).

The oscillator signals feed into signal processor ZX09 on pins 6 and 7. These inputs are low-level inputs, so the 510ohm resistors on these inputs attenuate the oscillator signals. Pins 5 and 8 adjust the levels of the signals; the A signal is always on, and the B signal is turned off when the ring mod is selected.

The signal processor includes a four-pole low-pass filter, using capacitors CX25 through CX27. The filter is tuned by the CUTOFF

MAIN BOARD: (CONTINUED)

signal, attenuated to an 18mv/octave level and applied to pin 15. The resonance is controlled by the voltage on pin 10, which is determined by three digital bits: RESA, RESB, and RESC. The diodes in the resonance control network assure that there will be a large jump between the maximum resonance control voltage (level 6) and the self-oscillation control voltage (level 7).

The filter output is on pin 17. It feeds back into the resonance circuit on pin 11 and forward into the output volume VCA on pin 12. The volume level is controlled by the level on pin 13 RX49 and CX29 slow changes in the volume down just enough to prevent harsh clicks. The final output is a current that is steered by ZX08C into either MAIN OUT or ALT OUT.

ZX00 is the latch that holds the various digital control bits for the voice. It is written to by generating a WR SYN(N)/ strobe (from) Z32). It is only written when one of the parameters contained in it is changed.

CONTROL PANELS:

Main Board Interface, I/O Strobe Decoder

The Left Control Panel Board and Right Control Panel are best explained together, as the left one is really just an extension of the right one. The cable from the Main Board connects to the right board and that is where the address decoder for all control panel devices is located.

Z4 on the right board takes in three address bits, called A0, A1 and A2. These actually connect to address bus bits 1, 2 and 3 coming from the computer. This is because the computer has a 16-bit wide data bus, allowing it to read and write two consecutive memory or I/O locations at the same time; thus, bit 0 of the address bus selectes which half of the data bus the data transfer takes place on. Since all I/O devices are on the low half of the data bus, all I/O addresses are even numbers, and address bit 0 is always a 0.

All data to and from the panel flows across an 8-bit bidirectional data bus, labelled B0 through B7. When the computer is outputting a byte of data to a device on the control panel these lines are driven by a buffer on the Main Board. When the computer is inputting a byte of data from a device on the control panel these lines are driven by that device. When the computer is neither outputting to or inputting from the control panel, all eight data lines, as well as the address lines, are tri-stated.

CONTROL PANELS: (CONTINUED)

Z4 also accepts a strobe input called STB. This is a postive-going pulse that occurs whenever the computer reads from or writes to an I/O device on the panel. Whenever the computer performs a bus cycle that refers to a panel I/O device, the address lines (and data lines, if the operation is an output) are first driven with the correct information. Once this has stabilized the strobe pulse is generated. When the strobe pulse completes, the address and data lines are tri-stated again. The width of the strobe pulse is normally 250ns with an 8MHz clock (16MHz crystal) or 333ns with a 6MHz clock (12MHz crystal).

Z4 steers the strobe pulse to the appropriate device. Four outputs of this chip are used, numbered 0 through 3, corresponding to I/O addresses 0180, 0182, 0184 and 0186 (hex). No specific indication is given to the panel devices of whether an operation is input or an output. This, however, is not a problem, as each device has a separate I/O address and the computer never attempts to input from an output device or vice versa.

Panel Switch I/O

Reading the state of the membrane switches requires the use of two I/O devices. The switches themselves are organized into a matrix containing eight banks of eight switches each and five switch positions in the matrix are not used. The computer reads one bank of switches at a time by outputting a switch bank number (binary 00000000 to 00000111) to the I/O location 0184. The number 2 output of the strobe decoder (Z4-13) generates an active-low pulse which latches the bank number into Z2. The output of Z2 is connected to Z1 and causes one of its eight outputs to turn on. The outputs of this chip are open collectors to ground, so the selected output is connected to ground while the remaining outputs float.

Outputs 0, 1 and 2 of Z1 connect to the switches in banks 0, 1 and 2 on the left membrane switch, while outputs 3 through 7 connect to the switches in banks 3 through 7 on the right membrane switch. When a switch is closed, one of these outputs, designated SWSTBn/, will be electrically connected to one of the switch data lines, designated SWn/. Normally all eight of these lines are pulled high by R9 through R16, but a closed switch in the selected bank will pull one of these lines low.

The computer reads in the state of the switches in the selected bank by performing an input from I/O location 0186. This causes an active-low pulse to be generated by output 3 of the strobe decoder (Z4-12) and this turns on Z3, causing the eight data bits to appear on the data lines B0 through B7 where the computer

CONTROL PANELS: (CONTINUED)

can read them.

The software in the computer inputs all eight banks of switches in a short burst and this burst is repeated roughly every 12ms in an 8MHz system or 20ms in a 6MHz system. When the computer sees that a switch is closed that wasn't closed on the previous scan, it takes action based on that switch.

LED Drivers

Each LED is driven directly by one of the outputs of one of the 74LS164 shift registers. These chips happen to have about the right output current for LED's and are very cost-effective. Each data line, B0 through B7, is connected to the data input of a shift register. Five of these are on the right board (Z7 through Z11) and the other three are on the left board(Z5 through Z7). All chips are clocked by the number 1 strobe from the I/O decoder.

When the computer outputs a byte to I/O location 0182, each bit in that byte appears on pin 3 of one of the shift registers and the bits in the shift registers move up one position. The data that were previously in the last bit positions, pins 13, are lost. The computer has a special instruction that allows repetetive outputs to an I/O location at full speed and this instruction is used to output eight bytes to location 0182. This causes all the data in the shift registers to be flushed and replaced with new data.

The strobe pulses that output to the LED shift registers occur every 1us in an 8MHz system or every 1.33us in a 6MHz system. Between the first and last outputs, the contents of the LEDs is incorrect, but this condition only lasts 7us in a 8MHz system, or 9.33us in a 6MHz system, and is therefore all but invisible to the human eye. The operation of outputting to all the LEDs takes place whenever any single LED or combination of LEDs needs to be turned on or off by the computer.

Slider Mux

This section selects the voltage from one of the sliders or other analog inputs and connects it to the ADC line going back to the A/D converter on the Main Board. There are twenty-four analog inputs in the system and each one is selected by outputting a code to I/O location 0180. This causes output 0 of the strobe decoder (Z4-15) to generate an active-low pulse. The code is latched into Z6, which presents it to the mux (multiplexer) circuitry.

CONTROL PANELS: (CONTINUED)

The mux consists of three 8-input mux chips; Z5 on the right board and Z3 and Z4 on the left board. The three lsbs of the code go to the A, B and C inputs on the mux chips, selecting one of the eight channels within each mux. The 3 msbs of the code each go to the enable input on one of the mux chips. One of the muxes is enabled by making one of these bits a 0 and the other two bits 1's.

Thus, exactly one of the analog switches in one of the mux chips will be turned on and the selected voltage will drive the ADC line. The sliders hang between the ADC GND and ADC REF lines, which are at 0V and +5V, as this is the range expected by the A/D converter.

Analog Input Buffers

Four analog inputs come from off the control panel. Buffers Z1A, Z1B, Z2A and Z2B are provided for these on the left panel. The LEVER 1 and LEVER 2 inputs are voltages that are derived from rotary pots in the lever assembly. Since only a small portion of the pot rotation is used, these pots are supplied with +12V, and the voltage they produce is roughly +1V to +4V, resting at around +2.5V. The PEDAL input expects to connect to a 100K pot to ground inside the optional foot pedal. This results in roughly a 0V to +4V range at the input to its buffer. The CMOS RAM battery is connected to the BATT line that comes from the main board through the right panel and is nominally around +3V.

Note that the buffer amps include transistors. Although the outputs come from the collectors, they are actually functioning in their inverted configuration as emitter followers. In this configuration, the emitters act as collectors and vice versa; the reason for this is historical and not very interesting. The circuits would work just as well with transistors connected normally. The main point of these transistors is that they allow the outputs to go exactly up to +5V, at which point they saturate; or down to 0V, at which point they cut off. Therefore, there is no danger of blowing out the mux inputs, even if the pedal is unplugged or a lever is mechanically misadjusted and producing more than +5V.

Note also that the buffers are FET input. This is particularly necessary in the case of the battery voltage buffer. Even when the power to these buffers is removed the input will not draw current even though it is sitting at around +3V.

The buffers have a zener diode in series with their minus supply to limit how far negative the output of the op-amp can go if the inputs should go negative. This is a precaution that is probably

CONTROL PANELS: (CONTINUED)

unnecessary.

Power System

Most power to the panel is carried by the DIG GND, +5V DIG, ANA GND, +12V ANA and -12V ANA. The LEDs are given their own power system, LED GND and LED +5V, so that their high current drain will not upset the ground reference used by the data, addresses and strobe. The sliders are also given a separate power system, ADC GND and ADC REF, so that varying current consumption in other parts of the system will not introduce jitter into the slider position measurements.

POWER SUPPLY:

AC Input

The AC power comes through a three-conductor grounded line cord. The chassis is connected to earth ground for the protection of the user and to minimize radio-frequency emissions. The receptacle on the rear panel includes an integral line filter connected to chassis ground. The power switch is a double pole switch that completely isolates the unit from the line when turned off, even if the grounding system has been defeated.

Primary Board

This small board to the left of the transformer includes a fuse, a voltage selection switch, and two MOV's (medal-oxide varistors) to clamp line transients. The switch connects the two transformer's primaries in parallel for 100V to 130V operation or in series for 200V to 260V operation. If you change the position of this switch, you must also change the fuse value. 3/4A or 800mA is the correct rating for the low-voltage setting and 3/8A or 400mA is correct for the high-voltage setting.

Semko Primary Board

This board uses a SEMKO approved fuse and has jumpers installed in place of the voltage selection switch. The transformer primaries are permanently in series.

Transformer

The power transformer has two identical primaries (as mentioned

POWER SUPPLY: (CONTINUED)

above) and two different secondaries, one for the digital supply and the other for the analog supply. It also has an electrostatic shield between the two that is connected to chassis ground for added protection and interference suppression. In the SEMKO version each secondary is fused on each side.

Analog Supplies

CR1 through CR4 rectify the voltage from one of the transformer secondaries and C1 and C2 filter it. C5 and C6 provide better high-frequency filtering, necessary for stable operation of the regulators. Four regulators are provided, all of them "three-terminal" types. The +12V, -12V and -5V supplies are fixed and the +5V supply is adjustable. Z3, a LM317, is a 1.2V regulator whose "ground" terminal (pin 1) draws very little current. By connecting pin 1 to a feedback network, the device can regulate to any voltage greater than +1.2V. The output voltage is made adjustable by making the feedback network adjustable.

C10, C12 and C15 provide additional filtering and stabilization; R26 provides a minimum load so that the negative regulators will operate correctly when the Main Board is disconnected.

Digital Supply

CR5 and CR6 rectify the voltage from the other transformer secondary and C3 and C13 filter it. C15 filters the high harmonics of the diode switching to minimize interference generation. Z5 is an adjustable regulator that works on the same principle is Z3, except that has a much higher power rating. C14 provides output stabilization. At the output of the supply, the digital ground is connected directly to the analog ground and through a 1M resistor to the chassis. This is the only place in the system the gounds are connected.

AC OK CIRCUIT

An additional rectifier, CR7 and CR8, is connected to the analog supply secondary and it is filtered by C4. This supply generates a positive voltage that is loaded to a negative voltage through R10. The time constant of C4 and R10 is such that when the power is shut off the voltage on C4 drops toward zero very quickly. The remaining resistors and transistors form a crude comparator circuit with hysteresis. When the AC input is turned on, the AC OK signal goes high pretty much with the +5 DIG supply that powers it. When the AC input is turned off, the AC OK signal goes low within a cycle or two of the AC input long before the +5 DIG

POWER SUPPLY: (CONTINUED)

supply goes out of regulation. This signal interrupts the computer on the Main Board allowing it to "put itself to sleep" in an orderly manner.

DC OK Circuit

This circuit contains a precision 1.2V reference diode and a comparator circuit with an adjustable threshold and a small amound of hysteresis. Its purpose is to indicate whether or not the +5V DIG supply is within regulation. The comparator must be set so that it switches off when the supply falls to about +4.80V or 4.85V. When so set, the comparator will switch on when the supply rises to about +4.90V. The LED, CR10, allows the service technician to see the state of the output while adjusting the comparator.

The signal produced by this circuit, DC OK, connects to the RESET input on the computer, switches the CMOS RAM between battery and line supply, and gates the chip select lines to the CMOS RAM. When the Polaris is turned on the computer will not be allowed to function until the supply is within regulation and DC OK goes high. When the Polaris is shut off the AC OK signal will fall, as described above, and then the DC OK signal will fall, halting the computer.

OUTPUT BOARD:

Tune Buffer

When a channel is being tuned by the computer the output current produced by that channel alone is switched into the ALT OUT input to this board. Z1 converts this to a voltage whose amplitude is sufficient to drive the input to the timer circuit on the main board, but not so high that it will clip. The 100ohm resistors, R9 and R11, simply isolate the buffer input and output from the cable capacitance.

Master Volume

Normally, all channels' outputs connect to the MAIN OUT input to this board. In addition, the outputs of the click generators and cassette monitor circuits combine to drive the DATA AUD input. This DATA AUD signal from the main board has a +2.5V DC bias, which sets the bias for the input to Z2. Since the channel outputs are current outputs, they don't mind operating into this voltage level.

OUTPUT BOARD: (CONTINUED)

The sum of all the channel output currents pass through R5, which converts them into a small voltage, say 30mV or 40mV p-p. This voltage drives the input to Z2. Since the signal from the Main Board is a current, R4 has no effect on the voltage seen at the input to Z2, but it does help to reduce the noise pickup by increasing the impedance on the MAIN OUT line. R3 couples the DATA AUD signal in as well, C3 filters high-frequency trash that is everywhere in computer circuits, and C2 provides AC ground and DC blocking.

Z2 is an "operational transconductance amplifier" or OTA. It takes its input, which must be small, and multiplies it by the bias current fed into pin 5. The result appears as a signal current from pin 6. The bias current input looks like a diode to the minus rail of the chip. R14 and Q1 provide level shifting so that the computer can use a 0 to +5V signal to control the gain of this circuit. C4 and R6 provide filtering to the volume control signal, as any changes in it occur in discrete steps rather than smoothly. C5 provides additional filtering of any noise in the area, as pin 5 is fairly sensitive.

Headphone & Line Amplifier

The output of Z2 is ideally a bipolar current signal with no DC component. However, due to offset error in its input, there is usually a slight DC component. R7 and C6 separate the DC and AC. Z2-6 should be between -2V and +2V; if it is outside that range, either there is DC at its input or it is a bad chip.

At any rate, the AC current passes through C6 into current-to-voltage converter Z3A. The fact that the signal passes as a current from the high-impedance output of Z2 to the low-impedance input of Z3A allows the final output to derive its ground reference from whatever external device it is connected to. The output jacks are floating with respect to the chassis and their sleeves are connected to the LINE RETURN, which is the ground reference to the output circuit. Thus, if there is a small amount of hum on the external device's ground, the hum will be duplicated at the LINE OUT, making it invisible to the external device.

The voltage at the output of Z3A is buffered by voltage followers Z3B, and Z3D. All four outputs are mixed through four 4.7 ohm resistors to provide the actual final output of the circuit. Offsets in the op-amps cause quiescent currents to flow through these, but these currents are generally less than a milliamp. C13 helps stabilize the circuit by allowing high frequencies to be fed back directly without having to go through the remaining op-amp sections.

OUTPUT BOARD: (CONTINUED)

The purpose of the extra buffering is so that the circuit can directly drive headphones. When driving the line output an additional 100ohm resistor is connected in series with the output to isolate the output from the potentially large capacitive load that a long audio cable would provide. R8 provides a ground reference for use when the external device provides none of its own, such as when headphones are used or when the output is transformer coupled at the other end.

Although this circuit can tolerate some common mode voltage at its output, too much would damage the op-amp Z3A. To guard against this, diodes CR1 and CR2 keep the LINE RETURN from getting more than a half volt or so from the chassis ground. C1 filters computer noise picked up in the output circuit.

Note that this output circuit is not designed to be used to drive a line output and headphones at the same time. If you try this you will find that the current drain of the headphones may cause clipping at volume levels that are too soft at the line output. In addition, any common mode voltage present at the device connected to the line output will be injected into the circuit and heard full-strength in the headphones.

This entire board is rather sensitive to noise pickup. C9, C10, C11, and C12 bypass the power supply and C2, C3, C5, and C7, along with the shielded input wires and careful layout, reduce the noise picked up from the air.

SECTION 4: DISASSEMBLY

MAJOR COMPONENT LOCATIONS:

As can be seen in figure 4-1, most of the electronic components are on the main board. Six identical synthesizer voices are on the right and the computer with expandable memory on the left. Notice that all of the chips on this board are socketed, a great benefit to expedient troubleshooting. Six "satellite" boards contain the hardware for the two control panels, output amplifiers, primary board, secondary board and, of course, the keyboard.

OPENING FOR SERVICE:

Most servicing may be accomplished by opening the sloping panel. Back off on screws 1 and 2 underneath the Polaris shown in figure 4-2. These screws do not come all the way out, but it will be obvious to you when they disengage. Next, remove screws 3 through 6. The panel may be raised and carefully positioned behind the main chassis with the bracket propped against the chassis as shown in figure 4-1.

KEYBOARD REMOVAL:

Certain components on the main board are covered by part of the keyboard. They may be accessed by gently lifting the keyboard and positioning it in front of the main board. To do this, remove inside screws 7 through 9 (fig. 4-1) and bottom screws 10 through 13 (fig. 4-2). CAUTION: watch for keyboard spacer shims.

REPLACING KEYS:

Individual keys may be removed by pressing down on the rear top key shaft while simultaneously pulling the key toward you. Certain natural keys must be removed before pulling a sharp key. Watch for the keyspring as it may pop off upon removing a key. There are two different keysprings, natural and sharp. Since they have different tension values they are not interchangeable.

REPLACING BATTERIES:

Although the capacitor on the battery holder retains its charge for a minute or more, to ensure no interruption of power to the memory chips the batteries should be changed with the power on. Alkaline "D" cells should be used. Refer to figure 4-1 for location of batteries.

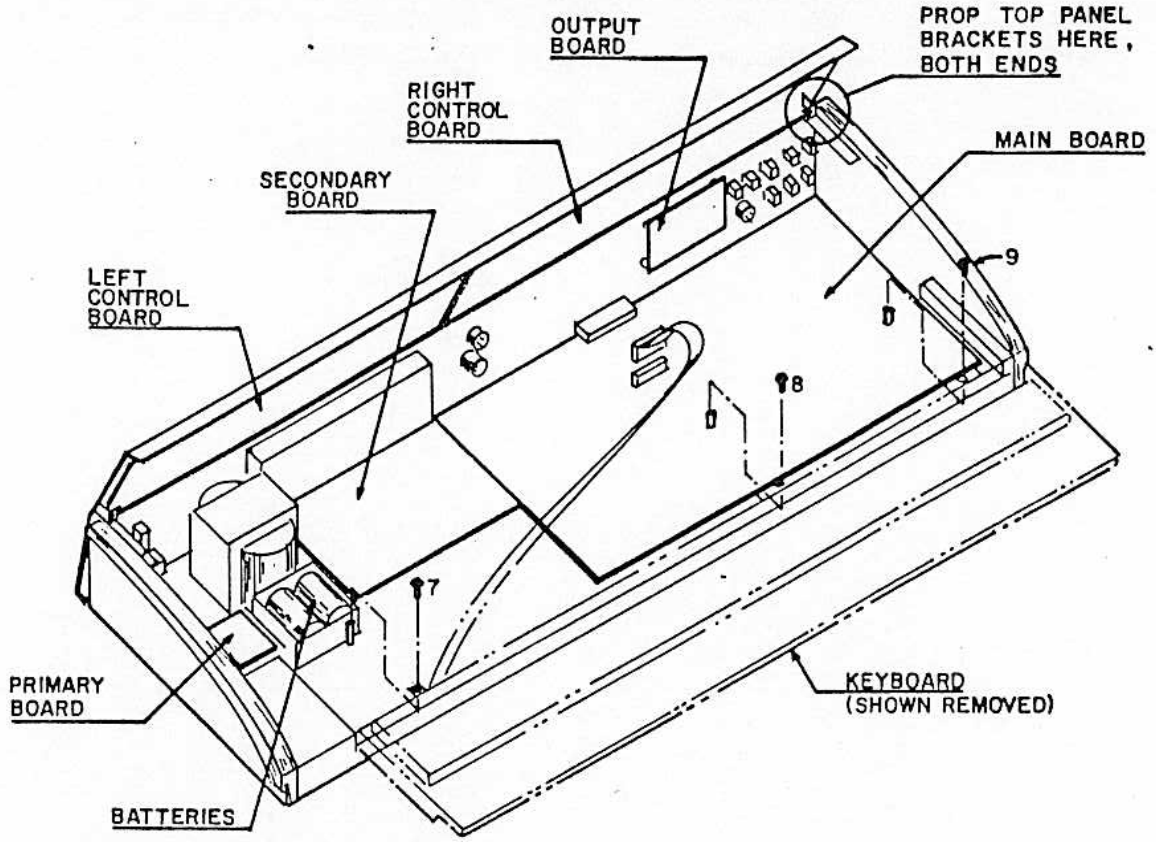


FIGURE 4-1

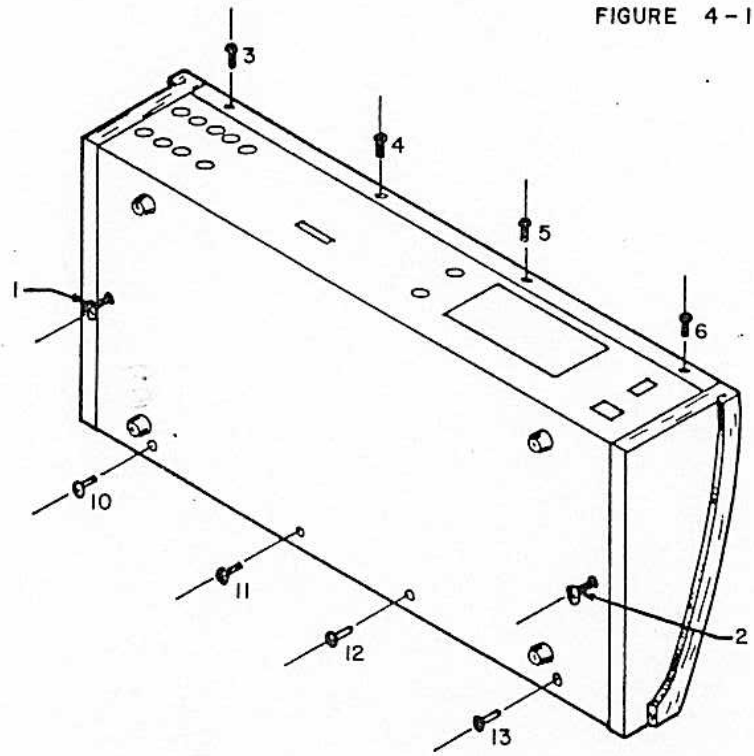


FIGURE 4-2

SECTION 5: DIAGNOSTICS

THE "SCRATCH PATCH":

Prior to making any adjustments on the Polaris a "scratch patch" should be established. The "scratch program" is also useful in trouble analysis, since you can be sure there is nothing in the program that will mysteriously affect the sound.

Any program erased from memory will revert to default values thereby establishing the "scratch program". So you need to erase a program, but what if you are working on a Polaris with 132 programs stored? No problem! Simply use the swap feature. The following sequence works fine:

1. Select progam A1. (A1 is now in the workspace).
2. Press upper function - erase prog. - A1 (Scratch now in A1).
3. Press upper function - swap prog. - A1 (Scratch now in workspace, A1 now back in A1).

You should hear a raspy sounding sawtooth, characteristic of the scratch program when keyed. This is the starting point for most diagnosing and adjusting.

CHANNEL ENABLE/DISABLE:

One of the more important functions in troubleshooting is the ability to listen to one voice at a time, or shut off voices one at a time to locate an offending sound. Simply press LOWER FUNCTION - E (CHANNEL CK). Switches 1 through 6 now control the 6 voices. The LED's, obviously, indicate the on/off status of the corresponding channel. Switch 7 controls the channel most recently played.

OSCILLATOR ENABLE/DISABLE:

Along the same line of reasoning, you may want to disable the number 1 oscillators or number 2 oscillators. Select pulse and set the pulse width to minimum (0%) or maximum (100%) for either oscillator 1 or oscillator 2.

DIAGNOSTIC READOUTS:

LOWER FUNCTION - D (DIAGNOSTICS) - 1: Displays charge on battery in right column of LEDs in assignable control section. Expect 4 or 5 LED's to light for a normal condition. Replace the battery cells if less than 2 LED's light. If all 7 LED's light, it may mean that the capacitor on the battery holder has charged to more than the normal 3.2V. Likely, the capacitor will have

DIAGNOSTIC READOUTS: (CONTINUED)

charged up to +5V indicating an open connection between a cell and the holder terminal. Turning off the Polaris for a short time will not dump memory; off for a lengthy time, clearly will.

LOWER FUNCTION - D (DIAGNOSTICS) - 2: Displays revision level of EPROMs by a flashing number LED. Example: flashing LED number 5 indicates revision 5 software.

LOWER FUNCTION - D (DIAGNOSTICS) - 3: Turns on all LED's. Useful for checking LED's and loading the digital +5V supply by drawing maximum current. Voltage levels and ripple should always be checked with the supply under full load.

LOWER FUNCTION - D (DIAGNOSTICS) - 4: Turns on the LED above the master slider when the master slider is positioned to produce a value of 255. This checks out the range of the A/D converter.

LOWER FUNCTION - D (DIAGNOSTICS) - 12, STOP: Erases all RAM and resets the microprocessor. Everything in RAM is wiped out; all adjustments, programs, and sequences. The Polaris must be reloaded and all factory adjustments must be performed following this particular function. Generally, this should be used whenever EPROM's are changed to a different revision.

LOWER FUNCTION - 10: MIDI reset. Sends a MIDI reset byte over the MIDI interface to reset any external device that recognizes the standard MIDI reset (hexadecimal FF).

LOWER FUNCTION - 11: Warm reset. Clears minor glitches. Example: A surge on the power lines can cause impulse or oscillatory noise on the 120V mains. This may result in unusual glitches such as self-sustaining notes, etc. Use this function to clear these kinds of problems without clearing any configuration parameters you may have set up through the software controlled switches.

LOWER FUNCTION - 12: Cold reset. This is a major reset, similar to turning off the power and turning it back on. It will clear configuration parameters and set them to their default condition.

HIDDEN FUNCTIONS QUICK REFERENCE:

The following is a listing reprinted from the Owner's Manual, providedhere as a quick reference to hidden functions. It is not intended to be used as a comprehensive guide, rather, every service center should have on hand an actual Owner's Manual. The terms "LOWER FUNCTION" and "UPPER FUNCTION" are designated by "LF" and "UF" respectively.

HIDDEN FUNCTIONS QUICK REFERENCE: (CONTINUED)

RESETS:

LF, 10: MIDI reset.
LF, 11: Warm reset.
LF, 12: Cold reset.
LF, D, 12, STOP: Erase and reset all.

ADJUSTMENTS:

LF, A, 1: Stop mode click volume.
LF, A, 2: Record mode click volume.
LF, A, 3: Play mode click volume.
LF, A, 4: Switch press click volume.
LF, A, 5: Error honk volume.

INTERFACE:

LF, B, 1: Main local control switch.
LF, B, 2: Link local control switch.
LF, B, 3: Sequencer local control switch.
LF, B, 4: Main Chroma out switch.
LF, B, 5: Link Chroma out switch.
LF, B, 6: Sequencer Chroma out switch.
LF, B, 7: Main MIDI in switch.
LF, B, 8: Link MIDI in switch.
LF, B, 9: Sequencer MIDI in switch.
LF, B, 10: Main MIDI out switch.
LF, B, 11: Link MIDI out switch.
LF, B, 12: Sequencer MIDI out switch.

CASSETTE:

LF, C, 1: Cassette load monitor.
LF, C, 2: Cassette save monitor.
LF, C, 3: Cassette input level. Off = audio, on = digital.
LF, C, 4: Cassette output level. Off = low, on = high.
LF, C, 5: Chroma program switch.
LF, C, 6: MIDI program switch.
LF, C, 7: Chroma panel switch.
LF, C, 8: MIDI panel switch.
LF, C, 9: MIDI omni mode.
LF, C, 10: MIDI mono mode.
LF, C, 11: Main workspace program sent out over Chroma interface.
LF, C, 12: Main workspace program sent out over MIDI interface.

SECTION 5: DIAGNOSTICS

HIDDEN FUNCTIONS QUICK REFERENCE: (CONTINUED)

DIAGNOSTICS:

LF, D, 1: Charge on battery.
LF, D, 2: Revision level of EPROMs.
LF, D, 3: All LEDs on.
LF, D, 4: ADC range.

CHANNEL CHECK:

LF, E, 1: Channel 1 enable/disable.
LF, E, 2: Channel 2 enable/disable.
LF, E, 3: Channel 3 enable/disable.
LF, E, 4: Channel 4 enable/disable.
LF, E, 5: Channel 5 enable/disable.
LF, E, 6: Channel 6 enable/disable.
LF, E, 7: Most recently played channel enable/disable.

METRONOME:

LF, H, 1: Metronome normal.
LF, H, 2: Metronome master, pulses out sync interface.
LF, H, 3: Metronome master, timing bytes out MIDI interface.
LF, H, 4: Metronome master, pulses out sync, timing out MIDI.
LF, H, 5: Metronome slaved to sync input.
LF, H, 6: Metronome slaved to sync, pulses out sync.
LF, H, 7: Metronome slaved to sync, timing out MIDI.
LF, H, 8: Metronome slaved to sync, sync pulse & MIDI timing out
LF, H, 9: Metronome slaved to MIDI input.
LF, H, 10: Metronome slaved to MIDI, sync pulses out.
LF, H, 11: Metronome slaved to MIDI, MIDI timing bytes out.
LF, H, 12: Metronome slaved to MIDI, sync pulse & MIDI timing out

SYNC INPUT:

LF, I, 1: Sync in 12 clocks/beat.
LF, I, 2: Sync in 24 clocks/beat.
LF, I, 3: Sync in 48 clocks/beat.
LF, I, 4: Sync in 96 clocks/beat.
LF, I, 5: Sync in 192 clocks/beat.
LF, I, 6: Toggles polarity of sync in trigger.
LF, I, 12: Toggles level of sync in.

HIDDEN FUNCTIONS QUICK REFERENCE: (CONTINUED)

SYNC OUTPUT:

LF, J, 1: Sync out 12 clocks/beat.
LF, J, 2: Sync out 24 clocks/beat.
LF, J, 3: Sync out 48 clocks/beat.
LF, J, 4: Sync out 96 clocks/beat.
LF, J, 5: Sync out 192 clocks/beat.
LF, J, 6: Toggles polarity of sync out.
LF, J, 7: Sync out rate limit 1200Hz.
LF, J, 8: Sync out rate limit 600Hz.
LF, J, 9: Sync out rate limit 400Hz.
LF, J, 10: Sync out rate limit 300Hz.
LF, J, 11: Sync out rate limit 200Hz.
LF, J, 12: Sync out rate limit 150Hz.

MIDI CHANNEL:

LF, K, 1 through 6: MIDI basic channel (b) = sum of these.
LF, K, 7: MIDI in, no extra channels.
LF, K, 8: MIDI in, extra channel b+3.
LF, K, 9: MIDI in, extra channels b+3 & b+4.
LF, K, 10: MIDI in, extra channels b+3, b+4 & b+5.
LF, K, 11: MIDI in, extra channels b+3 through b+6.
LF, K, 12: MIDI in, extra channels b+3 through b+7.

SEQUENCES:

UF, A: Flashes currently selected sequence number.
UF, B: Chains current sequence to sequence specified by no.(1-12)
UF, C: Toggles cue flag at end of current sequence.
UF, D: Sets sequence tempo to metronome if on; erases if off.
UF, E: Select (A-K, 1-12) initial program for current sequence.
UF, F: Select sequence (1-12).
UF, G: Erase sequence (1-12).
UF, H: Swap current sequence with sequence (1-12).
UF, I: Save current sequence on tape.
UF, J: Save all sequences on tape.
UF, K: Loads one sequence over current sequence from tape.

PROGRAMS:

UF, 1: Store current program into (A-K, 1-12).
UF, 2: Erase program from (A-K, 1-12).
UF, 3: Swap current program with program (A-K, 1-12).
UF, 4: Save current program on tape.
UF, 5: Save all programs on tape.
UF, 6: Loads one program from tape into main workspace.
UF, 7: Displays in Assignable Control approximate memory used.
UF, 10: Toggles cassette motor control.
UF, 11: Runs tape to verify. Any error stops tape, sounds honk.
UF, 12: Runs tape to load programs and sequences.

SECTION 6: ADJUSTMENTS AND CHECKOUT

This section outlines both hardware and software adjustments. The hardware adjustments involve measurements which require a reference ground. The main ground test point is located on the main PC board below Z63, just to the right of connector J14. This is a fine reference for troubleshooting digital circuits, but when checking a supply, especially for noise, use the actual supply reference ground. Stay away from the ground side of filter capacitors, because of the heavy currents, and from chassis ground, which is isolated by 1M ohm. Long ground leads pick up extra noise; use a local ground from the shielded scope probe instead.

DIGITAL +5V LEVEL:

Prior to any adjustments load the supply by pressing LOWER FUNCTION - D - 3. Measure the +5V digital level between P3 pin 3 (orange wire) and pin 2 (red wire). Adjust R9 for +5.00V (the tolerance is 10mV). Check to see that all 60 LEDs are lit. During normal full load operation the noise level on the output should be approximately 20mV P-P. The ripple on the input to Z5 should be about 1.25V P-P at a DC level of an unregulated 13V. Since this is a full wave supply, the ripple frequency should be 120Hz. (having a period of 8.33 msec). Press LOWER FUNCTION to return panel to normal operation.

REFERENCE +5V LEVEL:

Measure the +5V reference between P4 pin 1 (brown wire) and pin 6 (blue wire). Adjust R5 for +5.00V to within 10mV. The noise level on this output is normally about 1mV P-P; too small to be seen through the noise picked up from the air by most scope probes. The ripple at the input to Z1 should be approximately 2V P-P at a DC level of an unregulated 23V. Since this is derived from a full wave bridge, the period should be 8.3 msec.

DC OK THRESHOLD:

The factory setting for the DC OK threshold requires the use of a rather elaborate test circuit; however, it is sufficient in the field to simply back off on R17 to minimum (full CCW), then turn it clockwise until LED CR10 lights. The nominal DC level out at DC OK (P3 pin 1, brown wire) is +3V.

Late serial numbers use a different secondary board with a modified DC OK circuit. On these no adjustment is necessary or provided. The nominal DC level out at DC OK (P3 pin 1, brown wire) is +5V.

SECTION 6: ADJUSTMENTS AND CHECKOUT

ADC RANGE:

Push the Master (leftmost) slider up to maximum and pull all the other sliders to minimum. Press LOWER FUNCTION D - 4 and watch the LED in the Master section of the panel (labled VOLUME /TUNE). Turn R45 clockwise to maximum, then back off counterclockwise until the LED lights. Continue turning CCW 5 degrees beyond this point. Press LOWER FUNCTION to return panel to normal operation.

DAC NULL:

As stated in the circuit descriptions of Section 3, there must be no DC offset going into the differential input of Z58 if the accuracy of the DAC chip is to be upheld. This input must be within 200uV of 0V. Use a 3-1/2 or 4 digit meter with 100uV resolution MINIMUM! Using an analog meter to measure this is like trying to analyze nanosecond duration pulses in a computer system using a light bulb instead of a fast scope. With your DVM floating in respect to ground, measure between the test points TP1 and TP2 on the main PC board. Adjust R46 until the meter reads to within 100uV of 0V (-0.0001 to +0.0001V). This is a critical adjustment and is quite sensitive. Check your meter with the test leads shorted to be sure it reads 0.0000 prior to making the adjustment.

LEVER POSITION:

Measure the DC voltage between the center terminal and ground of each potentiometer in the lever assembly. With the lever at rest (center position), the voltage should read between 2V and 3V. If either is out of range, use a thin 1/2 inch wrench to loosen the nut on the potentiometer. Rotate the potentiometer, keeping the lever centered, until the voltage reads 2.5V and tighten the nut.

The following adjustments are software oriented, using the computer built into the Polaris. No external test equipment is needed.

TUNING:

The Polaris has good tuning stability and resolution. Further, it remembers exactly how it was tuned when last shut off; so, when turned on, it does not automatically tune itself. Still, there will be times when it needs tuning; after a change in temperature for example. Press LOWER FUNCTION - TUNE ALL. The Polaris will tune the 6 voices in about 8 seconds. During this process, the tune LED in the Master section of the panel will blink 6

TUNING: (CONTINUED)

times, provided that each voice is capable of being tuned. If you see that the LED blinks less than 6 times, it is likely a voice cannot be tuned and it will automatically be turned off by the computer. Individual voices may be tuned by pressing UPPER FUNCTION - TUNE ONE. This instructs the computer to tune only the most recently played voice.

The following adjustments can be made only by first going into the adjustment mode. Press LOWER FUNCTION - A - (ADJUSTMENTS) to enter the adjustment mode followed by the number for the specific adjustment. The master slider is assigned and used to complete many of the adjustments. After completing the adjustments, press LOWER FUNCTION a second time to return the panel to normal operation.

VOLUME:

Press 1 and move the master slider to adjust the volume of the metronome click for the stop mode of the sequencer. Normally, this will be set to minimum volume by positioning the master slider all the way down.

Press 2 and move the master slider to adjust the volume of the metronome click for the record mode of the sequencer. This usually will be set to maximum.

Press 3 and move the master slider to adjust the volume of the metronome click for the play mode of the sequencer. This usually will be set to minimum.

Press 4 and move the master slider to adjust the volume of the click generated whenever a panel switch is pressed. This usually will be set to minimum.

Press 5 and move the master slider to adjust the volume of the error honk. Normally, this will be set to maximum.

LEVER RANGE:

Press 7 and move the levers (the two levers on the left cheeckblock, not the sliders) through their entire mechanical range. This will enable the computer to establish the correct lever range provided they were in their center positions prior to pressing switch number 7.

SECTION 6: ADJUSTMENTS AND CHECKOUT

PEDAL RANGE:

Press 8 and move the pedal (if pedal option is used) through its entire mechanical range. The computer will establish the correct electrical excursions from this. If pedals are ever changed this adjustment will have to be done with the new pedal.

VOLUME OFFSET:

The volume offset on each VCA must be trimmed to properly shape the volume envelope. When misadjusted notes may sustain or end abruptly.

Before entering this mode put a scratch program in the main workspace. Use the sequence outlined under "scratch patch" in section 5 of this manual if you need help. You will have to temporarily leave the adjustments mode by pressing LOWER FUNCTION to do this, then re-enter the adjustments mode using LOWER FUNCTION A. Preset the volume by setting the assignable control volume to 1/4 and the master slider volume to maximum. The LED above the master slider must be OFF to be in the volume mode, if on the tune mode is activated.

Press 9 to enter the volume offset mode and move the master slider down to 1/8 on. Play 6 different notes, 1 at a time. After releasing each note move the master slider up until you hear the note bleeding through, then back off carefully on the slider until it just disappears.

KEY SENSITIVITY:

Individual keys may be adjusted for touch sensitivity. Before entering this mode select a touch sensitive program by exiting the adjustments mode(LF), then return to the adjustments mode (LF-A).

Press 10 to enter the key sensitivity mode. If one or more keys feels too sensitive, or not sensitive enough, play the key repeatedly and use the master slider to adjust its sensitivity.

CONFIGURATION PARAMETERS:

The following outline provides the initialized configuration parameters as set on a new unit at the factory. In general, when a Polaris is serviced, these parameters should be set to the initial configuration.

CONFIGURATION PARAMETERS: (CONTINUED)

Press B to enter the computer interface configuration mode. Turn on LED's 1, 2, 3, 7, 8, 9, 10, 11 and 12. Turn off LED's 4, 5 and 6.

Press C to enter the cassette interface configuration mode. Turn on LED's 1, 2 and 9. Turn off all others.

Press I to enter the sync input configuration mode. Turn on LED 2. Turn off LED's 6 and 12.

Press J to enter the sync output configuration mode. Turn on LED's 2 and 7. Turn off LED 6.

Press K to enter the MIDI channel configuration mode. Turn on LED's 1 and 7. Turn off all others.

(Press LOWER FUNCTION to return panel to normal operation.)

WHAT TO DO IF YOU LOSE YOUR MEMORY:

While it might seem redundant to some, this outline is simply a condensed list of instructions and adjustments already covered in this manual. Its purpose is to provide under one sub-title a concise means for corrective action in the event of having lost everything in memory.

1. Press LOWER FUNCTION - D - 12 - STOP.

2. Press LOWER FUNCTION - TUNE ALL. Move the master slider to maximum, then back to 1/4.

3. Select A-1. You should now have a "scratch sound".

4. The LED above the master slider must be off. If on, turn it off to establish the volume mode. The assignable volume LED must be on. Set the assignable slider 1/4 on.

5. Press LOWER FUNCTION - A.

6. Press 1 and move the master slider down to its minimum position.

   NOTE: If the master slider is already down to minimum, move it up then set it back down to minimum. The motion of the slider is what causes each adjustment to be set.

WHAT TO DO IF YOU LOSE YOUR MEMORY: (CONTINUED)

7. Press 2 and move the master slider up to its maximum position.

8. Press 3 and move the master slider down to minimum.

9. Press 4 and move the master slider up, then down to minimum.

10. Press 5 and move the master slider up to its maximum position.

11. Press 7 and move both levers (not sliders) through their entire mechanical ranges.

12. Press 8 and move the pedal through its range.

13. Press 9 and move the master slider down to 1/8 on. Play 6 different notes, 1 at a time. After releasing each note move the master slider up until you hear the note bleeding through, then back off on the slider until it just dissapears.

14. Press B. Turn on LED's 1, 2, 3, 7, 8, 9, 10, 11 and 12. Turn off LED's 4, 5 and 6.

15. Press C. Turn on LED's 1, 2 and 9. Turn off all others.

16. Press I. Turn on LED 2. Turn off 6 and 12.

17. Press J. Turn on LED's 2 and 7. Turn off 6.

18. Press K. Turn on 1 and 7. Turn off others.

19. Press LOWER FUNCTION to return Polaris to normal operation.

20. LOAD programs and sequences from cassette.

GENERAL OPERATIONAL CHECKOUT:

Connect the Polaris to a sound system using the high level output jack. Plug a footswitch into each of the footswitch jacks and a volume pedal into the pedal jack. Do not initially connect the cassette interface cable or the headphones.

Supply AC power, press LOWER FUNCTION - D - 3 and set the AC input to 117VAC. LED 3 will flash, all other LEDs will turn on.

GENERAL OPERATIONAL CHECKOUT: (CONTINUED)

Press LOWER FUNCTION again to return panel to normal operation. The VOLUME/TUNE LED in the MASTER section should be on; if it is off press the VOLUME/TUNE switch to turn it on. The best signal to noise ratio is obtained when the assignable volume is set high and the master volume is set low.

Select a program, then play up and down the keyboard using single notes and chords. Listen for noises, distortion, loud/soft notes or other anomalies.

Move the levers (on left cheekblock) noting any discontinuity or binding. Test all membrane switches to make sure they work. Using a velocity sensitive program try all keys, making sure none are loud or soft relative to the others.

Play a note, then depress the sustain footswitch and verify that the note stays on after release of the key. Depress the metronome footswitch on and off, tapping it rhythmically with your foot and verify that the LED on the STOP switch flashes in tempo with you. Depress the stop switch to stop the flashing LED.

Reconnect the sound system to the low level output jack and check for distortion or noise. Finally, connect headphones and listen for noise, distortion, clicks, etc.

TESTING THE SYNTHESIZER CHANNELS:

Remove the headphones and reconnect the sound system to the high level output. Load a "scratch program" into the main workspace. Refer to section 5, page 5-1 of this manual for the correct procedure.

Press LOWER FUNCTION - TUNE ALL. The tune LED in the Master section should flash 6 times indicating that each of the 6 channels have been tuned.

Press LOWER FUNCTION - E to enter the channel check mode. The LEDs in switch numbers 1 through 6 should all be on. If any of these are off, it indicates a faulty channel. The channel circuits are numbered from 1 to 6 starting at the rear of the instrument. To forcibly enable a disabled channel, or disable an enabled channel, press the corresponding number switch. Press LOWER FUNCTION again to return the control panel to normal operation.

Press the SAWS/PULSE switch in the two oscillator sections so that their LEDs are on. Then play six different notes, one at a time. When you press each note you should hear nothing. This is because the pulse waveshape has been selected, yet the pulse

TESTING THE SYNTHESIZER CHANNELS: (CONTINUED)

width is zero in a scratch program. For each note verify that pressing the SAWS/PULSE switch in oscillator 1 causes a note to be heard. Play six different notes again, this time verify that pressing the noise switch for each note causes noise to be heard. This exercises the waveshape and noise bits in all six channels.

Move the PULSE WIDTH sliders in the two oscillators to their center positions. Play six different notes, one at a time. When you press each note you should hear the oscillators. For each note verify that pressing the RING MOD switch causes the pitch to jump an octave. This exercises the ring modulation bit in all six channels.

Press the DETUNE switch in the assignable control section and move the assignable slider all the way up. Play six different notes, one at a time. When you press each note you should hear two pitches a semitone apart. For each note verify that pressing the SYNC switch causes only one pitch to be heard. This exercises the sync bit in all six channels. When finished move the assignable slider to the center position to bring the oscillators back in tune.

Move the CUTOFF slider to about 3/4. Play six different notes, one at a time. When you press each note move the RESONANCE slider up and down slowly. You should hear seven steps along its range. In the highest position of the RESONANCE slider the filter should self-oscillate. You may want to use the CUTOFF slider to retune the filter to a setting that makes the resonance steps easier to hear. It is also easier to hear if you turn off one of the oscillators by setting its pulse width to zero. Check the seven filter tuning steps for all six notes. This test exercises the three resonance control bits in all six channels.

Reload a "scratch program" into the main workspace. Press LOWER FUNCTION - TUNE ALL to make sure the oscillators are in tune. Press the VOLUME/TUNE switch so that its LED is on; the MASTER slider will now function as a master tune slider. Play one note, such as middle C, and listen carefully to the beat frequency between the two oscillators. It should be slower than 0.5Hz. If it is too slow to hear select DETUNE and adjust the assignable slider so that you can hear the beat frequency. Slowly move the master slider while listening to the beat frequency. If the beat frequency changes noticably from point to point on the slider it indicates that the DAC is misadjusted or that not all the bits in the DAC circuit are working properly. If the beat frequency remains the same as you move the slider, the DAC is tracking correctly. This test checks DAC tracking and offset. Center the master slider to return tuning to "A-440". Press the VOLUME/TUNE switch to exit the tune mode and restore the volume mode.

SECTION 6: ADJUSTMENTS AND CHECKOUT

CHECKING FOR PROPER ADJUSTMENTS:

Note: The switch sequences or comments after each paragraph (in bold print) refer to the adjustment being tested. That adjustment should be performed if the test fails. The adjustment procedures are detailed earlier in this section.

Select the BEND LEVER RANGE switch from the assignable control section and move the assignable slider all the way up (away from you). Play a note and move the pitch bend lever slowly toward you. The pitch should begin to change as soon as you begin to move the lever and should continue to change until the lever has reached its maximum travel.
(LOWER FUNCTION - A - 7)

Without touching the bend lever move the assignable control up and down. Verify that the pitch does not change.
(Lever pot wiper, 2.5VDC at rest)

Select the MOD LEVER RANGE switch from the assignable control section and move the assignable slider all the way up. Move the sweep rate slider to about 2/3 of its travel. Play a note and move the mod lever slowly toward you. Vibrato should begin as soon as you begin to move the lever and should continue to increase in depth until the lever has reached its maximum travel.
(LOWER FUNCTION - A - 7)

Without touching the modulation lever move the assignable control up and down. Verify that the modulation does not change.
(Lever pot wiper, 2.5VDC at rest)

Select the PITCH PEDAL switch from the assignable section and move the assignable slider all the way up. Starting with the pedalinthe "heel" position play a note and slowly move the pedal to the "toe" position. The pitch should begin to change as soon as you begin to move the pedal and should continue to change until the pedal has reached its maximum travel.
(LOWER FUNCTION - A - 8)

Move the Release sliders in both envelope sections to about mid position. Play six different notes, one at a time. After releasing each note the note should die evenly and about the same time as the note before it.
(LOWER FUNCTION - A - 9)

Push all of the sliders on the control panel all the way down. Press LOWER FUNCTION - D - 4 and make sure the LED in the master section lights when the master slider is moved all the way up. Lower the master slider (slightly) and the LED should go out. It should take no more than 10% of the slider travel to turn off the LED.
(LOWER FUNCTION - D - 4 and R46)

CHECKING FOR PROPER ADJUSTMENTS: (CONTINUED)

Move the master slider all the way up, press LOWER FUNCTION, reselect the scratch sound, then move the master slider to mid position to restore normal operation to the panel.

Press the STOP switch and verify that the LED is flashing but you do not hear the metronome.
(LOWER FUNCTION - A - 1)

Select an empty sequence slot by pressing UPPER FUNCTION - SELECT SEQUENCE - 1-12 (one that is not lit). Press the record switch and verify that you can hear the metronome while the LED is flashing. Record a small sequence then press the STOP (or PLAY) switch.
(LOWER FUNCTION - A - 2)

Press PLAY, then the metronome footswitch and verify that you cannot hear the metronome while the sequencer is playing. Press STOP.
(LOWER FUNCTION - A - 3)

Select an empty sequence slot (as above), then press PLAY and verify that the error honk is present.
(LOWER FUNCTION - A - 5)

Make sure that you hear no clicks or pops when the sweep SINE/SQUARE switch is pressed.
(LOWER FUNCTION - A - 4)

Press LOWER FUNCTION and enter each configuration mode below (B - C- I - J - K). In each mode verify that the LED's are in their specified state (on or off). Correct them as necessary by turning them on or off:

Press B (computer interface). LED's 1, 2, 3, 7, 8, 9, 10, 11 and 12 should be on. LEDs 4, 5 and 6 should be off.

Press C (cassette interface). LED's 1, 2 and 9 on. All others off.

Press I (sync input). LED 2 on. LED's 6 and 12 off.

Press J (sync output). LED's 2 and 7 on. LED 6 off.

Press K (MIDI channel). LED's 1 and 7 on. All others off.

Press LOWER FUNCTION to return panel to normal operation.

TESTING THE INTERFACES:

The Polaris under test (P-U-T) should be connected to a known

TESTING THE INTERFACES: (CONTINUED)

working Polaris (K-W-P) for checkout of the interfaces. Connect the sync out of the P-U-T to the sync in of the K-W-P and the sync out of the K-W-P to the sync in of the P-U-T. Connect the MIDI ports the same way (out to in). Connect the Chroma interface port of the P-U-T directly to the Chroma interface port of the K-W-P. Connect the K-W-P to a sound system using the high level output jack and supply it with AC power. The P-U-T should already be connected to a sound system and have power. Both units should be turned on.

On the P-U-T press LOWER FUNCTION - B, then turn on 4 and turn off 10. Playing on the keyboard should cause both units to sound. When this has been verified (it is easier if they are out of tune with each other) press 4 again to disable the Chroma interface. Verify that the P-U-T plays only itself. Turn on 10 and both units should sound. Press 10, 12, LOWER FUNCTION to return the panel to normal operation.

On the K-W-P press LOWER FUNCTION - B, then turn on 4 and turn off 10. Make sure the K-W-P plays both units. Turn off 4 and make sure the K-W-P plays only itself. Turn on 10. Make sure the K-W-P plays both. Press 10, LOWER FUNCTION to return the panel to normal.

If the STOP LED is not flashing on either unit press the STOP switch to make it flash. Press LOWER FUNCTION - H - 2 on the P-U-T and LOWER FUNCTION - H - 5 on the K-W-P to tell the P-U-T to generate a sync and the K-W-T to follow it. Press LOWER FUNCTION on the P-U-T to restore operation to the panel.

Verify that the P-U-T is controlling the K-W-P by repeatedly pressing STOP on the P-U-T. The flashing LED should stop and start on both units. When this has been verified leave the LED's so they flash, then press LOWER FUNCTION - H - 5 on the P-U-T and 2 on the K-W-P. Press LOWER FUNCTION on the K-W-P to restore its panel to normal operation. Make sure that the K-W-P can start and stop the P-U-T in the same manner. Leave the LED's flashing. Press LOWER FUNCTION - H - 1, LOWER FUNCTION - STOP on the K-W-P, then press 1, LOWER FUNCTION - STOP on the P-U-T to restore the panel to normal operation.

The cassette interface tests require the use of a Factory Programmed Polaris data cassette tape, a cassette recorder/player and a cassette interface cable. We recommend the Radio Shack model CCR - 81 cassette recorder/player. Cassette interface cables are available from Fender (part number 30-2204901) or you may use one from Radio Shack (catalog number 26-1207).

Remove the sync in cable and install the cassette interface cable. The gray sub-miniature plug connects to the remote jack,

TESTING THE INTERFACES: (CONTINUED)

the gray miniature plug to the microphone inputjack, and the black miniature plug to the earphone output jack on the recorder.

Insert the data cassette into the cassette player. Press UPPER FUNCTION - LOAD ALL. Press PLAY on the cassette player. This will load all the programs. When the tape stops and the UPPER FUNCTION LED goes out, press UPPER FUNCTION - LOAD ALL again to load the demonstration sequences.

Simultaneously press the PAUSE, PLAY, and RECORD switches on the cassette recorder/player. While watching the record LED on the cassette recorder, press UPPER FUNCTION - SAVE ALL PROG. When the data is transmitted, the LED on the cassette recorder should light. Terminate the save operation by pressing UPPER FUNCTION. On the cassette recorder press STOP, then release the PAUSE.

SECTION 7: OPTIONS

EXPANDING RAM:

The Polaris supports two types of RAM chips, 6116's or 6264's. A Polaris is usually delivered from factory to dealer with eight 6116 2K x 8 RAM chips installed, equal to 16K.

Optional memory packages are available for field installation to expand RAM, providing an increase in available note storage for the on-board sequencer. Two packages are available: Memory Expansion Package I, or Package II. Package I consists of four 6264 8K x 8 RAM chips, expanding RAM to 32K. Package II consists of two 6264 8K x 8 RAM chips, expanding RAM another 16K, to 48K. Adding a second Package II will expand RAM to 64K. Refer to "Memory Array" in section 3 of this manual for a more detailed description of configurations allowed.

The following is a copy of the installation instructions for the memory expansion kits:

POLARIS MEMORY EXPANSION PACKAGE

INSTALLATION INSTRUCTIONS
PART NUMBER 309006401

MATERIAL REQUIRED:

P/N 306864000 Mem. Expan. Pkg. I or 306801901 Mem. Expan. Pkg. II
Cassette Recorder/Player w/tape
I.C. insertion/extraction tool - hand tools

MAKE SURE YOU SAVE THE CUSTOMER'S PROGRAMS AND SEQUENCES ON CASSETTE BEFORE YOU BEGIN. THIS PROCEDURE WILL ERASE ALL PROGRAMS AND SEQUENCES FROM MEMORY. OBSERVE STANDARD SAFETY PROCEDURES FOR STATIC SENSITIVE IC'S.

PROCEDURE:

1. Save the programs and sequences on cassette.
2. Disconnect line power and open the Polaris.
3. Remove the keyboard. CAUTION: Watch for keyboard spacer shims.
4. Disconnect J15 from the main board. It is not sufficient to remove a battery from the holder as the capacitor on the holder retains its charge for a rather long time.
5. Using the correct extraction tool, remove the 8, 6116, 2K x 8 RAM chips from sockets Z2 through Z9.
6. Using an insertion tool, carefully install 4, 6264, 8K x 8 RAM chips into sockets Z2, Z3, Z4, and Z5. Sockets Z6, Z7, Z8 and Z9 remain blank. This expands the memory from 16K to 32K and increases the sequencer note storage by 2700 notes. This conforms to the P/N 306864000 expansion package I.

SECTION 7: OPTIONS

EXPANDING RAM: (INSTALLATION INSTRUCTIONS CONTINUED)

7. For one P/N 306801901 expansion package II kit, install 2, 6264, 8K x 8, RAM chips into sockets Z6 and Z7. Sockets Z8 and Z9 remain blank. This expands memory from 32K to 48K and increases note storage by another 2700 notes.
8. For an additional P/N 306801901 expansion package II kit, simply install 2, 6264, 8K x 8 RAM chips into the remaining 2 sockets, Z8 and Z9. This expands memory from 48K to 64K and increases note capacity by 2700 more notes for an overall net increase of 8100 notes. Total capacity depends on program allocation to memory, but with a full 132 programs capacity equals 8750 notes. With 50 programs capacity is in excess of 9400 notes.
9. Reverse both jumpers between Z8 and Z9. The jumper closest to pin 14 of Z9 should now be shorting the center pin to the pin on its right and the jumper closest to pin 15 of Z9 should short its center pin to the top pin. The write strobes and address bits are changed by these jumpers to conform to the type memory chip in use.
10. Reconnect the battery connector J15.
11. Carefully align the keyboard and reassemble the Polaris.
12. Perform software adjustments as outlined in "WHAT TO DO IF YOU LOSE YOUR MEMORY".
13. Load programs and sequences.
14. Check-out.

CHANGING EPROMS:

The system supports two types of EPROM chips, 2764's and 27128's, allowing four configurations up to 64K ROM. The jumper located near the left rear corner of the main board (next to C819 and Z19) determines the addressing. This jumper should be shorting the center pin to the bottom pin (bottom is nearest keyboard) for 2764's. If 27128's are installed the jumper should short the center pin to the top pin. Refer to "Memory Array" in section 3 of this manual for a detailed description of allowable configurations.

One of the chief advantages EPROM's provide, is the relatively easy means of updating certain characteristics of the system by changing them to a different software revision. As stated in Section 3, it is important to realize that when you change to a different revision the memory locations used for different purposes usually change. This means you have to reload all programs and sequences, implement a "scratch program", then perform all software adjustments outlined by "What to do if you lose your memory" in Section 6 of this manual.

SECTION 7: OPTIONS

JUMPER OPTIONS:

There are five 3-pin and one 16-pin jumper connectors on the main board. Three of the 3-pin jumpers deal with memory chips (covered earier in this section) but all will be described under this one sub-title to provide easy reference.

No reference designations exist for any of the six jumper connectors, but they are relatively easy to locate using adjacent components. References are defined as follows: Top, away from keyboard. Bottom, closest to keyboard. Left, right, viewing over keyboard onto main board. Top synonymous with rear, bottom synonymous with front.

One of the 3-pin jumper connectors, located near the left rear corner of the main board (next to C819 and Z19), determines addressing of the EPROM's. The jumper should be shorting the center pin to the bottom pin for type 2764 EPROM's. Type 27128 EPROM's (or mixed 2764's and 27128's) require the jumper to short the center pin to the top pin.

Two 3-pin jumper connectors, located between RAM chips Z8 and Z9, steer the write stobes and address bits to conform to the type of RAM chip used. With type 6116 RAM chips the jumper closest to pin 14 of Z9 should short the center pin to the left pin and the jumper closest to pin 15 of Z9 should short the center pin to the bottom pin. With type 6264 RAM chips both pins must be reversed.

As described in Section 3, the Polaris uses either a 6 or 8 Mhz clock, derived from either 12 or 16Mhz, for the 80186-6 or 80186-3, respectively. Two 3-pin jumper connectors, reconfigure signal inputs for the two individual modes. In the 6Mhz version, the jumper adjacent to C884 and Z84 must short the center pin to the the bottom pin, while the jumper adjacent to C829 and Z29, short the center pin to the right pin. In the 8Mhz version, both pins must be reversed.

Next to C883 and Z83 is a 16 pin jumper platform. This was used for reconfiguring interrupt and DMA requests during development. Shorting jumpers should be installed to short pin 1 to 2, 3 to 4, 6 to 7, 10 to 11 and 14 to 15.

SECTION 8: PARTS LIST

This section outlines most parts needed to service the Polaris. Certain parts, commonly available, and stocked by most service centers (such as fixed value resistors) have been deleted from the list to keep it from becoming unnecessarily long.

MAIN BOARD, 307227701:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
R45, 46	301003302	--------	Pot rtry 10K 30% lin 1/5W	2
CX03-X35	301104401	--------	Cap mylar 0.0068uF 50V	25
C17	301104403	--------	Cap mylar 0.015uF 50V	1
CX02-X27	301104402	--------	Cap mylar 0.033uF 50V	52
C16	301104404	--------	Cap mylar 0.1uF 50V	1
CX01-X05	301104501	--------	Cap polyprop 0.0068uF 50V	12
CX02-X04	301104502	--------	Cap polyprop 0.033uF 50V	12
CX18-X22	301104601	--------	Cap polystyrol 1000pF 50V	12
Z210-710	301406101	--------	Res array 1M 2% 1/4Wx7 DIP	6
Z51	301414103	--------	Res array 10K 2% 1/4Wx8 DIP	1
Z74, 75	301414104	--------	Res array 1K 2% 1/4Wx8 DIP	2
Z76	301418301	--------	Res array 1K 2% 1/4Wx9 SIP	1
CR1	301200101	1N34A	Diode Ge	1
CR2,10	301200201	1N4001	Diode Si rect 1A 50PIV	2
CR3-702	301200301	1N4148	Diode Si sig	28
Q1-5,7-9	301306601	2SC1815*	Transistor Si NPN	8
Q6	301306701	2SB859**	Transistor Si PNP	1
CY1	302600303	--------	Crystal 12Mhz	1
Z1	301416201	C80186-6	Microprocessor 16 bit 6Mhz	1
Z19,80,85	301401702	74LS00	IC TTL quad 2 input nand	3
Z42	301401802	74LS02	IC TTL quad 2 input nor	1
Z23	301418701	74LS03	IC TTL quad 2 input nand OC	1
Z73,81,82	301406601	74LS04	IC TTL hex inverter	3
Z20,21,44, 45	301416501	74LS32	IC TTL quad 2 input or	4
Z25,26,43, 47,52	301406701	74LS74	IC TTL dual D flop	5
Z27	301413102	74LS138	IC TTL 1 of 8 decoder	1
Z28	301416601	74LS139	IC TTL dual 1 of 4 decoder	1
Z83	301418501	74LS163	IC TTL sync. binary counter	1
Z16,18,24	301413001	74LS244	IC TTL oct buff/line driver	3
Z17	301412701	74LS245	IC TTL oct bus transceiver	1
Z14,15	301412901	74LS373	IC TTL oct transparent latch	2
Z84	301410501	74LS393	IC TTL dual modulo-16 count.	1

* Approved substitute for 2SC1815: 2SC945 or 2N3904
** Approved substitute for 2SB859 : 2N3906

SECTION 8: PARTS LIST

MAIN BOARD, 307227701: (CONTINUED)

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
Z32,35,36, 60,61	301416701	74HC138	IC HS CMOS 3-8 line decoder	5
Z55,63	301416801	74HC174	IC HS CMOS hex D flop	2
Z33,39	301416901	74HC175	IC HS CMOS quad D flop	2
Z34,49	301417001	74HC244	IC HS CMOS oct buffer	2
Z29,38	301417101	74HC251	IC HS CMOS 8-chan multiplex	2
Z30,31	301417201	74HC259	IC HS CMOS 3-8 line decoder	2
Z22,56, 200-700	301417301	74HC374	IC HS CMOS oct D flop	8
Z37	301417401	74HC393	IC HS CMOS dual bin counter	1
Z201-701, 202-702,62	301404901	4051B	IC CMOS 8-ch multiplx/demul	13
Z207-707, 208-708	301406201	4053B	IC CMOS tri 2-ch mulplx/dml	12
Z48	301418601	4066B	IC CMOS quad bilatrl switch	1
Z70,71	301416401	4070B	IC CMOS quad exclusive or	2
Z40,58	301407601	TL081	IC bifet op amp	2
Z41,54,57	301409001	TL082	IC bifet op amp	3
Z203-703, 204-704	301417701	TL084	IC bifet op amp	12
Z206-606	301413601	LM393	IC dual differen comparator	6
Z64	301414201	MM5837	IC noise generator	1
Z53	301415401	0804	IC analog/digital convertor	1
Z59	301417601	HS3140	IC digital/analog convertor	1
Z46	301417501	1489A	IC line receiver	1
Z86	301418101	6N138	IC opto isolator	1
Z209-709	301417901	CEM3372	IC vcf/vca signal processor	6
Z205-705	301417801	CEM3374	IC dual vco	6
Z87	301418201	68B50	IC communica interf 2MHz	1
Z2-9	301416301	6116L	IC random access memory	8
Z10-13	301418001	2764G	IC erase/prog read only mem	4
	(Use part no. 306802201 for preprogrammed Eprom set)			
K1	301905501	LAB2	Relay 5VDC	1

CONTROL PANEL LEFT, 307227501:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
R1-12	301003201	--------	Pot slide 10K 30% lin 1/5W	12
CR21	301200502	RD6.8E	Diode zener 6.8V 5%	1
CR1-20	301202701	SLR40UR5	Diode LED SLR 40UR5	20
Z1,2	301409001	TL082	IC bifet op amp	2
Z3,4	301404901	4051B	IC CMOS 8-ch multiplx/demul	2
Z5-7	301416001	74LS164	IC TTL ser/par shift reg	3
Q1-4	301306601	2SC945	Transistor Si NPN	4
----	307550301	--------	Membrane sw. lf w/graphics	1

SECTION 8: PARTS LIST

CONTROL PANEL RIGHT, 307227601:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
R1-8	301003201	--------	Pot slide 10K 30% lin 1/5W	8
CR1-40	301202701	SLR40UR5	Diode LED SLR 40UR5	40
Z1	301408001	74LS145	IC TTL BCD decimal decoder	1
Z2	301409101	74LS175	IC TTL quad D-flop	1
Z3	301413001	74LS244	IC TTL oct buff/line driver	1
Z4	301413102	74LS138	IC TTL 1 of 8 decoder	1
Z5	301404901	4051B	IC CMOS 8-ch multiplx/demul	1
Z6	301413201	74LS174	IC TTL hex D-flop	1
Z7-11	301416001	74LS164	IC TTL ser/par shift reg	5
----	307550401	--------	Membrane sw. rt w/graphics	1

PRIMARY BOARD, EARLY VERSION 307227301, LATE VERSION 307227302:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
LF1	302110401	FN323-3/01	Line filter	1
S2	301905601	SDE-4S	Power switch DPDT	1
R1-2	301002801	C20D241V	MOV 150V ERZ-C20D241V	2
T1	305712601	--------	Pwr transf (Early version)	1
T1	305712602	FJ-300009	Pwr transf (Late version)	1

SECONDARY BOARD, EARLY VERSION 307227101:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
R5,9	301003301	--------	Pot rtry 2.5K 30% lin 1/5W	2
R17	301003302	--------	Pot rtry 10K 30% lin 1/5W	1
CR1-4,7,8	301202101	1N4002	Diode Si rect 1A 100PIV	6
CR5,6	301201701	MR750	Diode Si rect 22A 50PIV	2
CR9	301200301	1N4148	Diode Si signal	1
Q1	301306801	2SA1029	Transistor PNP	1
Q2	301306601	2SC945	Transistor NPN	1
Z1	301415601	LM340T	Regulator 3 term	1
Z2	301403801	LM7912CT	Regulator 3 term	1
Z3	301415701	LM317T	Regulator 3 term	1
Z4	301415901	LM7905CT	Regulator 3 term	1
Z5	301415801	LM350K	Regulator 3 term	1
Z6	301414801	AD587KH	Voltage reference 1.2V	1
Z7	301411001	LM311	IC comparator	1

SECTION 8: PARTS LIST

SECONDARY BOARD, LATE VERSION 307227102:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
R4,15	301003303	--------	Pot rtry 1K 30% lin 1/5W	2
CR1,2	301201701	MR750	Diode Si rect 22A 50PIV	2
CR3-8	301202101	IN4002	Diode Si rect 1A 100PIV	6
Q1,3,5	301306801	2SA1029	Transistor PNP	3
Q2,4	301306601	2SC1815	Transistor NPN	2
Z1	301415801	LM350K	Regulator 3 term	1
Z2	301415601	LM340T	Regulator 3 term	1
Z3	301403801	LM7912CT	Regulator 3 term	1
Z4	301415701	LM317T	Regulator 3 term	1
Z5	301415901	LM7905CT	Regulator 3 term	1

OUTPUT BOARD, 307227801:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
CR1,2	301200201	1N4001	Diode Si rect 1A 50PIV	1
Q1	301306801	2SA1029	Transistor PNP	1
Z1	301407601	TL081	IC bifet op amp	1
Z2	301400401	LM3080	IC OTA	1
Z3	301418801	LM348	IC op amp	1

KEYBOARD, 305712501:

REFERENCE	PART NO.	MFG. NO.	DESCRIPTION	QTY
----	305712801	--------	Key - C - natural	5
----	305712802	--------	Key - D - natural	5
----	305712803	--------	Key - E - natural	5
----	305712804	--------	Key - F - natural	5
----	305712805	--------	Key - G - natural	5
----	305712806	--------	Key - A - natural	5
----	305712807	--------	Key - B - natural	5
----	305712808	--------	Key - high C - natural	1
----	305712901	--------	Key - sharp	25
----	305713001	--------	Keyspring - natural	36
----	305713101	--------	Keyspring - sharp	25
----	305713201	--------	Keyguide bushing	61

SECTION 9: SCHEMATICS, PC LAYOUTS AND DIAGRAMS

LEFT MEMBRANE SWITCH MATRIX = J8A/B

J8A

1	- NC
2	- SWSTB0
3	- SWSTB1
4	- SWSTB2
5	- NC

J8B

1	- NC
2	- SW0
3	- SW1
4	- SW2
5	- SW3
6	- SW4
7	- SW5
8	- SW6
9	- NC
10	- NC

MEMBRANE SWITCHES	MATRIX INTERSECTION
SEQUENCER:	
STOP	J8B-2 ($\overline{SW0}$) AND J8A-4 ($\overline{SWSTB2}$)
RECORD	J8B-3 ($\overline{SW1}$) AND J8A-2 ($\overline{SWSTB0}$)
PLAY	J8B-3 ($\overline{SW1}$) AND J8A-3 ($\overline{SWSTB1}$)
LOWER FUNCTION	J8B-3 ($\overline{SW1}$) AND J8A-4 ($\overline{SWSTB2}$)
KYBD:	
LINK UPPER	JB8-2 ($\overline{SW0}$) AND J8A-3 ($\overline{SWSTB1}$)
LINK UNISON	J8B-4 ($\overline{SW2}$) AND J8A-2 ($\overline{SWSTB0}$)
LINK LOWER	J8B-4 ($\overline{SW2}$) AND J8A-3 ($\overline{SWSTB1}$)
KYBD RANGE	J8B-4 ($\overline{SW2}$) AND J8A-4 ($\overline{SWSTB2}$)
MASTER:	
VOLUME/TUNE	J8B-2 ($\overline{SW0}$) AND J8A-2 ($\overline{SWSTB0}$)
OSCILLATOR 1:	
RING MOD	J8B-5 ($\overline{SW3}$) AND J8A-4 ($\overline{SWSTB2}$)
SWP PWM/ENV PWM	J8B-6 ($\overline{SW4}$) AND J8A-2 ($\overline{SWSTB0}$)
SAWS/PULSE	J8B-6 ($\overline{SW4}$) AND J8A-3 ($\overline{SWSTB1}$)
TRANSPOSE	J8B-6 ($\overline{SW4}$) AND J8A-4 ($\overline{SWSTB2}$)
OSCILLATOR 2:	
SYNC	J8B-5 ($\overline{SW3}$) AND J8A-3 ($\overline{SWSTB1}$)
SWP PWM/ENV PWM	J8B-7 ($\overline{SW5}$) AND J8A-2 ($\overline{SWSTB0}$)
SAWS/PULSE	J8B-7 ($\overline{SW5}$) AND J8A-3 ($\overline{SWSTB1}$)
TRANSPOSE	J8B-7 ($\overline{SW5}$) AND J8A-4 ($\overline{SWSTB2}$)
SWEEP:	
SINE/SQUARE	J8B-5 ($\overline{SW3}$) AND J8A-2 ($\overline{SWSTB0}$)
FILTER:	
NOISE	J8B-8 ($\overline{SW6}$) AND J8A-2 ($\overline{SWSTB0}$)

RIGHT MEMBRANE SWITCH MATRIX = J9A/B

J9A

1	NC
2	SWSTB3
3	SWSTB4
4	SWSTB5
5	SWSTB6
6	SWSTB7
7	NC

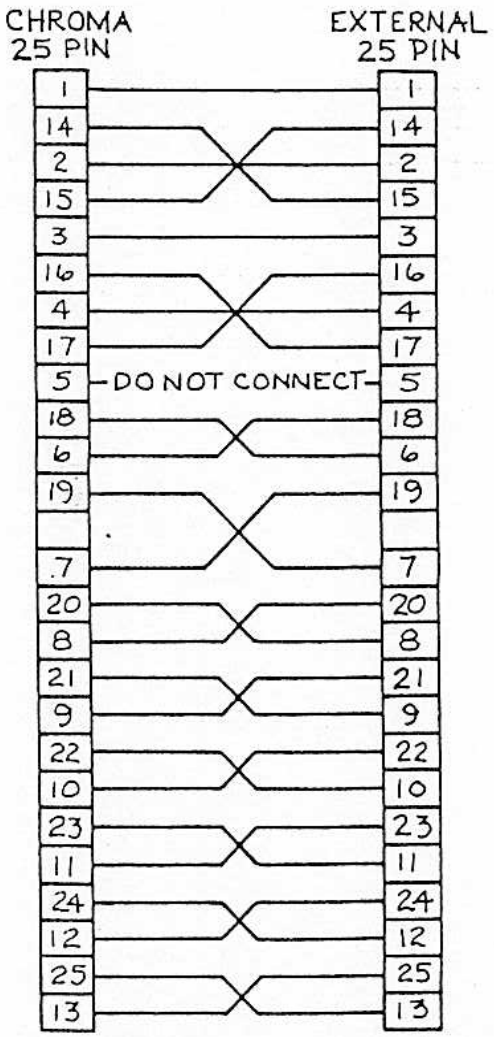
J9B

1	NC
2	SW0
3	SW1
4	SW2
5	SW3
6	SW4
7	SW5
8	SW6
9	SW7
10	NC

MEMBRANE SWITCHES	MATRIX INTERSECTION
ENVELOPE:	
FIXED TOUCH	J9B-2 ($\overline{SW0}$) AND J9A-2 ($\overline{SWSTB3}$)
VOLUME ENVELOPE:	
FIXED TOUCH	J9B-3 ($\overline{SW1}$) AND J9A-2 ($\overline{SWSTB3}$)
ASSIGNABLE CONTROL:	
GLIDE	J9B-3 ($\overline{SW1}$) AND J9A-3 ($\overline{SWSTB4}$)
RATE PEDAL	J9B-2 ($\overline{SW0}$) AND J9A-3 ($\overline{SWSTB4}$)
VIBRATO PEDAL	J9B-3 ($\overline{SW1}$) AND J9A-4 ($\overline{SWSTB5}$)
PITCH PEDAL	J9B-2 ($\overline{SW0}$) AND J9A-4 ($\overline{SWSTB5}$)
CUTOFF PEDAL	J9B-3 ($\overline{SW1}$) AND J9A-5 ($\overline{SWSTB6}$)
VOLUME PEDAL	J9B-2 ($\overline{SW0}$) AND J9A-5 ($\overline{SWSTB6}$)
VOLUME	J9B-2 ($\overline{SW0}$) AND J9A-6 ($\overline{SWSTB7}$)
MOD LEVER RANGE	J9B-3 ($\overline{SW1}$) AND J9A-6 ($\overline{SWSTB7}$)
BEND LEVER RANGE	J9B-4 ($\overline{SW2}$) AND J9A-2 ($\overline{SWSTB3}$)
VIBRATO DELAY	J9B-5 ($\overline{SW3}$) AND J9A-2 ($\overline{SWSTB3}$)
OSC 1 VIBRATO	J9B-6 ($\overline{SW4}$) AND J9A-2 ($\overline{SWSTB3}$)
OSC 2 VIBRATO	J9B-7 ($\overline{SW5}$) AND J9A-2 ($\overline{SWSTB3}$)
OSC 2 ENVELOPE	J9B-8 ($\overline{SW6}$) AND J9A-2 ($\overline{SWSTB3}$)
DETUNE	J9B-9 ($\overline{SW7}$) AND J9A-2 ($\overline{SWSTB3}$)
BANK SELECT/PROGRAM SELECT:	
UPPER FUNCTION	J9B-4 ($\overline{SW2}$) AND J9A-3 ($\overline{SWSTB4}$)
A	J9B-5 ($\overline{SW3}$) AND J9A-3 ($\overline{SWSTB4}$)
B	J9B-6 ($\overline{SW4}$) AND J9A-3 ($\overline{SWSTB4}$)
C	J9B-7 ($\overline{SW5}$) AND J9A-3 ($\overline{SWSTB4}$)
D	J9B-8 ($\overline{SW6}$) AND J9A-3 ($\overline{SWSTB4}$)
E	J9B-9 ($\overline{SW7}$) AND J9A-3 ($\overline{SWSTB4}$)
F	J9B-4 ($\overline{SW2}$) AND J9A-4 ($\overline{SWSTB5}$)
G	J9B-5 ($\overline{SW3}$) AND J9A-4 ($\overline{SWSTB5}$)
H	J9B-6 ($\overline{SW4}$) AND J9A-4 ($\overline{SWSTB5}$)
I	J9B-7 ($\overline{SW5}$) AND J9A-4 ($\overline{SWSTB5}$)

RIGHT MEMBRANE SWITCH MATRIX - J9A/B (CONTINUED)

J.....J9B-7 ($\overline{SW6}$) AND J9A-4 ($\overline{SWSTB5}$)
K.....J9B-9 ($\overline{SW7}$) AND J9A-4 ($\overline{SWSTB5}$)
1.....J9B-4 ($\overline{SW2}$) AND J9A-5 ($\overline{SWSTB6}$)
2.....J9B-5 ($\overline{SW3}$) AND J9A-5 ($\overline{SWSTB6}$)
3.....J9B-6 ($\overline{SW4}$) AND J9A-5 ($\overline{SWSTB6}$)
4.....J9B-7 ($\overline{SW5}$) AND J9A-5 ($\overline{SWSTB6}$)
5.....J9B-8 ($\overline{SW6}$) AND J9A-5 ($\overline{SWSTB6}$)
6.....J9B-9 ($\overline{SW7}$) AND J9A-5 ($\overline{SWSTB6}$)
7.....J9B-4 ($\overline{SW2}$) AND J9A-6 ($\overline{SWSTB7}$)
8.....J9B-5 ($\overline{SW3}$) AND J9A-6 ($\overline{SWSTB7}$)
9.....J9B-6 ($\overline{SW4}$) AND J9A-6 ($\overline{SWSTB7}$)
10.....J9B-7 ($\overline{SW5}$) AND J9A-6 ($\overline{SWSTB7}$)
11.....J9B-8 ($\overline{SW6}$) AND J9A-6 ($\overline{SWSTB7}$)
12.....J9B-9 ($\overline{SW7}$) AND J9A-6 ($\overline{SWSTB7}$)



INTERFACE CABLE SCHEMATIC