

BS 524-7

Address	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
3	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
5	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
7	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1

NORMAL MODE
(A5, A6 = 1, 0)

Address	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
0																																		
1																																		
2																																		
3																																		
4																																		
5																																		
6																																		
7																																		

REPEAT MODE
(A5, A6 = 0, 0)

Address	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
0																																		
1																																		
2																																		
3																																		
4																																		
5																																		
6																																		
7																																		

"φ" DELAY MODE
(A5, A6 = 1, 1)

Address	Bit 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
0																																		
1																																		
2																																		
3																																		
4																																		
5																																		
6																																		
7																																		

REPEAT / "φ" DELAY MODE
(A5, A6 = 0, 1)

SAME AS REPEAT ONLY.

EPROM LISTING
DDL.3.φ.φ

ADDRESS	00H	10H	20H	30H	40H	50H	60H	70H	80H	90H
	EF EF 6F EF EF EF AF EF EF EF EF EF EF ED E5 E1	F5 F5 75 F5 F5 F5 B5 F5 F5 F5 F5 F5 F5 E5 ED E9	EF EF 6F EF EF EF AF EF EF CF CF EF EF EC E4 E1	F5 F5 75 F5 F5 F5 B5 F5 F5 D5 D5 F5 F5 E4 EC E9	EF EF EF EF EF EF EF EF EF EF EF 6F EF EF ED A5 E1	F5 F5 F5 F5 F5 F5 F5 F5 F5 F5 75 F5 F5 E5 AD E9	EF EF EF EF EF EF EF EF EF EF CF 4F EF EF EC A4 E1	F5 F5 F5 F5 F5 F5 F5 F5 F5 D5 55 F5 F5 E4 AC E9	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF

REPEAT MODE (A5, A6 = 0, 0)
 NORMAL MODE (A5, A6 = 0, 1)
 REPEAT & φ DELAY MODE (A5, A6 = 1, 0)
 φ DELAY MODE (A5, A6 = 1, 1)
 NOT USED

MODEL 524 DDL DIGITAL TIMING

ROM MAP

3-23-83 FIR

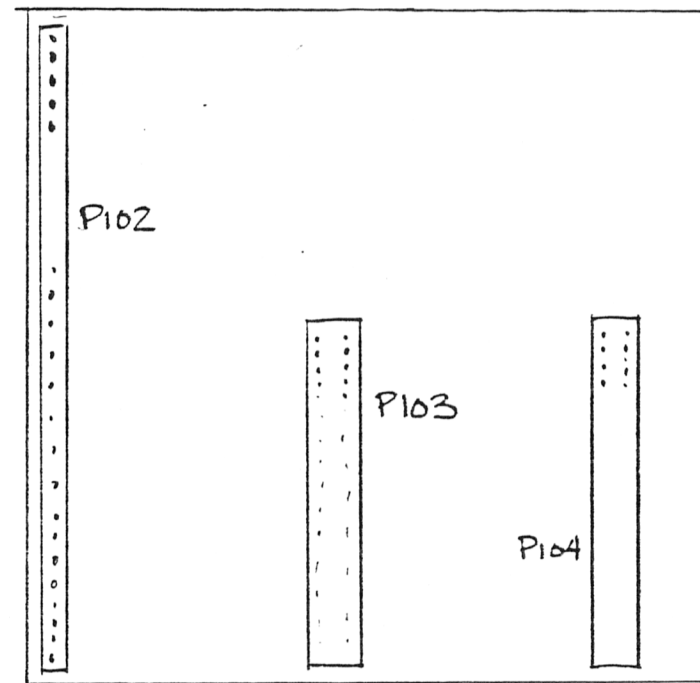
BS 524-8

MODEL 524 DDL BOARD INTERCONNECT DIAGRAM

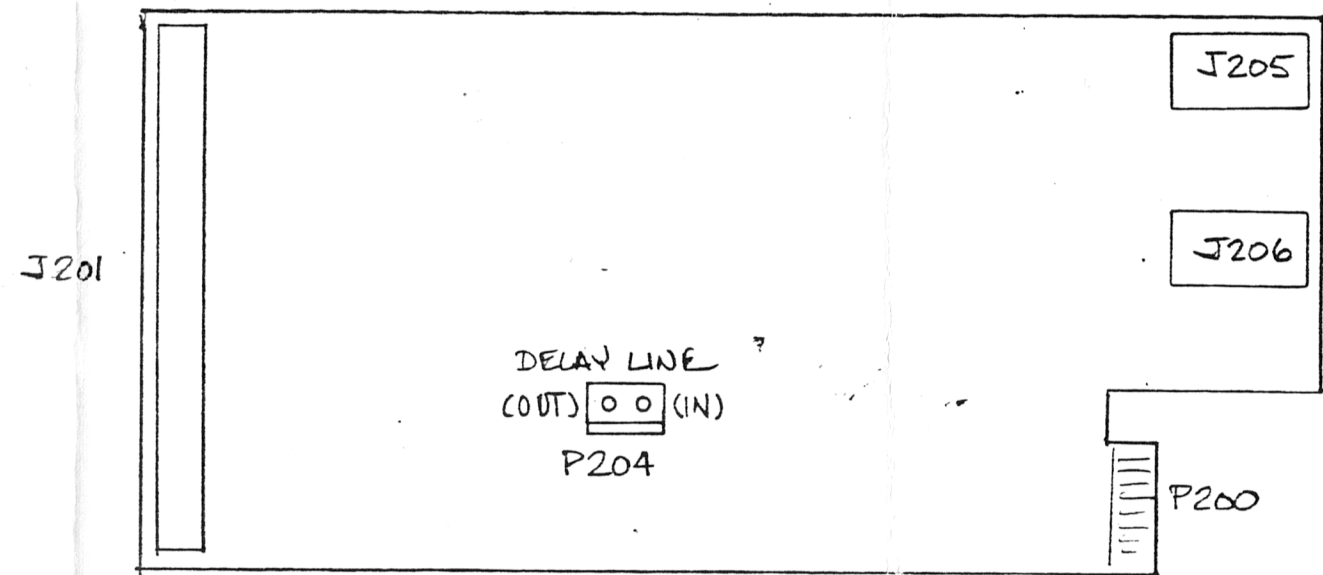
3-7-83

RJR

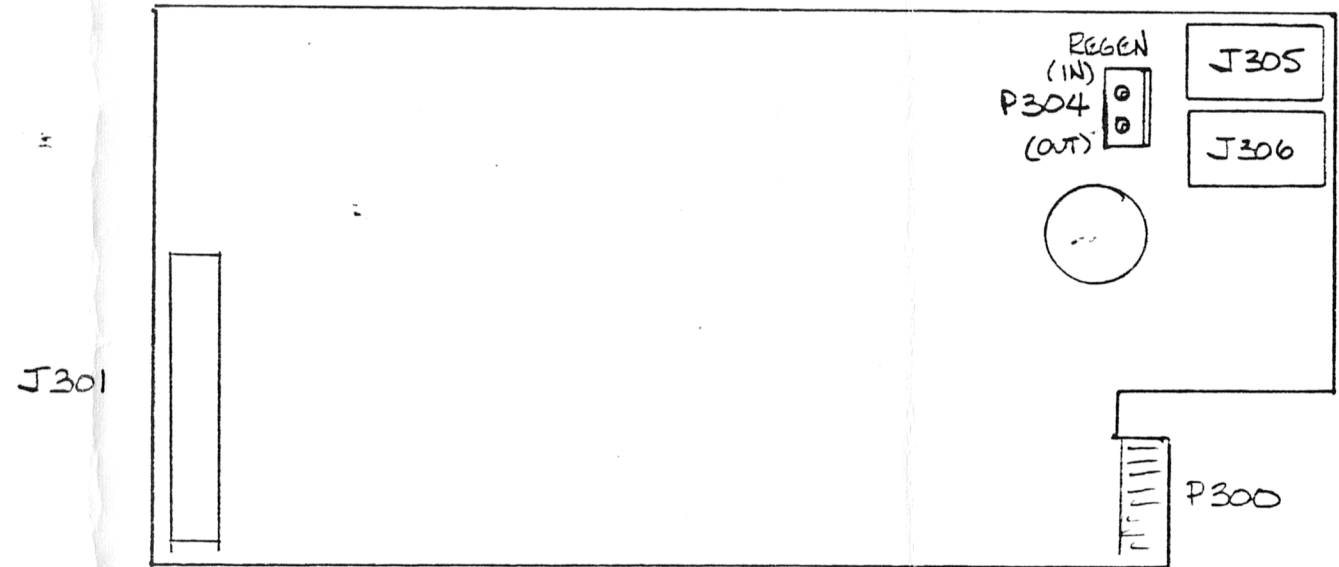
BS 524-10



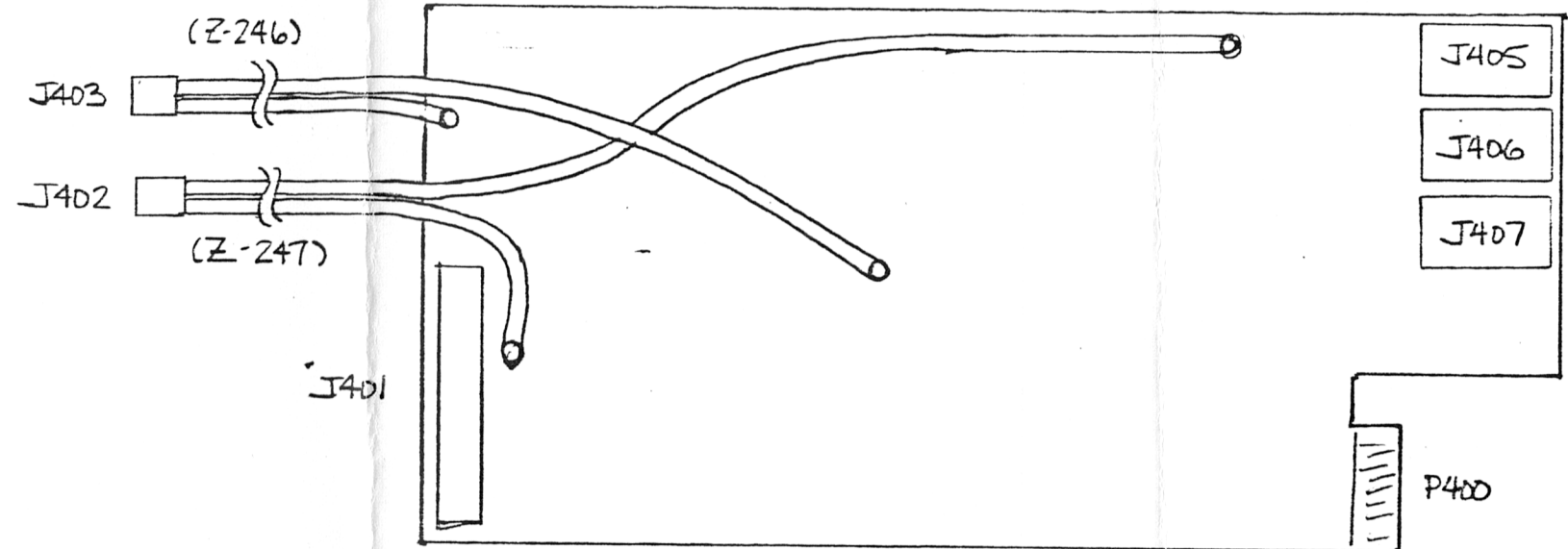
PCB 1
(BACK VIEW)



PCB 2 - DA/AD

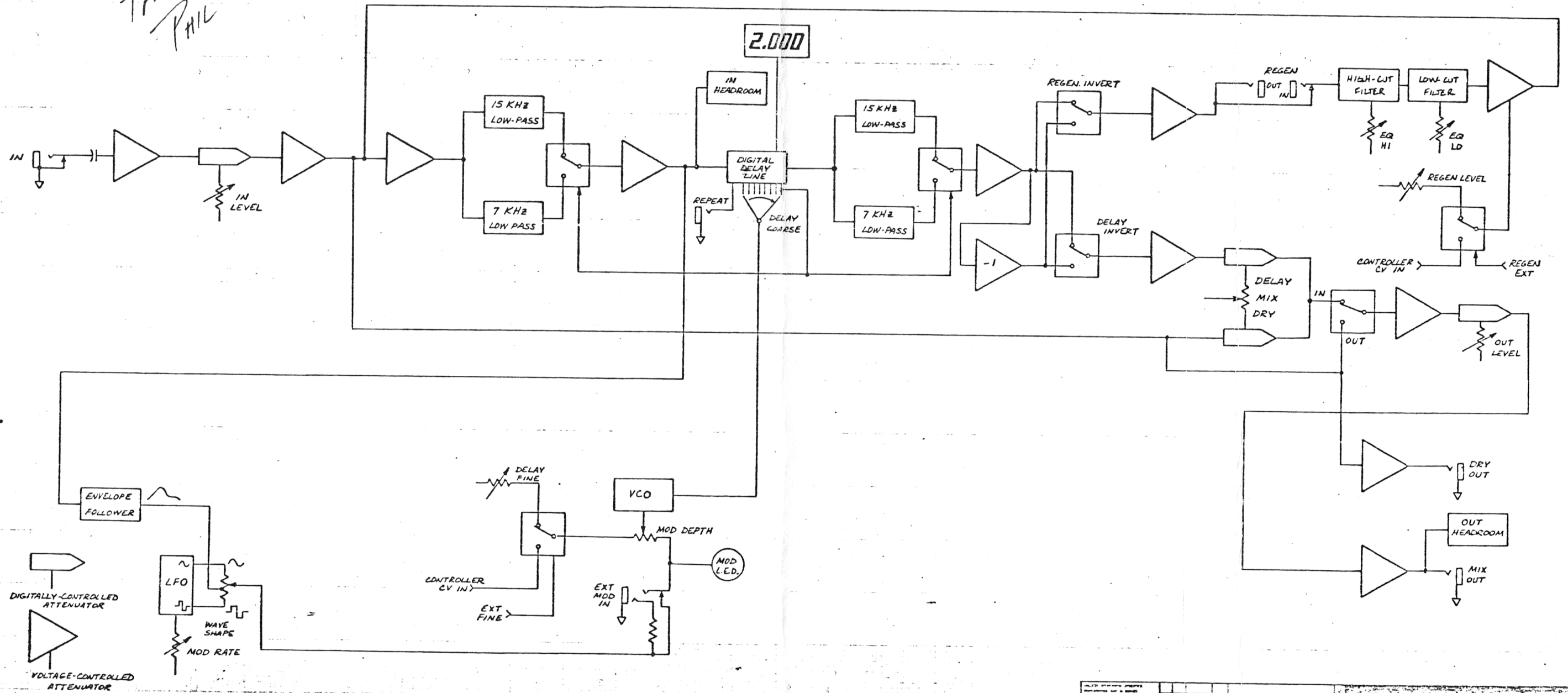


PCB 3 - DIGITAL



PCB 4 - ANALOG

STEVE!
 THIS ONE DOES HAVE
 A FEW NEW MODS,
 BUT THESE ARE NOT AVAILABLE
 TO ME AT THIS TIME.
 I'LL SEND YOU AN ECO
 AS SOON AS I GET
 ONE -
 TAKE CARE
 PHIL

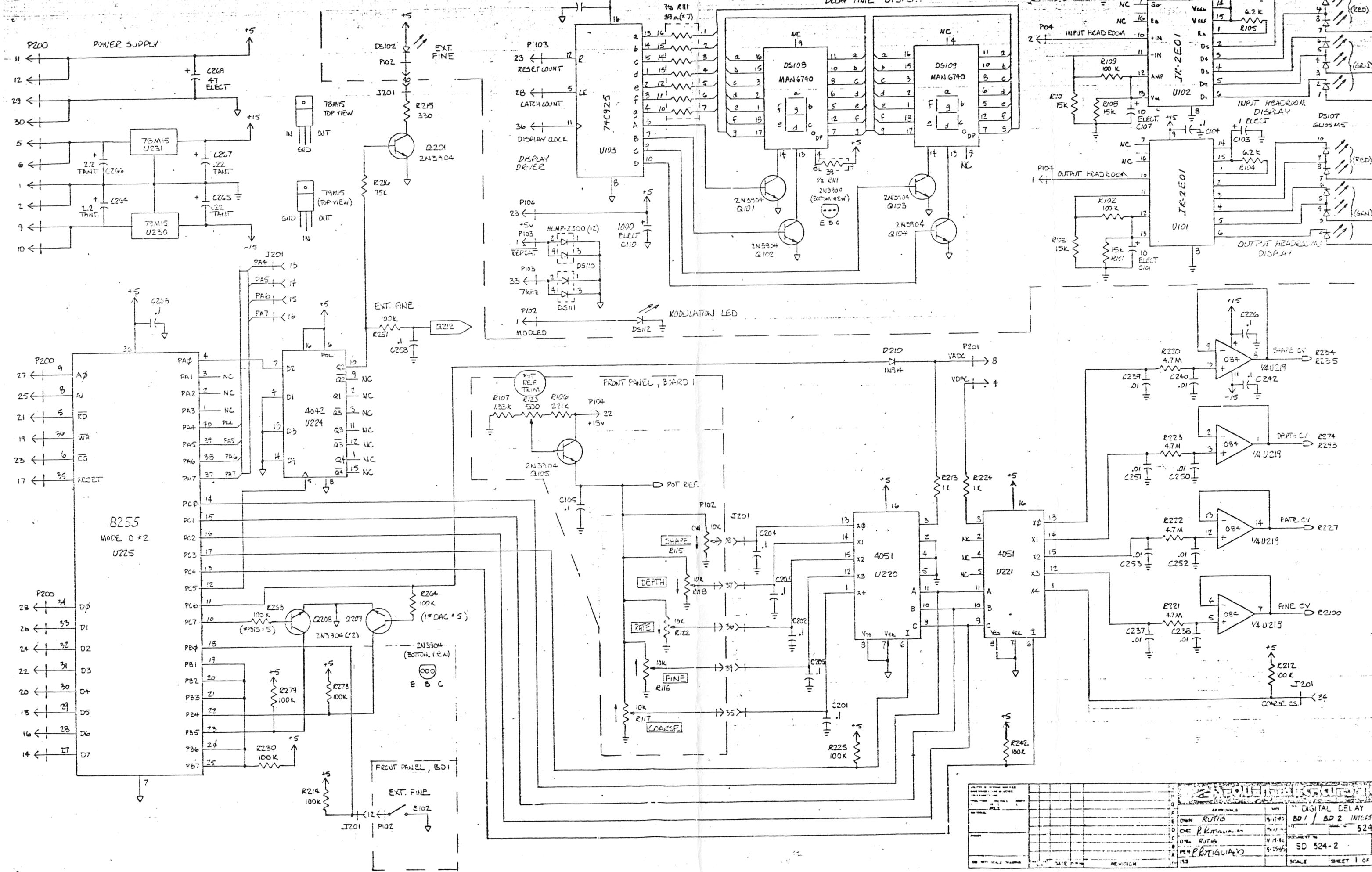


REV	DATE	REVISION	SCALE	SHEET	TOTAL
1				1	1

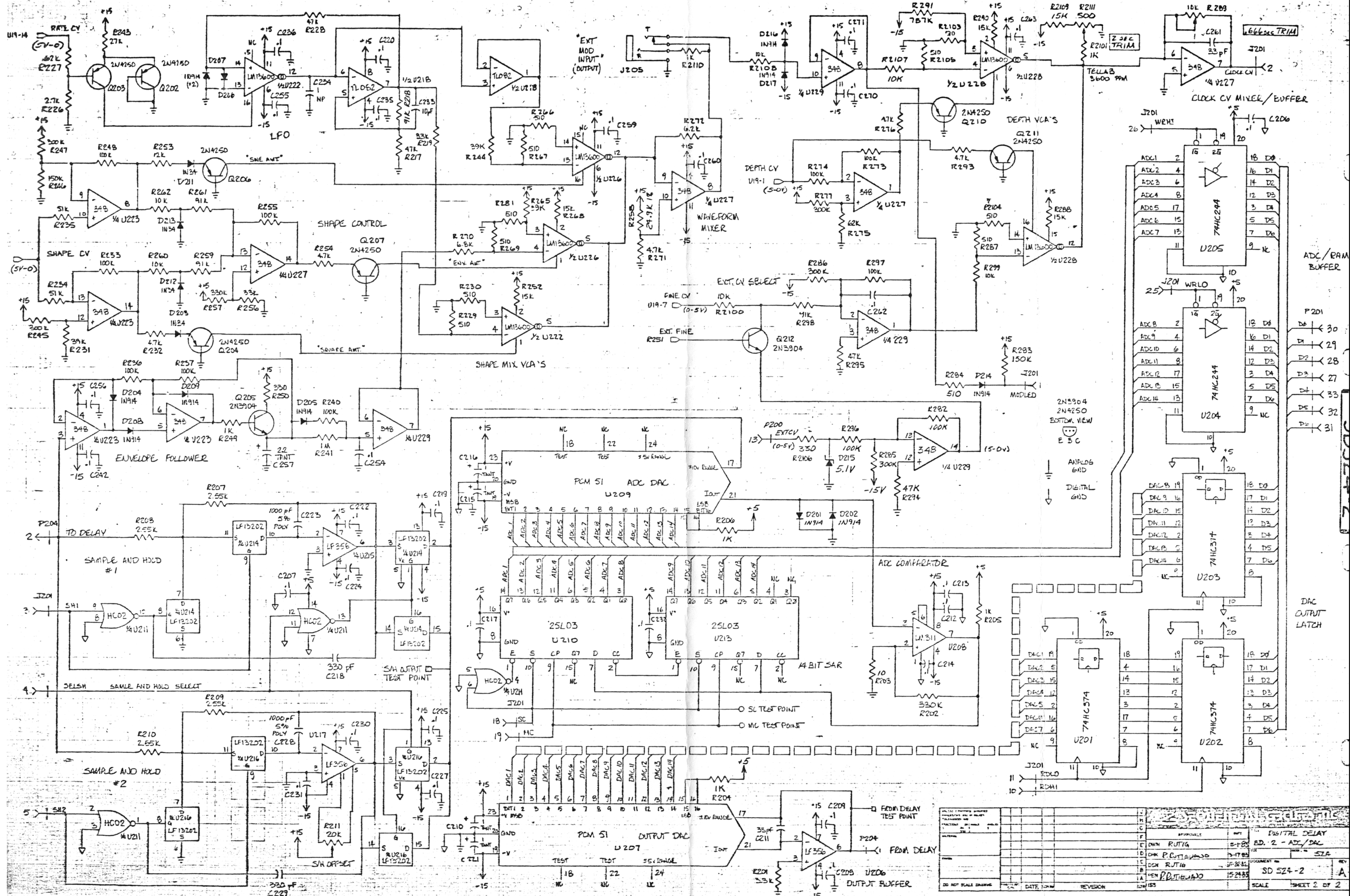
BLOCK DIAGRAM	
DESIGNER: M. FARWIG	DATE: 7/21/68
CHECKER: P. RUTIGLIANO	DATE: 8/1/68
PROJECT: BS 524-2	REV: A
SCALE: SHEET 1 OF 1	

BD 2: ADC/DAC INTERFACE

BD 1: FRONT PANEL BOARD

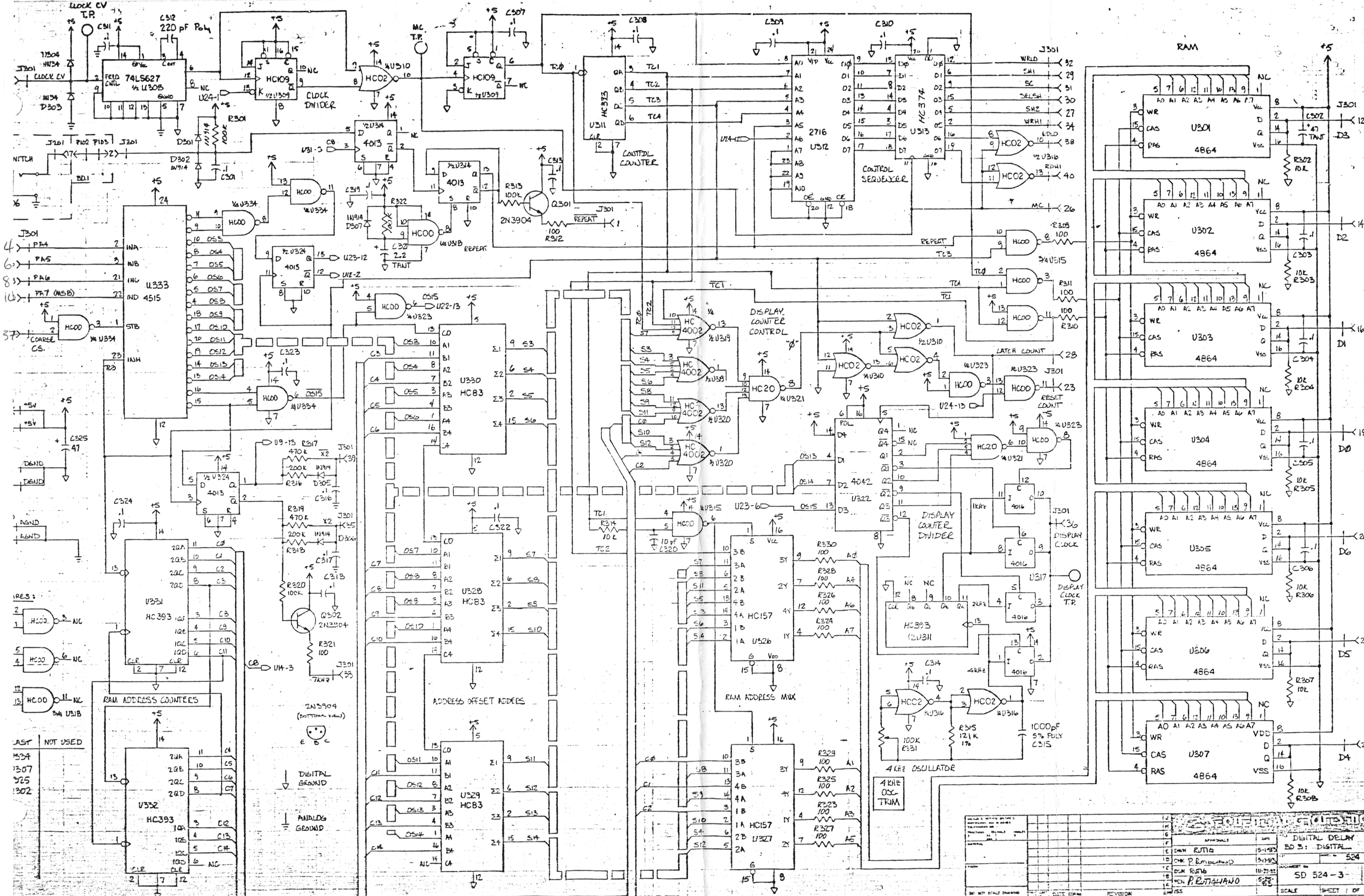


APPROVALS		DATE	DIGITAL DELAY
OWN	RUTIG	5-15-68	BD 1 / BD 2 INTERF.
CHK	P. RUTIG	5-15-68	524
DRG	RUTIG	5-15-68	SD 524-2
APP	P. RUTIG	5-15-68	SCALE
REV			SHEET 1 OF



NO.	DESCRIPTION	DATE	REVISION
1	ISSUED FOR FABRICATION	12-17-83	1
2	REVISED	12-17-83	2
3	REVISED	12-17-83	3
4	REVISED	12-17-83	4
5	REVISED	12-17-83	5
6	REVISED	12-17-83	6
7	REVISED	12-17-83	7
8	REVISED	12-17-83	8
9	REVISED	12-17-83	9
10	REVISED	12-17-83	10
11	REVISED	12-17-83	11
12	REVISED	12-17-83	12
13	REVISED	12-17-83	13
14	REVISED	12-17-83	14
15	REVISED	12-17-83	15
16	REVISED	12-17-83	16
17	REVISED	12-17-83	17
18	REVISED	12-17-83	18
19	REVISED	12-17-83	19
20	REVISED	12-17-83	20
21	REVISED	12-17-83	21
22	REVISED	12-17-83	22
23	REVISED	12-17-83	23
24	REVISED	12-17-83	24
25	REVISED	12-17-83	25
26	REVISED	12-17-83	26
27	REVISED	12-17-83	27
28	REVISED	12-17-83	28
29	REVISED	12-17-83	29
30	REVISED	12-17-83	30
31	REVISED	12-17-83	31
32	REVISED	12-17-83	32
33	REVISED	12-17-83	33
34	REVISED	12-17-83	34
35	REVISED	12-17-83	35
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37	REVISED	12-17-83	37
38	REVISED	12-17-83	38
39	REVISED	12-17-83	39
40	REVISED	12-17-83	40
41	REVISED	12-17-83	41
42	REVISED	12-17-83	42
43	REVISED	12-17-83	43
44	REVISED	12-17-83	44
45	REVISED	12-17-83	45
46	REVISED	12-17-83	46
47	REVISED	12-17-83	47
48	REVISED	12-17-83	48
49	REVISED	12-17-83	49
50	REVISED	12-17-83	50

DIGITAL DELAY
 ED. 2 - ADC/DAC
 SD 524-2
 SHEET 2 OF 2



RES:

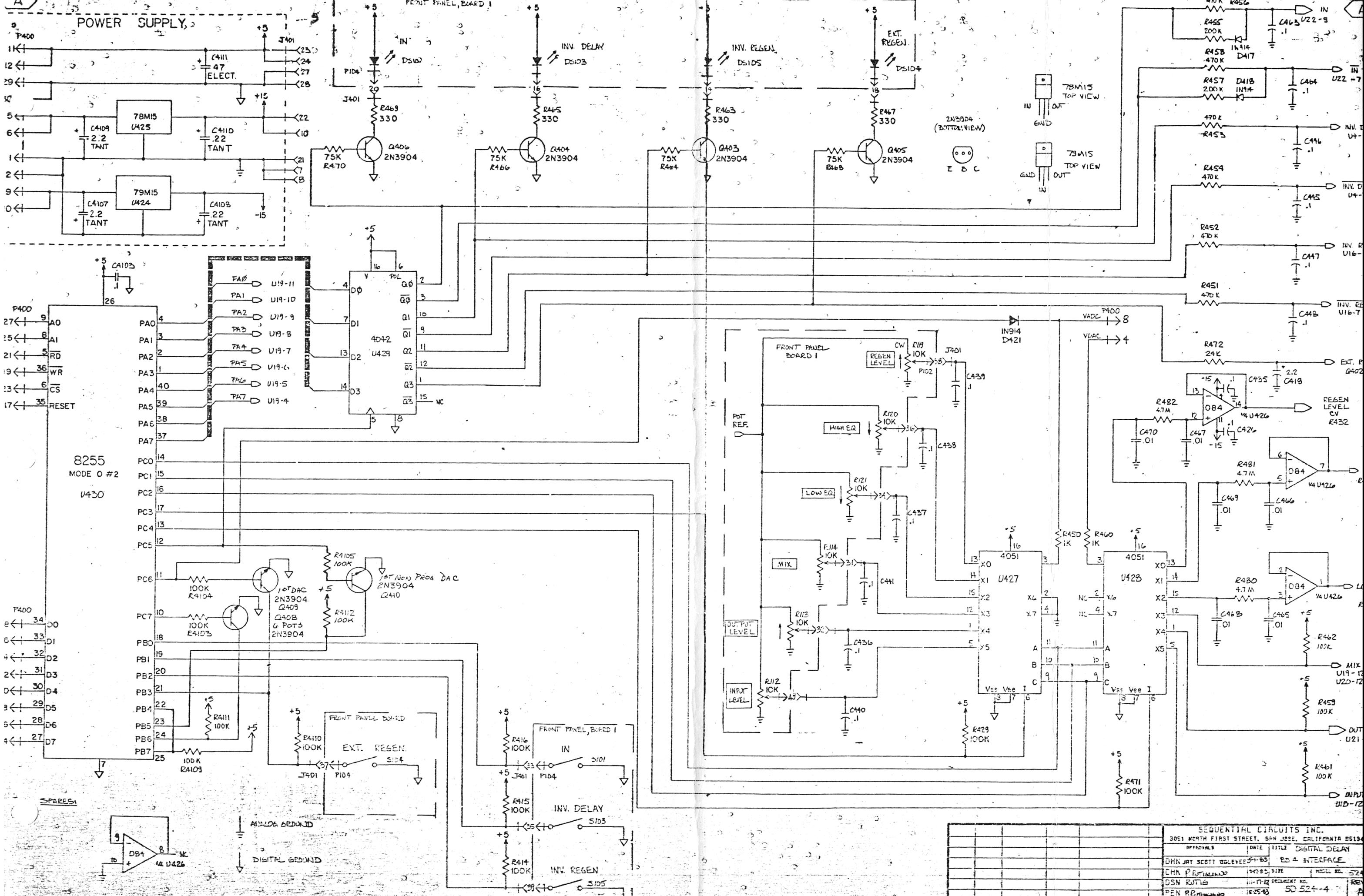
2	HC00	3	NC
5	HC00	6	NC
13	HC00	11	NC

LAST NOT USED

1534	
1307	
325	
1302	

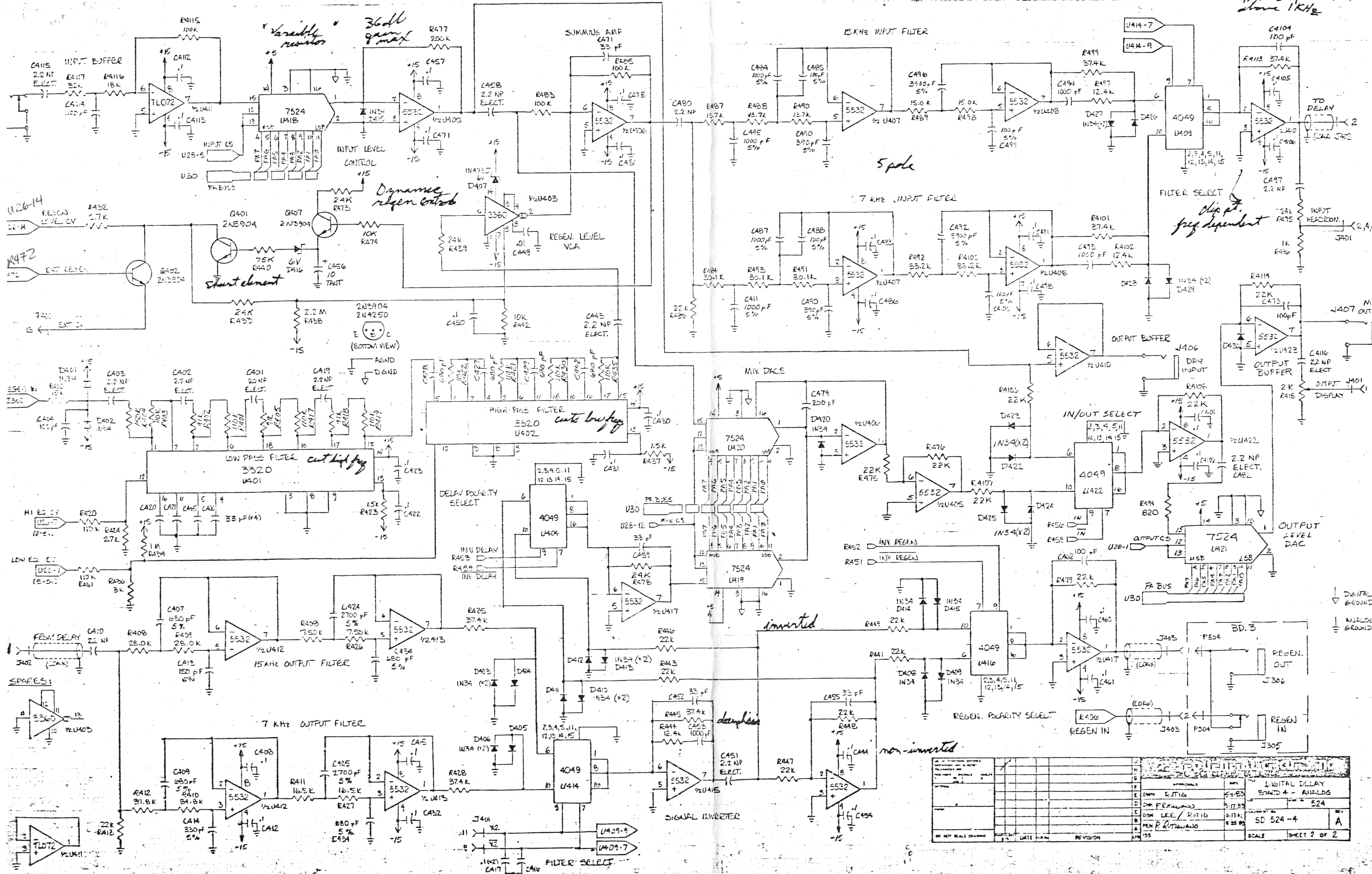
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DIGITAL DELAY
SD 524-3-
REVISION
DATE
SCALE
SHEET 1 OF



SEQUENTIAL CIRCUITS INC.			
3051 NORTH FIRST STREET, SAN JOSE, CALIFORNIA 95134			
APPRAISAL	DATE	TITLE	BY
		DIGITAL DELAY	ED A INTERFACE
DRN JAY SCOTT	05-11-85		
CHN P. RUTING	10-17-85	SIZE	MODEL NO. 524
DSN RUTING	11-17-85	DEPARTMENT NO.	
PEN P. RUTING	12-25-85	50 524-4	REV
FIRST	LAST	DATE	ISS

Pre-emphasis above 1KHz



NO.	DESCRIPTION	DATE	REVISION
1	OWN RIT16	5-1-63	
2	CHK P. RIT16	5-11-63	
3	OWN LEE / RIT16	5-11-63	
4	PEN P. RIT16	5-25-63	

APPROVALS	DATE	REVISION
EDWARD A - ANALDS	5-24-63	
SD 524-4		
SCALE		SHEET 2 OF 2