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**PROPHET-T8**  
**PRELIMINARY SERVICE DATA**  
Manual No. TN1008-0  
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02979-6211  
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### **PRELIMINARY INFORMATION**

**All subject to change.**

#### **GENERAL**

For the following discussion, please refer to the accompanying block diagram and schematics.

The computer contains a Z-80B 8-bit Main processor and a 16-bit Z8002A Final processor, both running at 6 MHz.

The Z-80 Main handles the keyboard and control panel inputs, MIDI, and program and sequence data to constantly update Common RAM with current data in the formats required by the Final. For example some of the knobs act as plus/minus controls. In this case the Main would take the 00-FFH number from the ADC and convert it to a plus/minus two's complement sixteen-bit number with the correct weighting. The Z-80 also latches out switch bits to control the analog switches in the synth.

The Z-8002 Final processor calculates the digital envelopes, LFOs, and generates six final CVs for each of the eight voices (48 total) plus a few miscellaneous CVs. It refers to the Common RAM for data which it processes and sends to a First-In-First-Out (FIFO) buffer from which they are eventually clocked out as control voltages (CVs) to the Sample/Holds.

#### **MAIN SYSTEM**

The Main processor system consists of the Z-80 CPU, 2764 8K EPROM, five 6116LP Non-volatile static RAMS and the MIDI UART. The memory decoder enables only one of these devices at a time to use the Data bus. NV RAM can not be enabled if power is off.

The various input drivers and output latches are selected by chip selects (CSO-out, CSI-in) from the I/O decoder. The CSs clock:

- a decoder for the LED and switch matrices,
- a latch for the LED matrix,
- a driver for the switch matrix,
- a decoder and driver for the keyboard optics,
- a miscellaneous latch for tape output and A-440,
- a miscellaneous driver for tape and footswitch input,
- a latch for programmed volume which drives two level DACs in the audio output stage,
- four latches with synth switch signals,
- two latches which address and select the multiplexer chips which channel the control knobs and pressure sensors to the Analog-to-Digital Converter (ADC), the ADC and ADC driver (input).

A 1-kHz interrupt clock is provided to both processors. In the Main, M1 is ORed with -IORQ to get INT ACK which resets INT FF. The INT FF has to be reset when first entering the interrupt state so the processor doesn't keep seeing INTs.

The Z-80 interrupt handling is much more complicated (in software) than the Z-8002, because the Main is doing keyboard scanning, knob conversion, switch scanning, LED output, MIDI processing. Keyboard scanning is most critical. It must be done on a 1 millisecond (= 1 kHz) basis to give sufficient resolution for velocity. The Main processor scans the entire keyboard every interrupt cycle. To prevent flickering, the LEDs are also strobed each cycle. Other tasks are accomplished on successive interrupt cycles. The knobs are read in background mode (in the time between the end of the interrupt handler and the appearance of the next INT).

Writing to the low-power RAMS (except Scratchpad) is enabled by a bit from the miscellaneous latch. The signal encounters an RC delay then enables writing (-WR) through an OR-gate. This hardware protects the memories against power-down problems.

## FINAL SYSTEM

The Final processor system consists of the Z-8002, two 2732 EPROMS (4K words), the 8253-5 Timer/Counter for Tune and A-440, and the 64-word deep FIFO which is decoded as a single memory location. The Tune control latch is also memory-mapped. The Final Address bus is latched off of the Final Address/Data Bus by a latch driven by AS.

The Z-8002 clears its interrupt with a signal from the status decoder. It only processes every third INT (3 ms). (This gives the envelopes 3 ms. resolution.) Each time it undertakes the same routine for CV calculation. In its spare time (background mode) it processes key on/off information which has been received from the Main.

At the beginning of each interrupt cycle, the Final does a high-speed block move of 59 words to the FIFO. Output Ready (OR) goes high. The processor continues with other tasks while the hardware synchronizes FIFO output to the 14-bit DAC and CV Demultiplexer. The most significant bit of the first word in the FIFO is set, which becomes the S/H CLR signal. This resets the dual 4-bit counter which generates the S/H demultiplexer addresses. Clocked at 62.5 kHz, the counter increments and writes Vdac to each S/H until the FIFO is empty as indicated by OR low.

## COMMON RAM AND ARBITRATION

The Main and Final Data busses interface Common RAM through transceivers which are governed ultimately by the Arbitration logic. The Main or Final Address busses define Common RAM locations through an Address bus multiplexer (selector) which is controlled by Z-80 and Z-8002 requests.

Optimized toward the Final processor, Common RAM is sixteen bits wide. The Z-80 can only access one byte at a time of course, so its Common RAM logic is a little more extensive than the Z-8002's because upper or lower bytes have to be selected.

For the Arbitration logic, both processors have REQUEST signals which are decoded memory addresses, ENABLE signals which turn on their Common RAM transceivers, and WAIT signals which tell them to pause. The Final has priority. Actually, neither processor enters a wait state unless there is contention for Common RAM. If both processors request RAM simultaneously, the Main must wait.

## SCALING PROCEDURE

Scaling is required periodically, and after any power supply repairs.

1. Allow the unit to warm-up for at least 1/2 hour.
2. Center MASTER TUNE.
3. Center the PITCH wheel.
4. Lower the MOD wheel fully off.
5. Hold RECORD and press PROGRAM/SEQUENCE SELECT #3. This calibrates the wheels.
6. Open the top. Do not unmount any PC boards.
7. Hold A-440 and press TUNE. This activates the computer scaling routine. The routine proceeds by scaling OSC 1A, 1B, and FILT 1, OSC 2A, 2B ...through FILTER 8.
8. Observe the SAVE TO TAPE LED, which may either be lit or unlit. Trim OSC 1A scale trimmer to the point where the LED toggles on and off. There is some hysteresis in the trim--just get it as close as you can.
9. To advance to the next adjustment, press TUNE. In this case this brings up OSC 1B.
10. Advance to the FILT 1 and remaining trims by again pressing TUNE. If you lose track of what trim is appropriate, you can identify active oscillators by probing their pin 8 with a scope, which should show a sawtooth wave. Tuning filters can be identified by a sine wave on their pin 17.
11. After FILTER 8 has been trimmed, the Prophet-T8 will return to normal mode, with the A-440 signal providing audible indication of the end of the procedure.
12. It may be necessary to press TUNE several times to get the instrument into proper tune.



## 2-XX TUNE

Another feature of analog/digital technology is represented by the T-8 in the tune system. The accuracy of instrument performance is dependant upon the tune system's reliability to keep all sixteen oscillators and eight filters corrected constantly.

Tune occurs in two parts. At power-up, the system accurately measures both oscillator and filter frequencies (In a consecutive order from voice 1 to voice 8) through a nine octave range, and correlates the precise CVs necessary to create perfectly tuned octaves. The system uses a technique called successive approximation. In successive approximation, the recorded count of the analog pulse is compared to a reference count represented first by the DAC MSB. The computer sets the MSB as long as the pitch does not exceed the reference. This procedure is repeated, setting all fourteen DAC bits in order of the MSB to the LSB. The difference between the actual (14-bit, 65 $\mu$ V) and hypothetical (83mV-step) CVs is called tuning "biases". The second part of tuning is active while playing, because the individual bias for the oscillators and filters are recalculated for each keystroke by the computer, and is then corrected for the note that is designated.

Like the Prophet 600, there is no tune multiplexer. Initially, U348-15 TUNE SELECT (TUNE SEL) controls U506 4053 analog switch, which selectively routes AUDIO LEFT (AUDIO L) for voices 1-4 and AUDIO RIGHT (AUDIO R) for voices 5-8 to the TUNE COMPARATOR (TUNE CPR). The computer then selects in order the oscillators and filters which drive U505 TUNE CPR (refer sheet J). TUNE CPR converts OSC and FILT references into pulses. R515 is placed in the feedback loop to prevent oscillations. U345-15 ENABLE TUNE (EN TUNE) acts as a pull-up reference at U505-7 output. The output is sent back to PCB-3 for counting in the tune circuit (refer sheet D).

The squared-up OSC/FILT pulses are attenuated through R316 and into U347-12 AND GATE. The computer generates a pulse from U345-2 to U347-13. This pulse serves as a "fake clock" which initializes the one-shot counter of U349 8253-5 Programmable Interval Timer. The PIT includes three independent 16-bit presettable down counters. CNTR 0 is programmed to count one oscillator pulse, but needs the fake clock to begin the count.

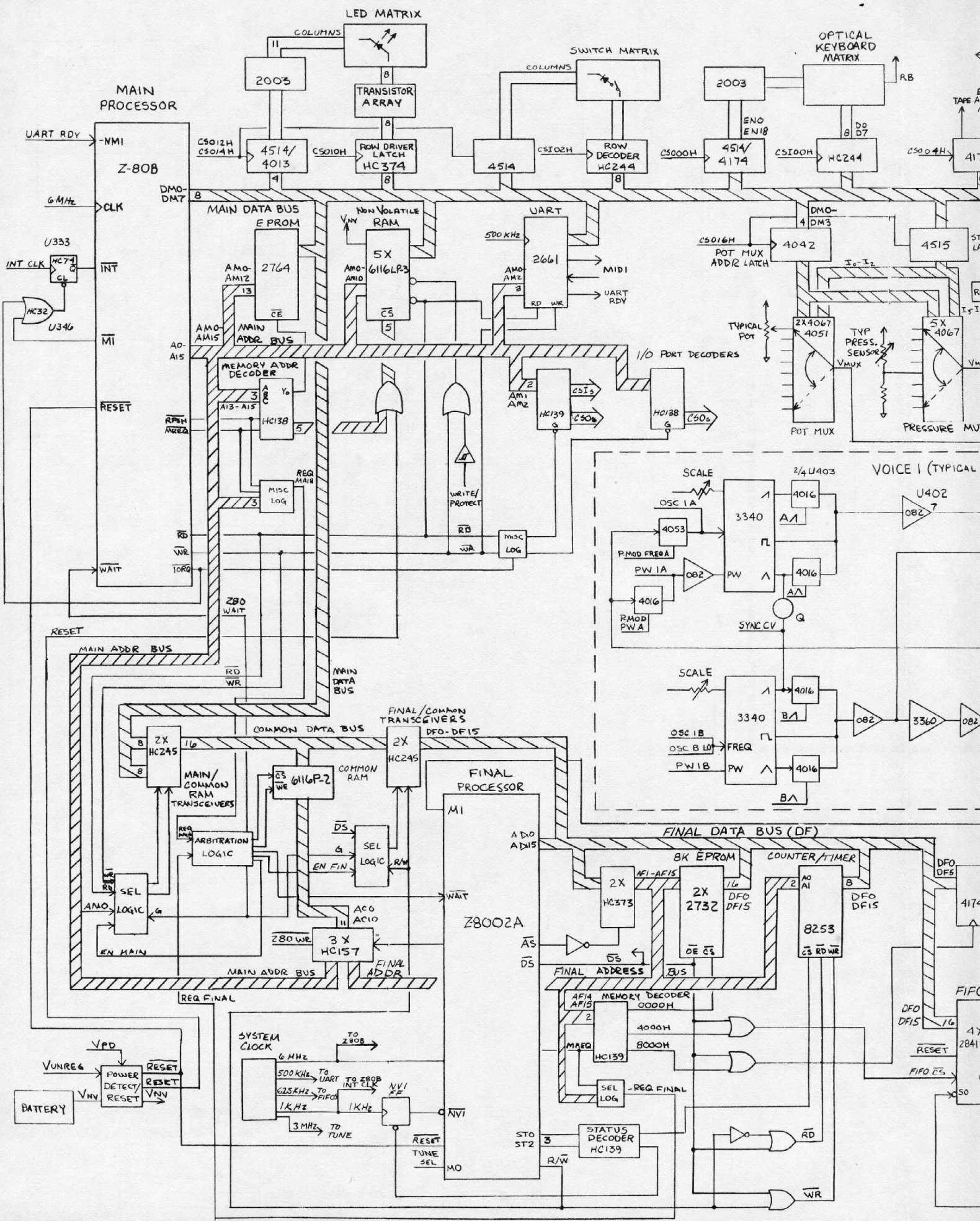
U345-5 latches the gate (G) signal to U349-11, which enables the cycle counter. Then it outputs the fake clock pulse to gate U347-11 high to begin the single count. When the cycle counter receives the first falling edge, the output (pin 10) goes low. Pin 10 is also connected to MULTI MICRO IN (MI) of U348-7 microprocessor. This monitors the state of the one-shot so that the computer knows when to read the total time counter (CNTR 1). The output of CNTR 0 is then inverted, gating on CNTR 1, which will count at a 3MHZ rate. Because CNTR 0 is programmed for a single count, at the next falling edge pin 10 goes high, stopping CNTR 1. CNTR 1 is used to count the amount of 3 MHZ cycles during the analog represented pulse, which is then read through the DATA BUS. The difference between this number of cycles and the given reference causes the CPU to conform S/H CV and sample the given control.

In tuning an oscillator from octave C3 to C4, the reference count is halved because one cycle at C4 approximates half the 3MHZ clock cycles at C3. The reference count



remains the same at octaves C5 - C9, as CNTR 0 doubles its cycle count ( 2,4,....  
....32). Because of the amount of time it would take to count pulses for C0 - C2,  
at the low octaves, this information is extrapolated from the curve described  
by C3 - C9 located in the bias table.

A-440 is activated from U319-5 ENABLE 440 (EN 440) to CNTR 2, U349-16. CNTR 2  
divides 3MHZ by 6818 to produce the 440-Hz square wave. EN 440 connects from  
P301-8 to P602-8 as control for 3/4 U607. When EN 440 is low, output 11 is disabled  
blocking any signal from CNTR 1. At this time output 9 is also disabled, allowing  
control pin 5 to be pulled high by R630, enabling this section which grounds out  
any leakage from pin 11. When EN 440 goes high, pin 6 goes high causing both pin  
9 and control pin 5 to be grounded, which causes pin 3 to "float". At the same  
time control pin 12 is high, allowing the 440 Hz signal to pass at pin 11. A-440  
is then inputted at AUDIO L and R at U609-6,9 (refer sheet M).



**MAIN PROCESSOR**

Z-800B

**LED MATRIX**

COLUMNS

**SWITCH MATRIX**

COLUMNS

**OPTICAL KEYBOARD MATRIX**

RB

2003

2003

4514/4013

4514

4514/4174

2764

5X 6116LR3

2661

4042

4515

HC138

HC139

2X 4067

5X 4067

HC138

HC139

3340

3340

4016

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4053

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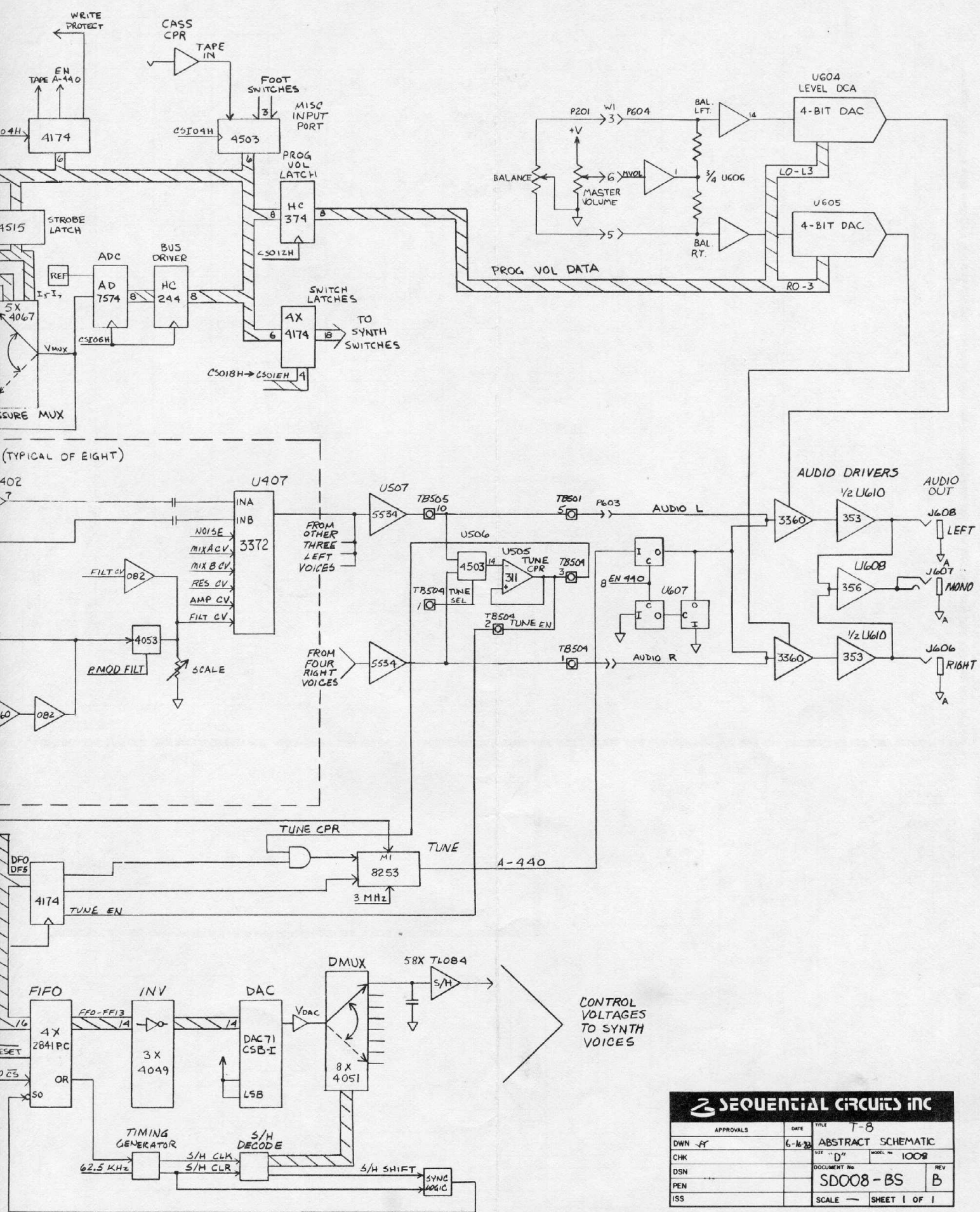
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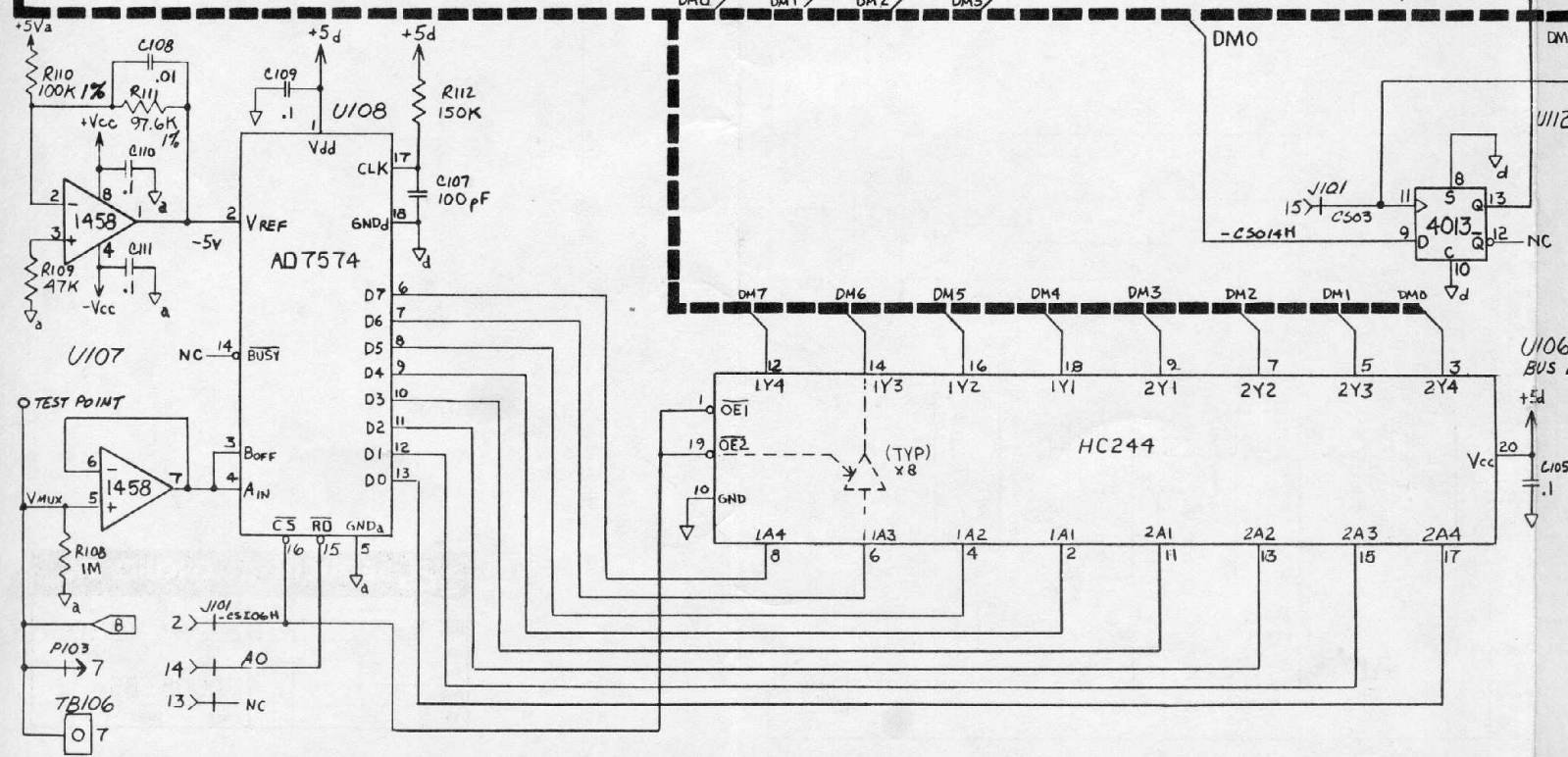
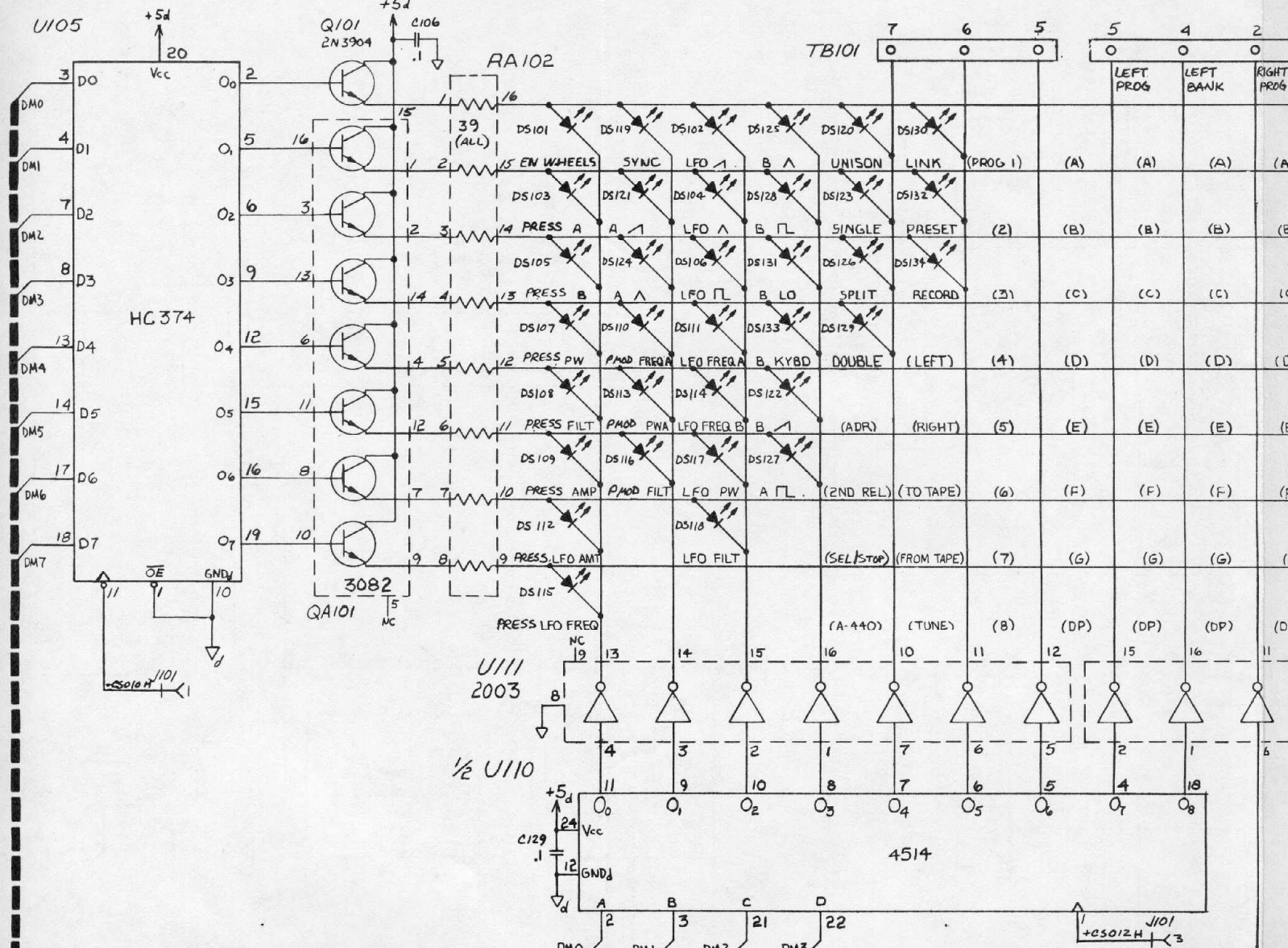
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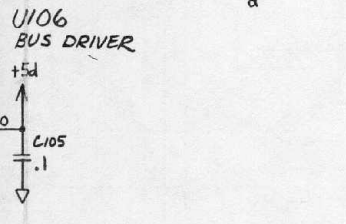
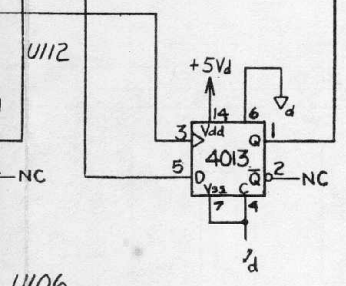
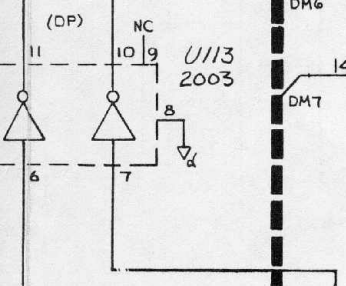
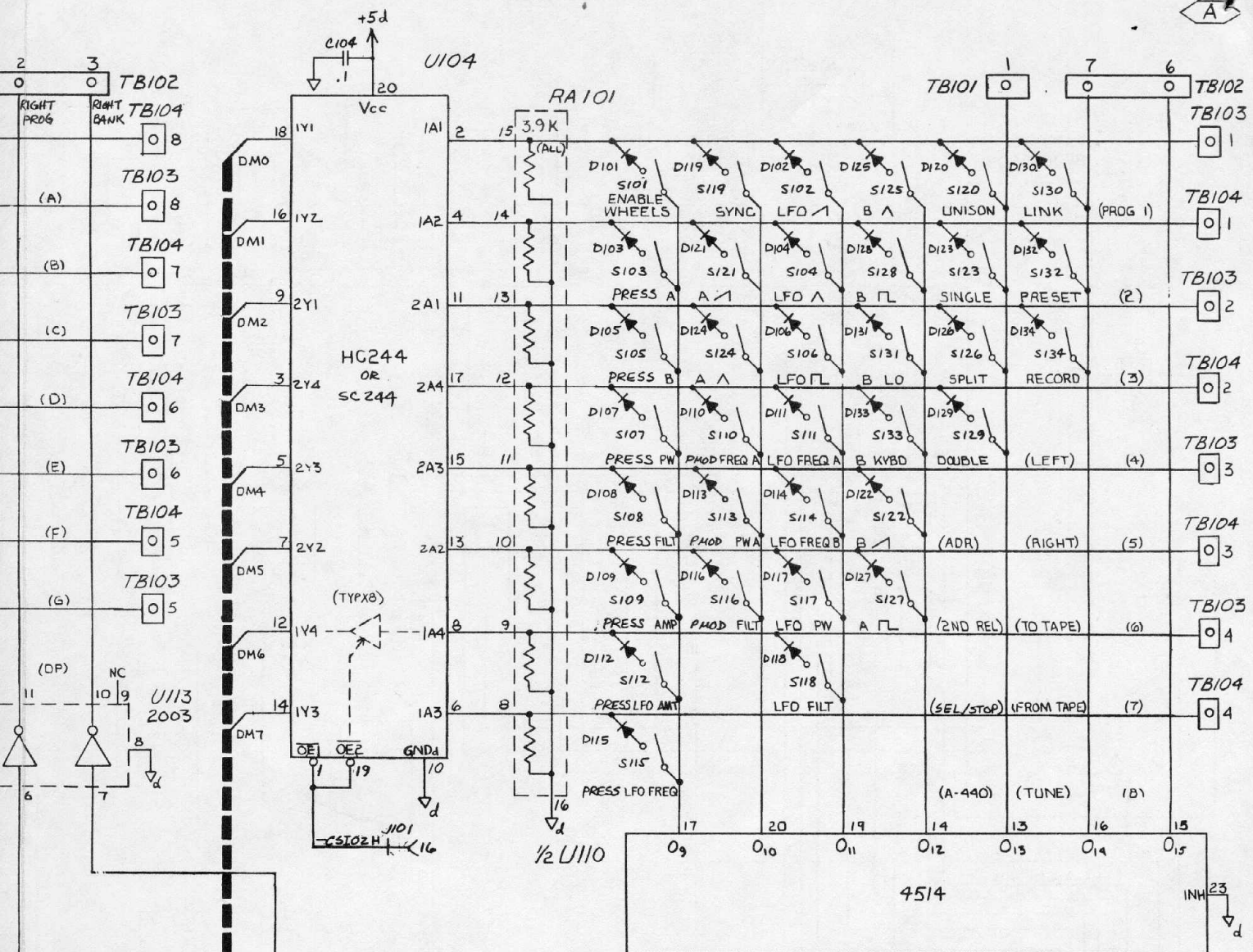


CONTROL VOLTAGES TO SYNTH VOICES

SEQUENTIAL CIRCUITS INC				
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DSN			S0008-BS	B
PEN			SCALE	SHEET 1 OF 1
ISS				

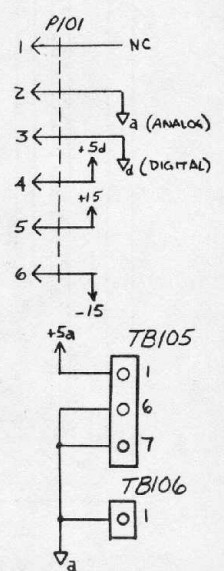
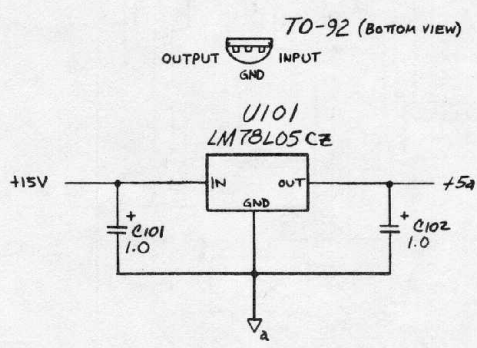
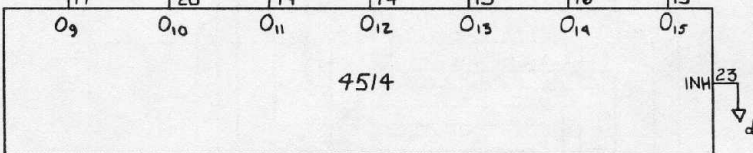
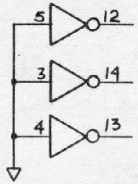






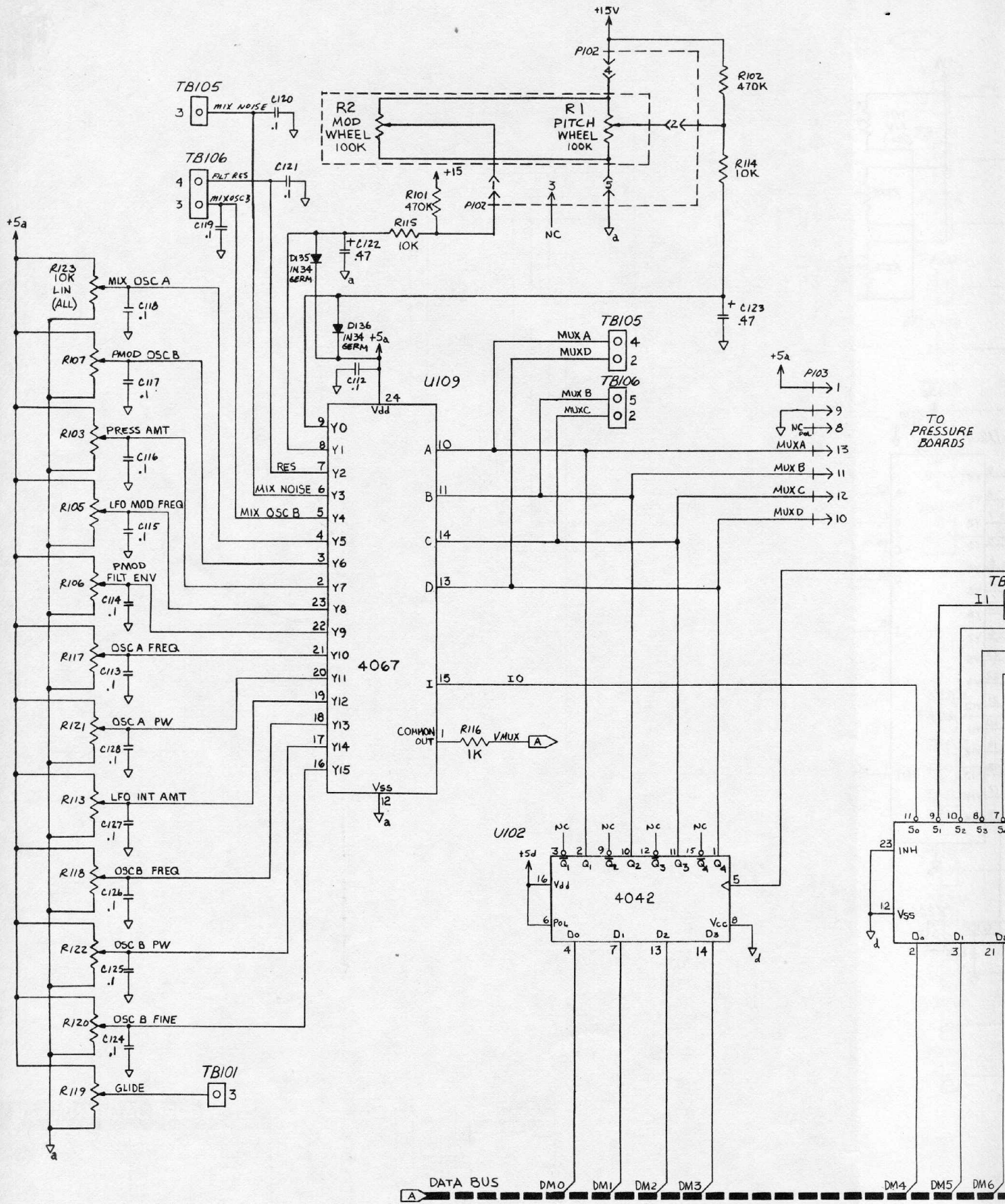
DATA BUS

SPARES:  
U113



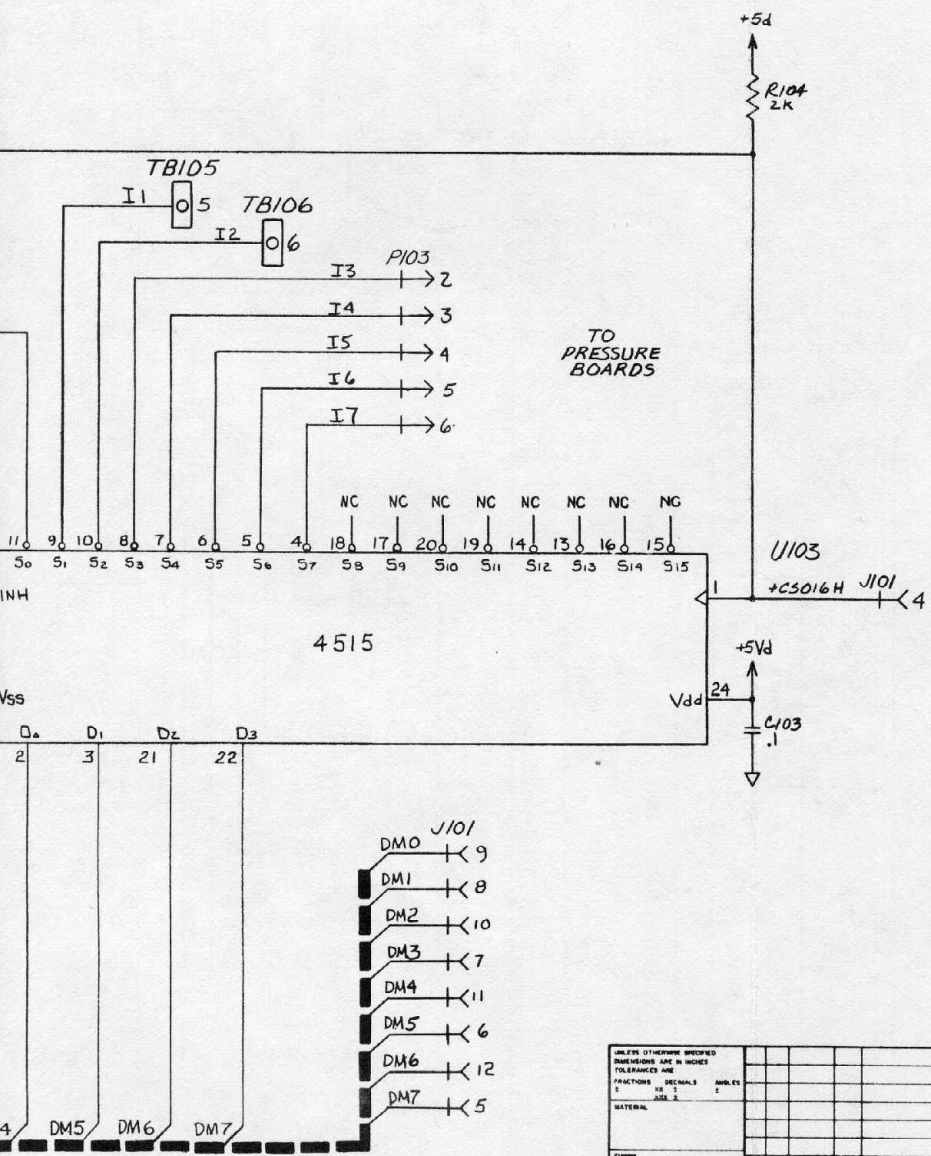
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		D	DSN		DOCUMENT NO. SD008-1
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DATE	REV. NO.	REVISION			







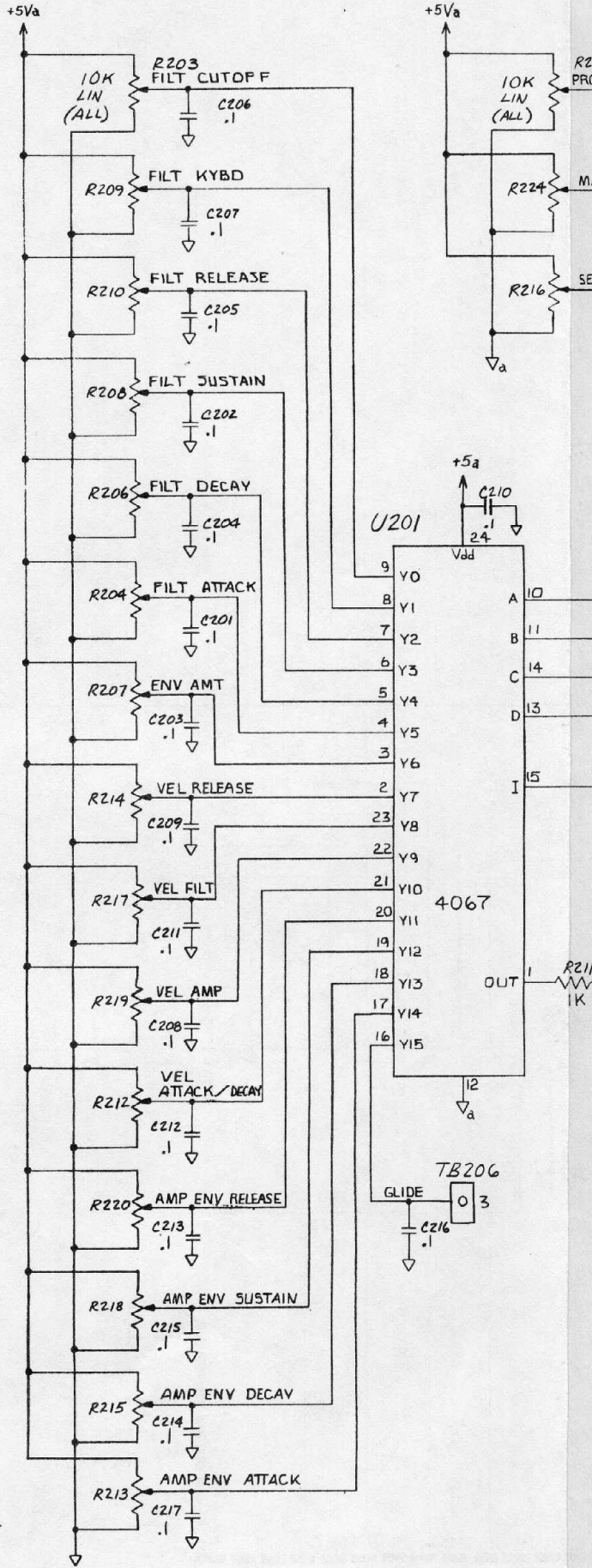
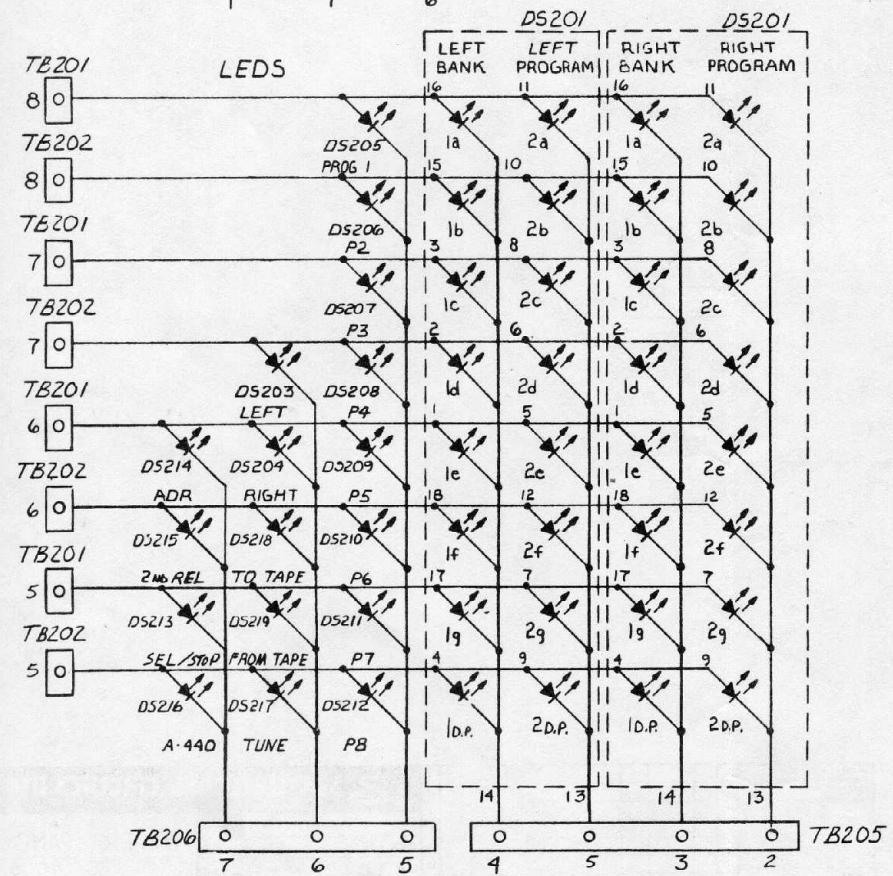
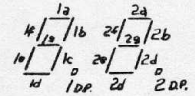
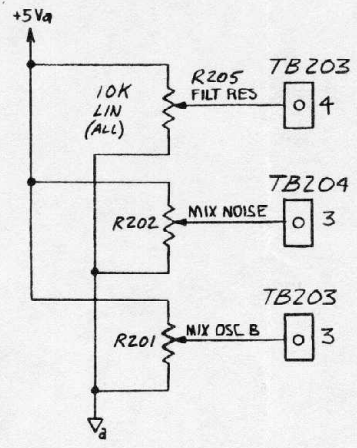
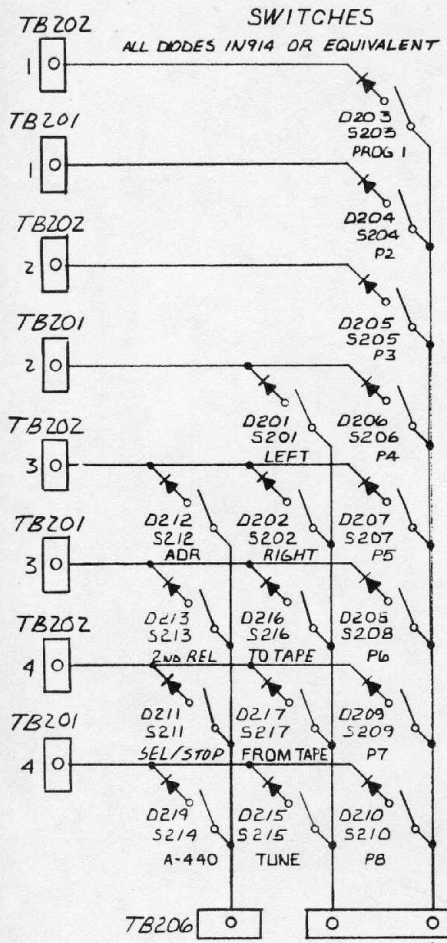
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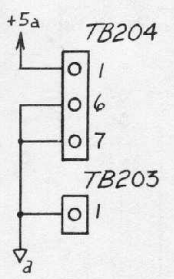
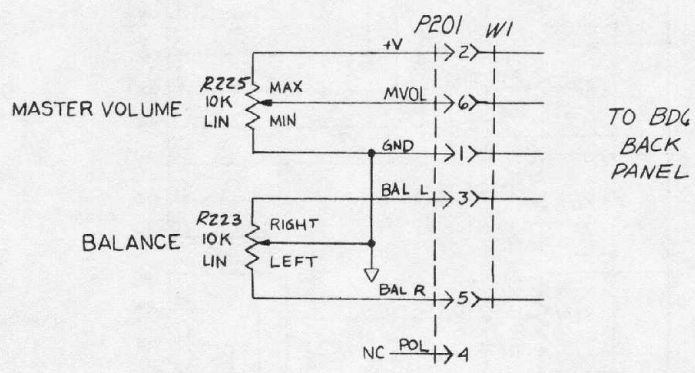
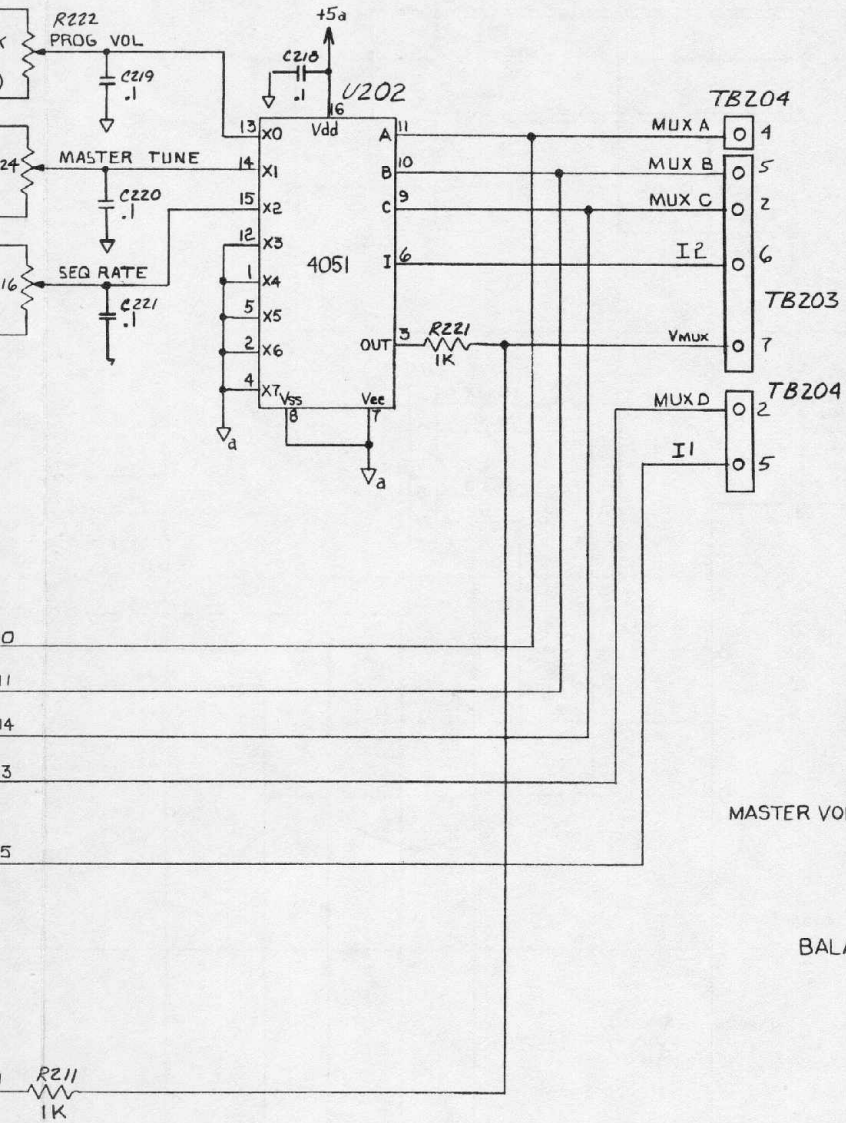


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**SEQUENTIAL CIRCUITS INC**

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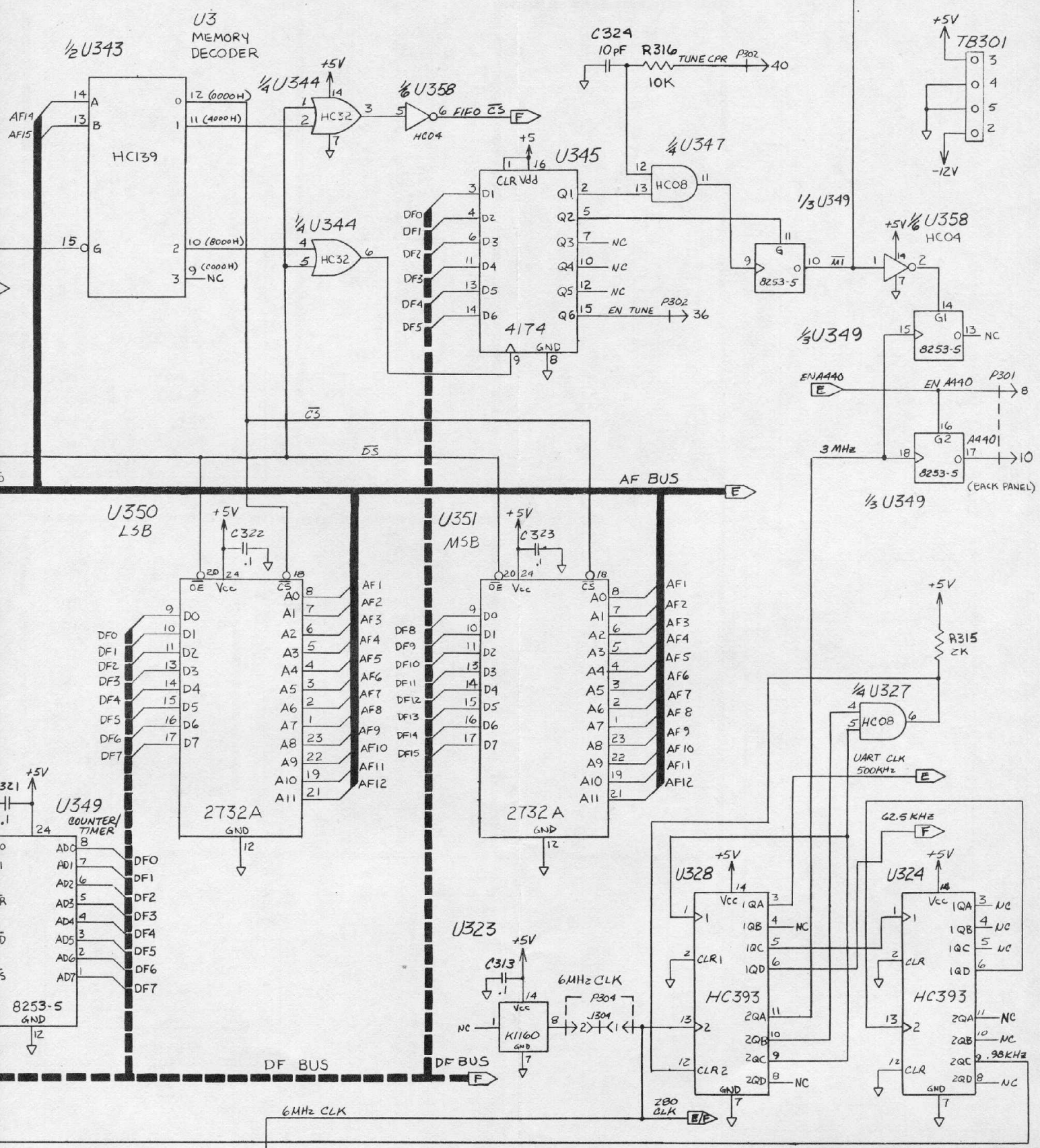




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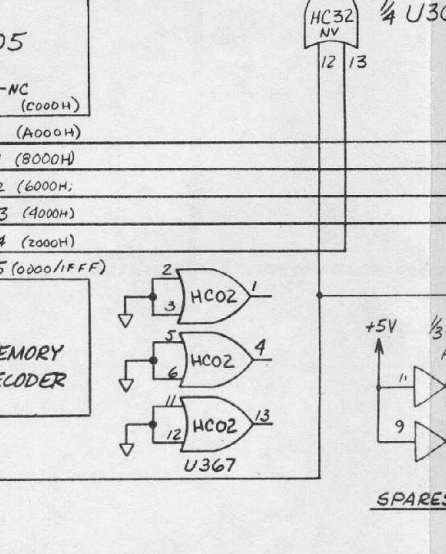
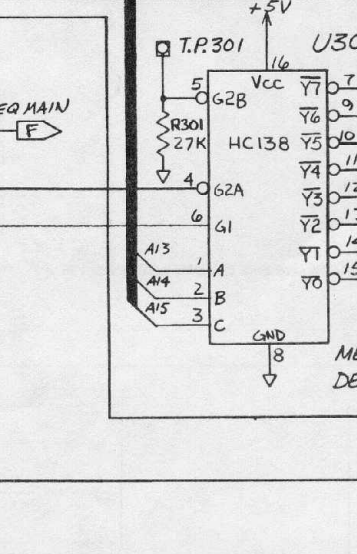
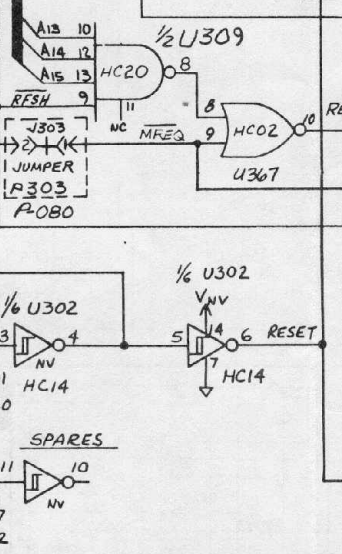
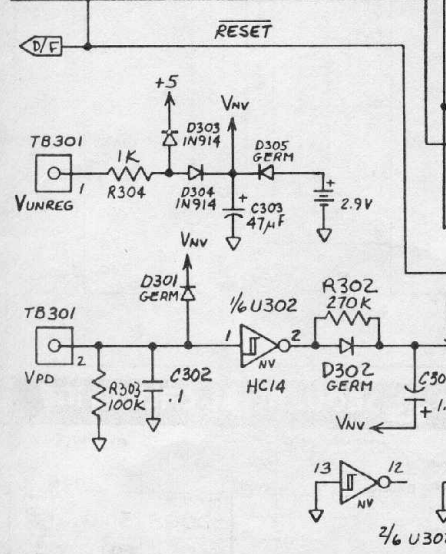
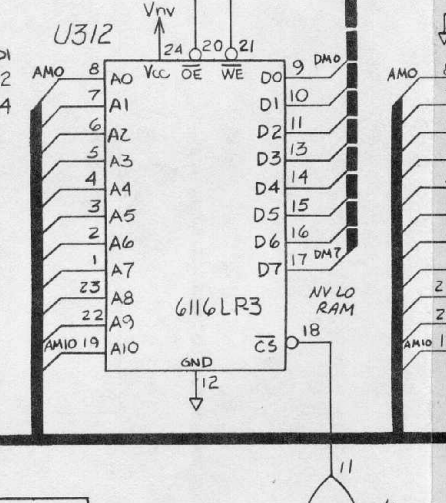
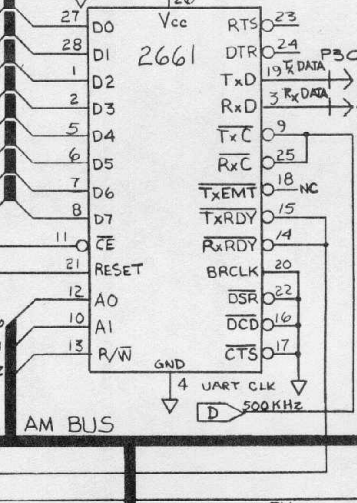
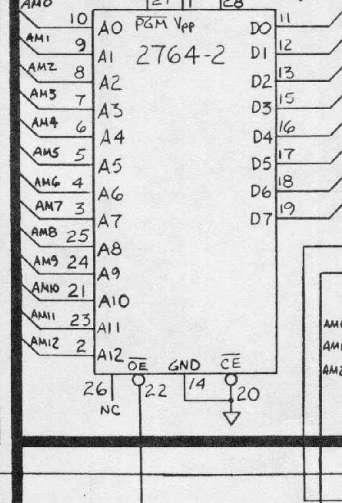
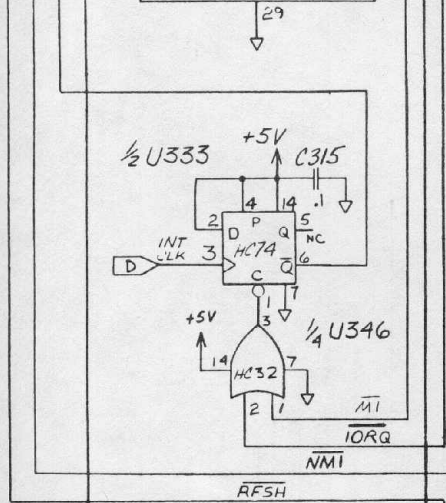
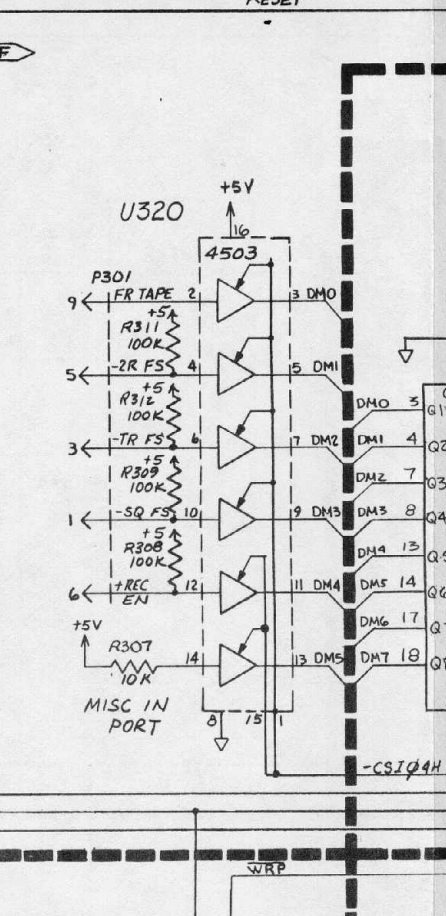
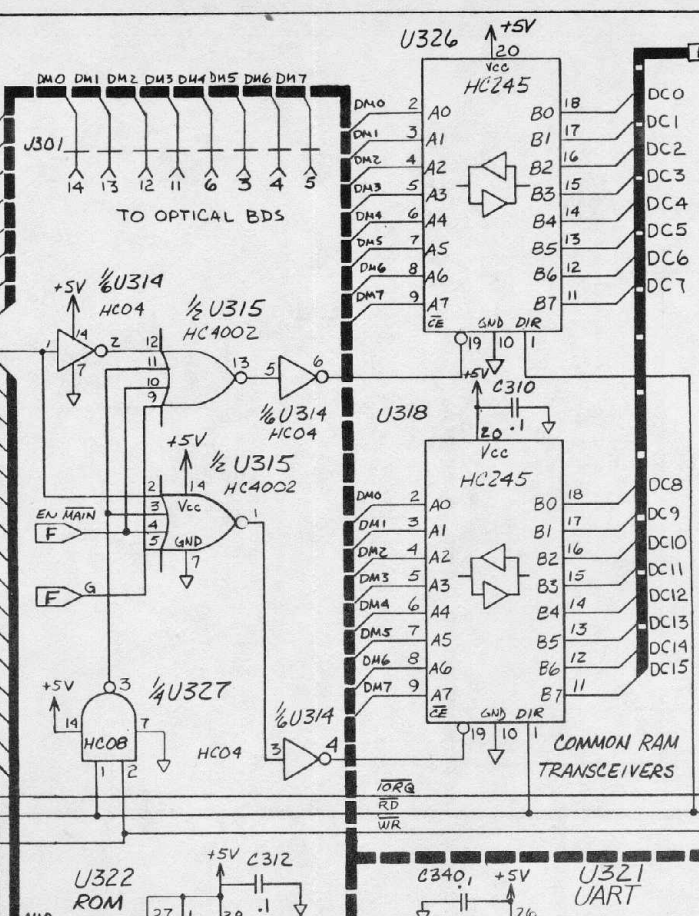
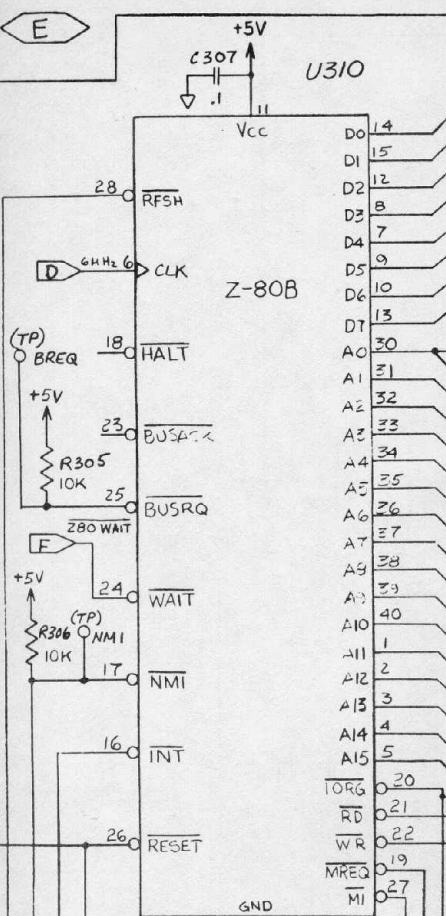
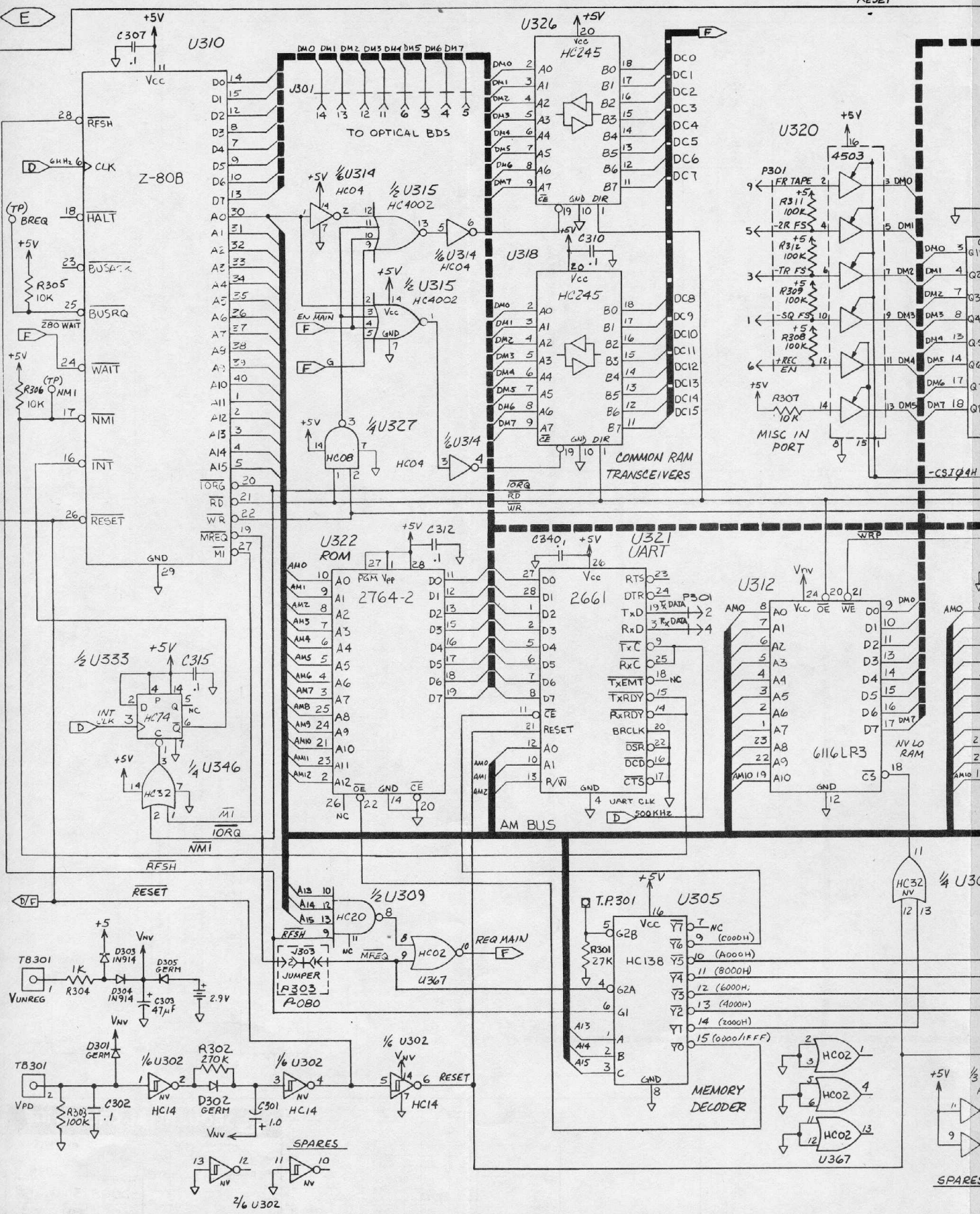




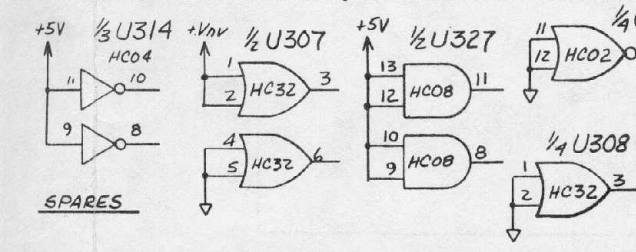
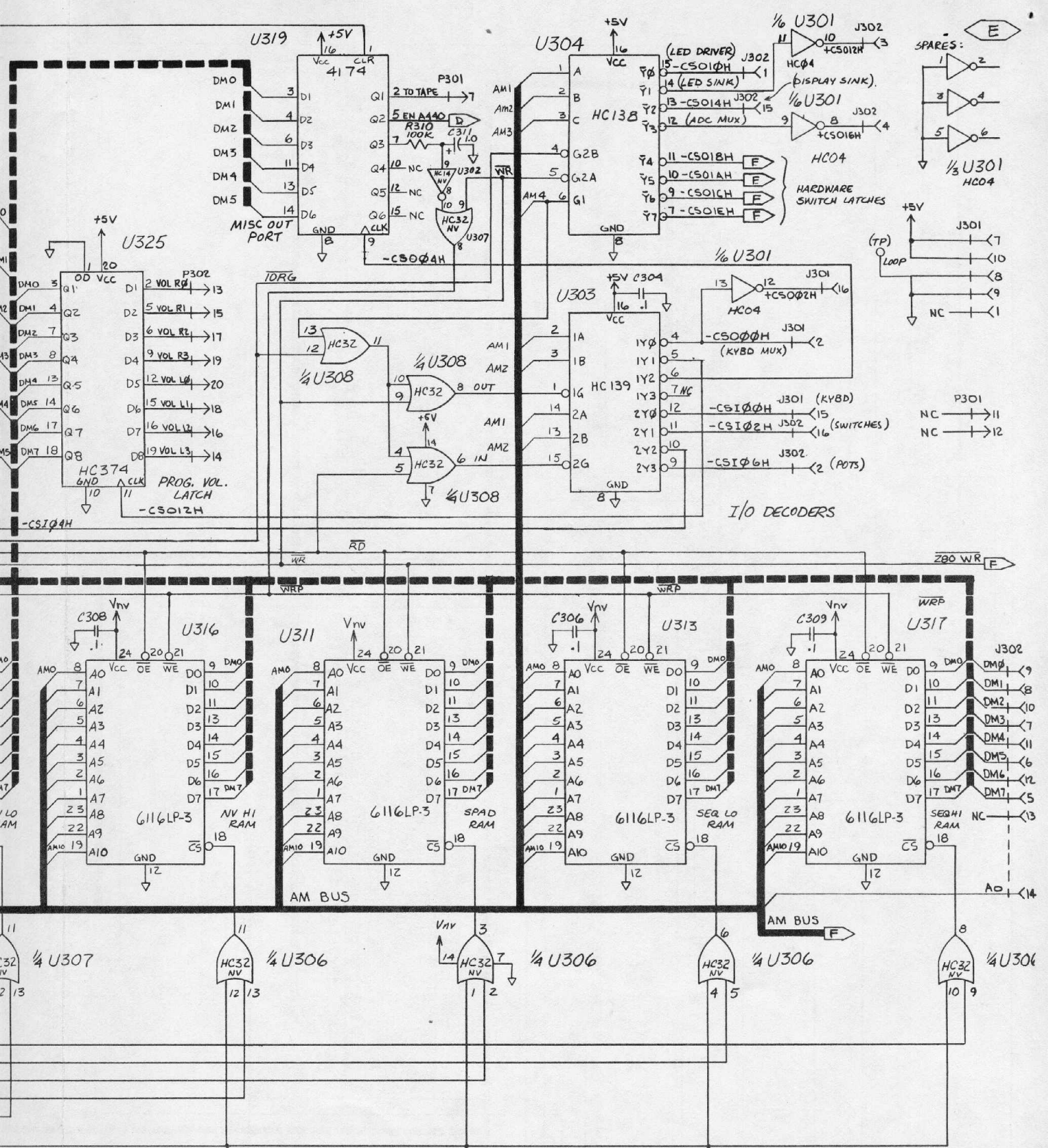
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D	CHK	Donna	6/19/85		
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B	PEN				SD008-3
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UN	ISS				SCALE
					SHEET 1 OF 3



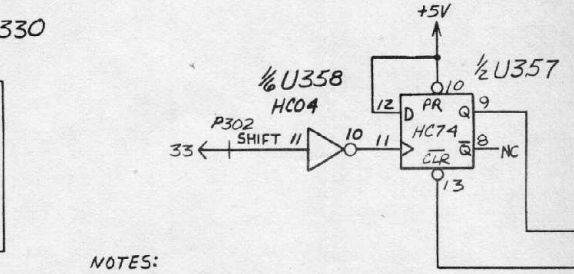
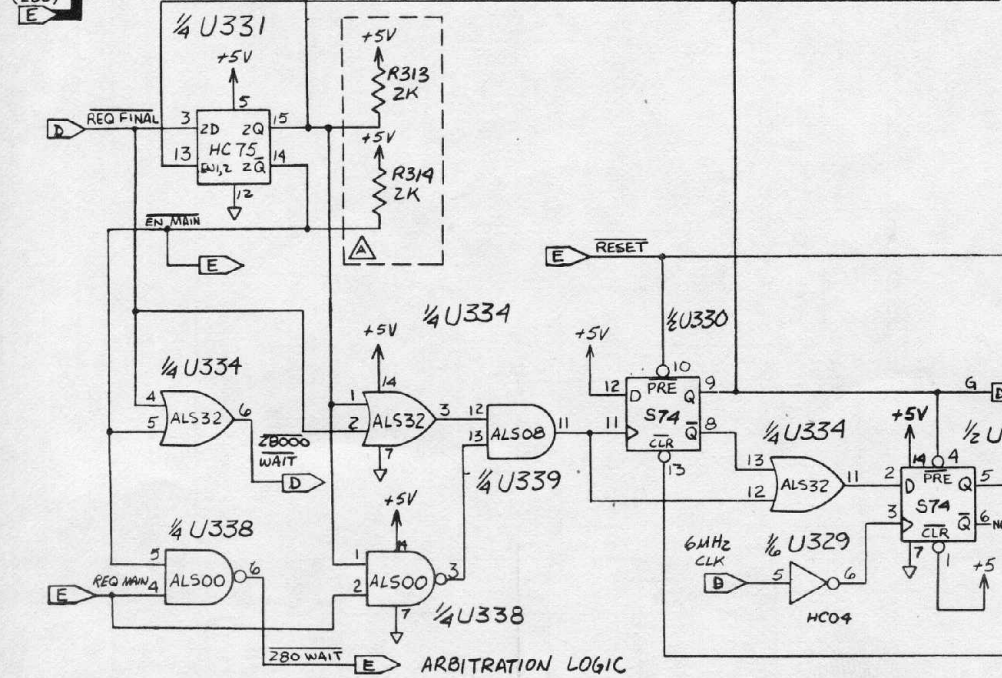
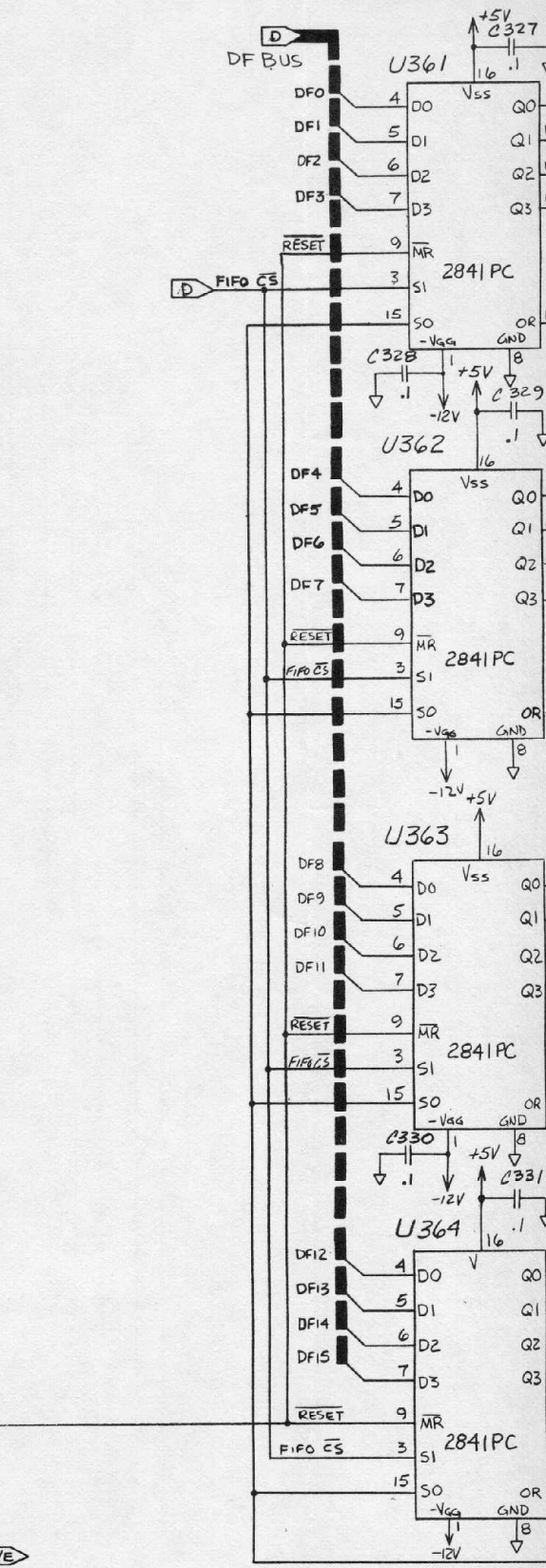
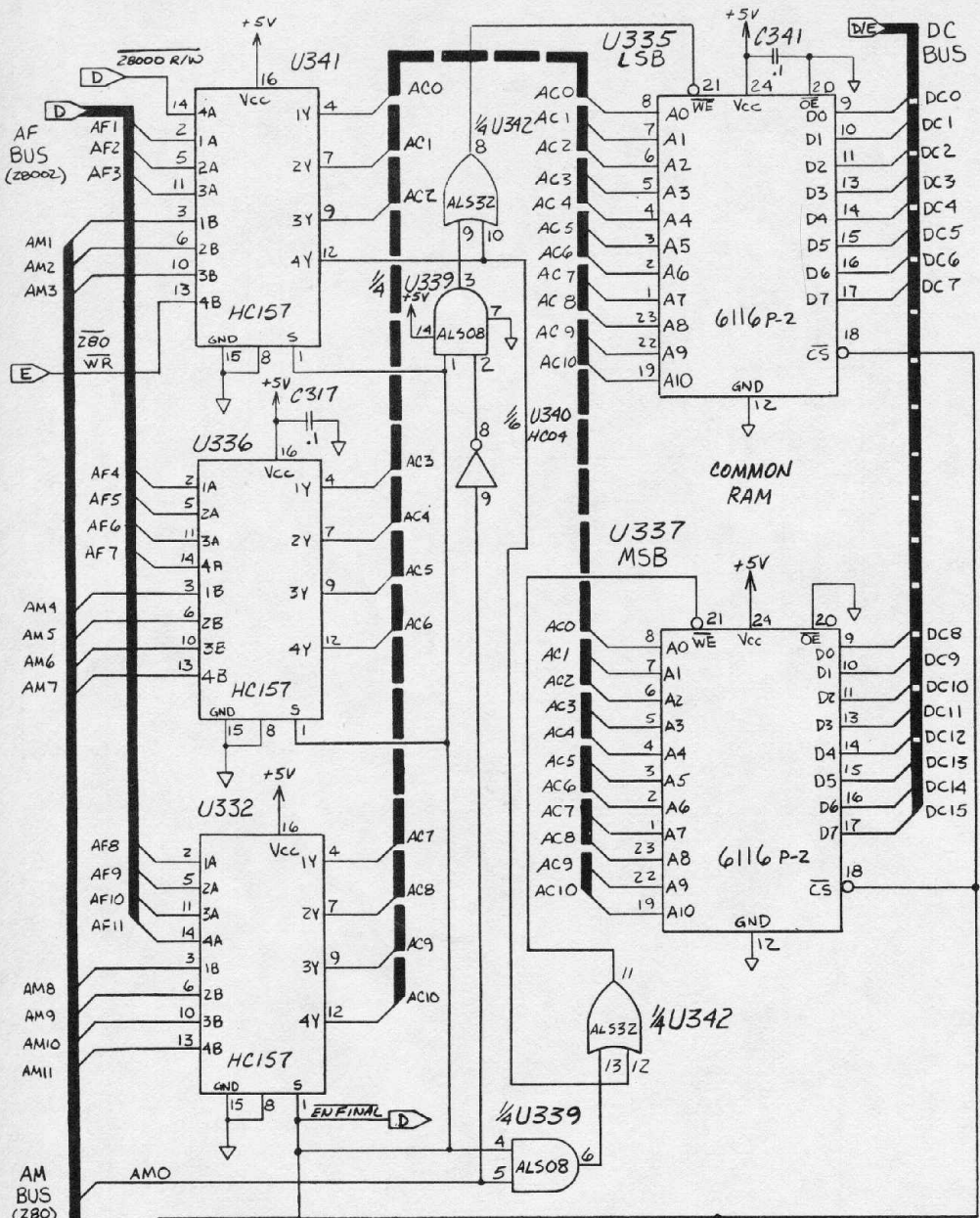
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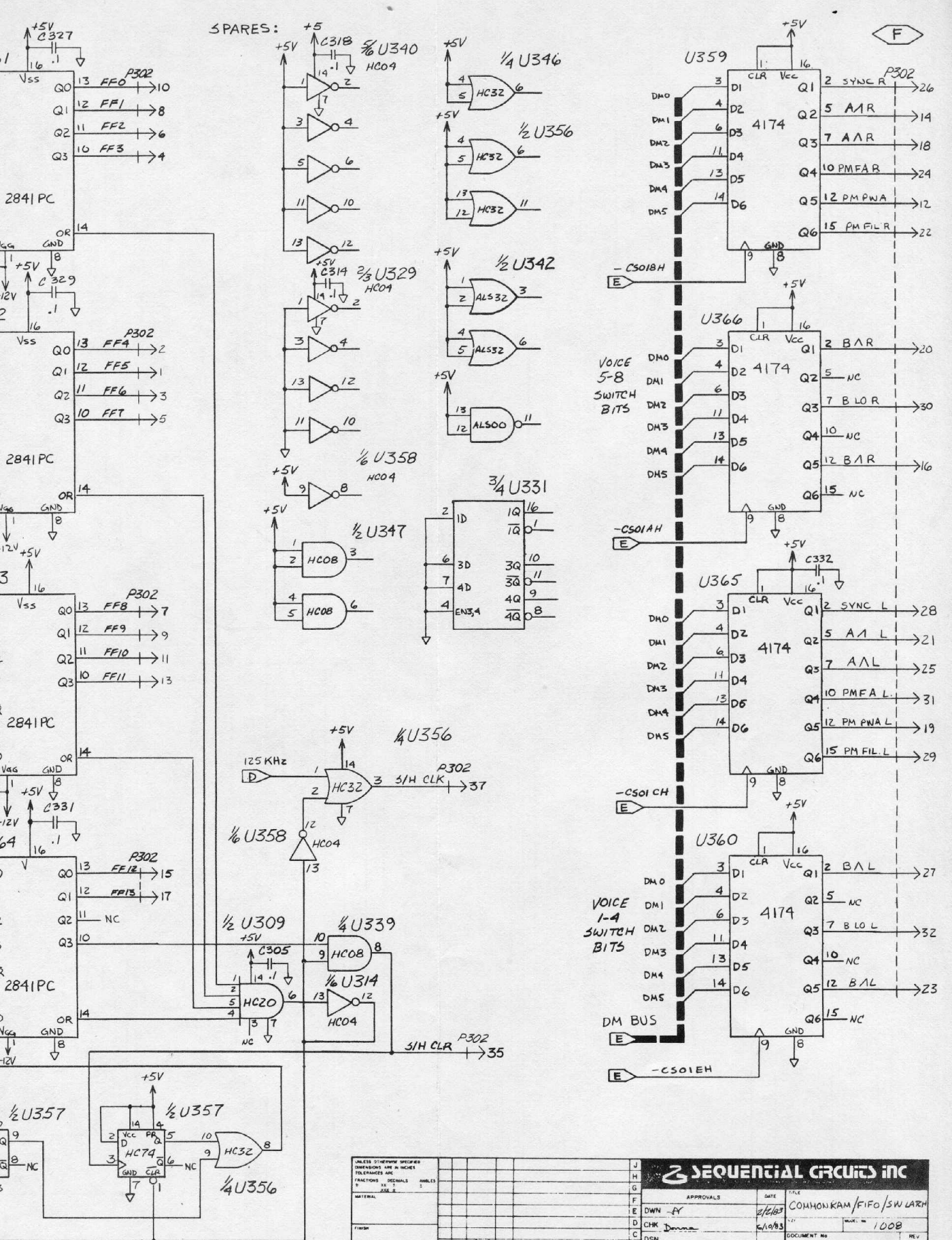


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F			
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UTN			SHEET 2 OF 3
DO NOT SCALE DRAWING	FIRST LAST S/N	DATE	REVISION
		5/31/83	

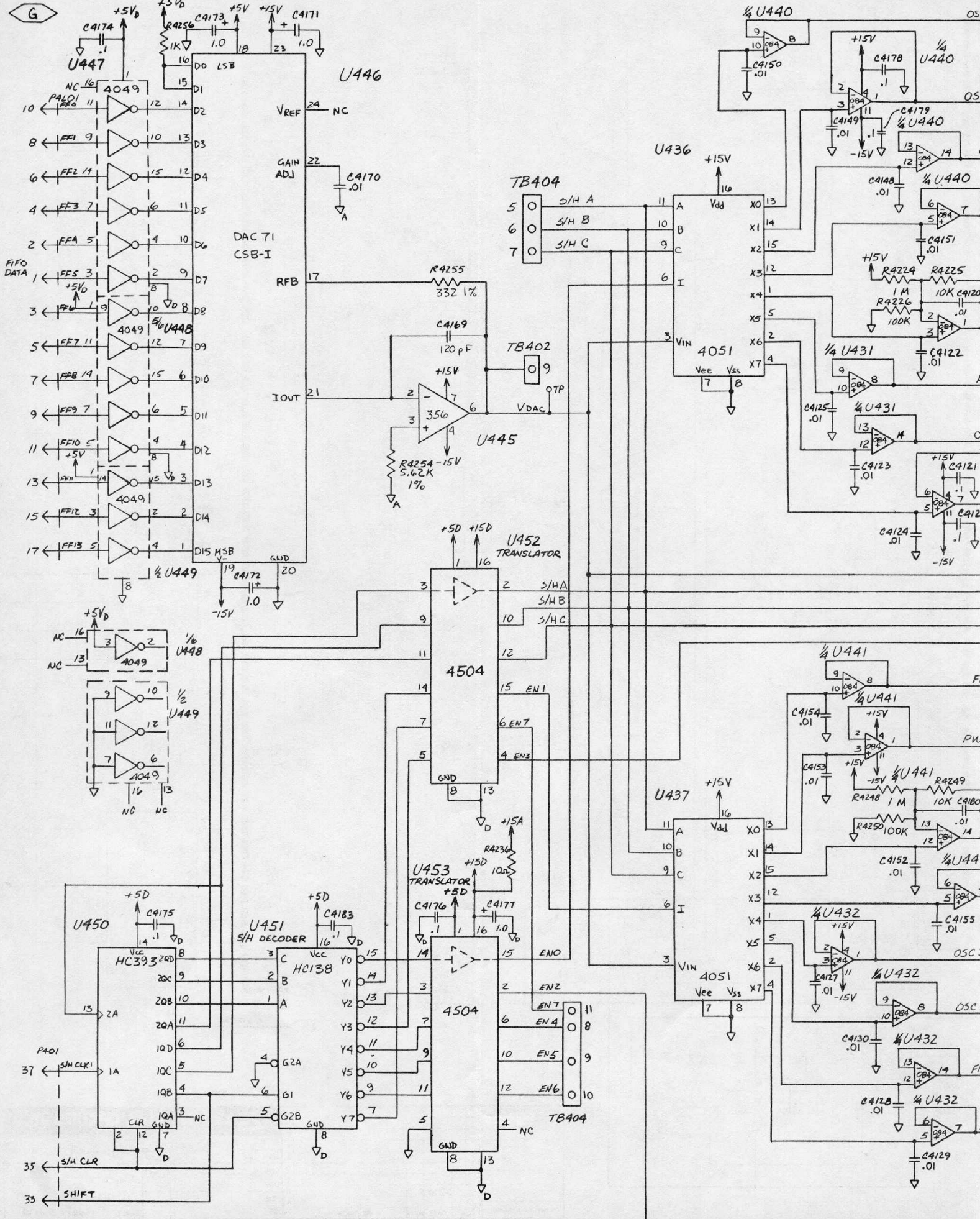


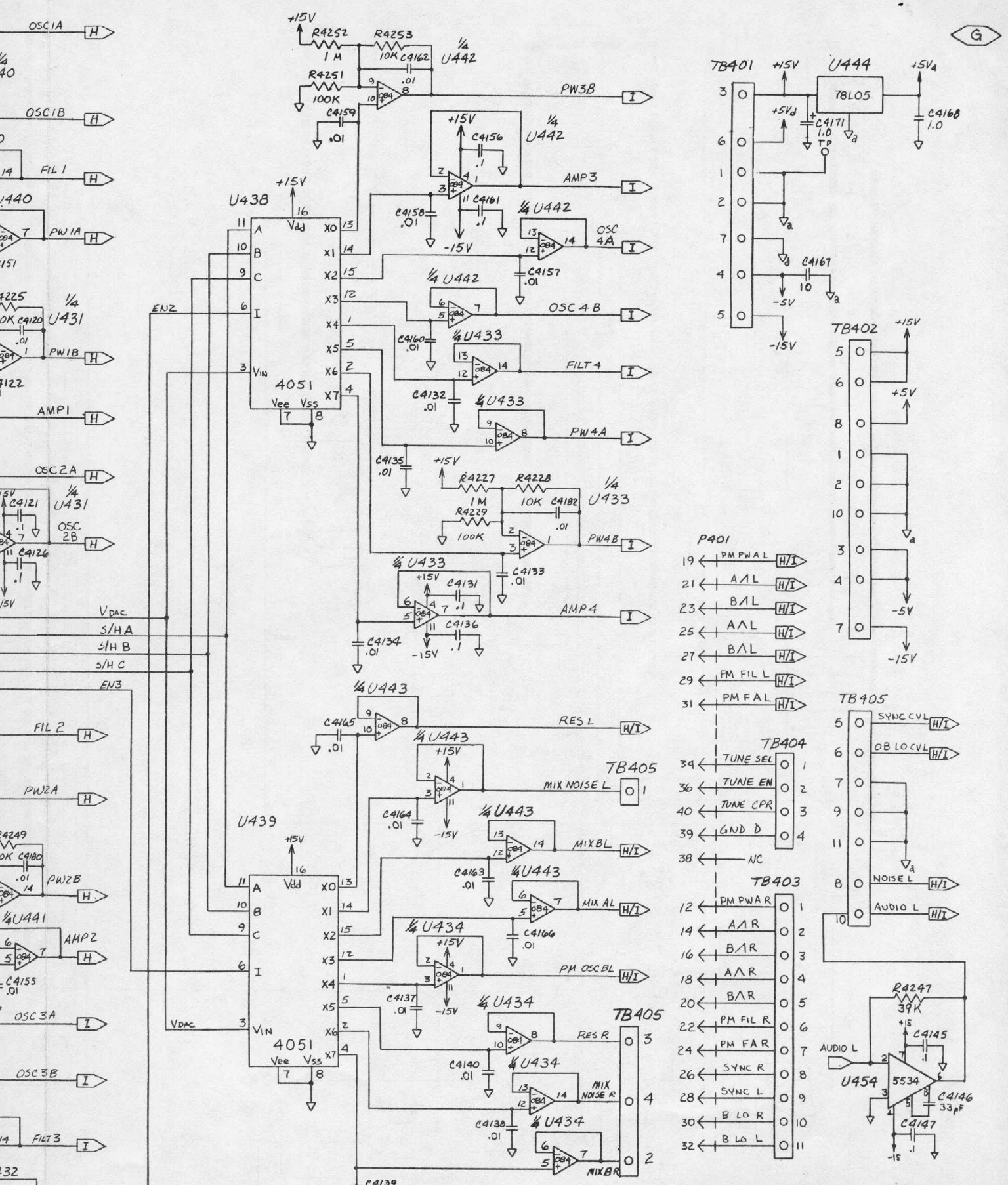
NOTES:  
 ▲ FOR USE ON MODELS WITH L575 (U331)



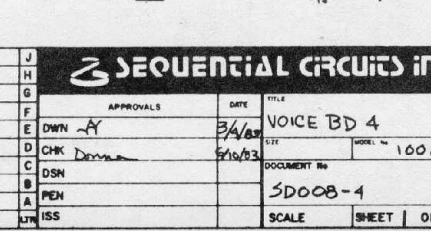
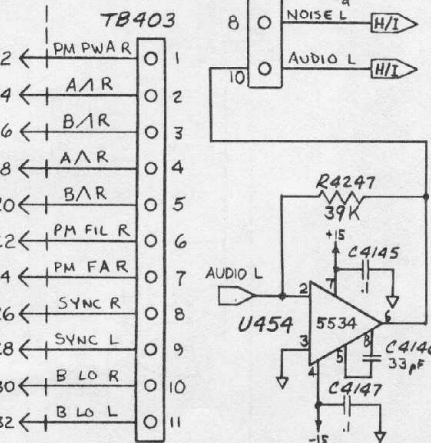
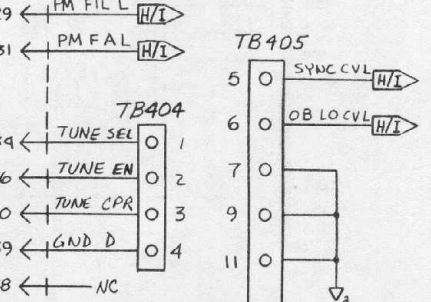
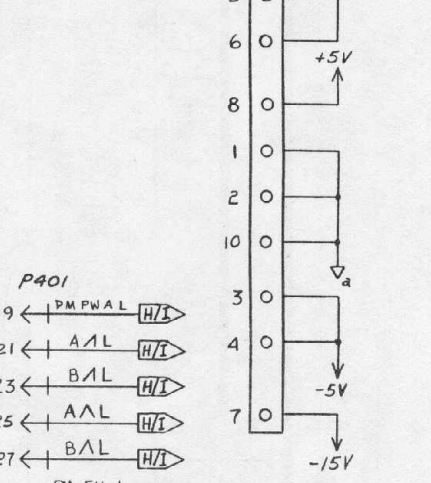
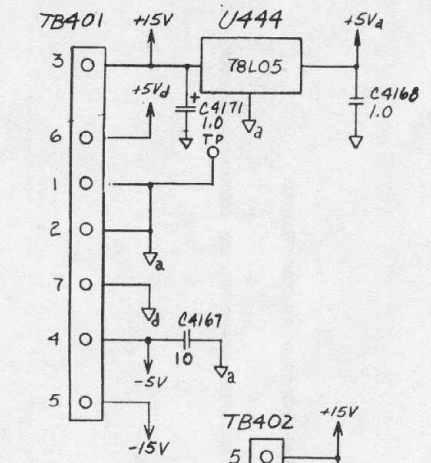








LAST USED: C4183  
R257  
D436



UNLESS OTHERWISE SPECIFIED  
RESISTORS ARE IN OHMS  
TOLERANCES ARE:  
PRACTICES: RESISTORS: 1% 5%  
CAPACITORS: ALL OTHERS: 5%  
MATERIAL: MGR 2

J					
H					
G					
F					
E	DWN	AY	3/4/83		
D	CHK	Duma	5/10/83		
C	DSN				
B	PEN				
A					
LTN	ISS				

DO NOT SCALE DRAWING

DATE: 5/10/83

REVISION: 1

SEQUENTIAL CIRCUITS INC

APPROVALS: [Signature]

DATE: 3/4/83

TITLE: VOICE BD 4

MODEL: 100B

DOCUMENT No: SDOOB-4

REV: B

SCALE: [Blank]

SHEET 1 OF 3























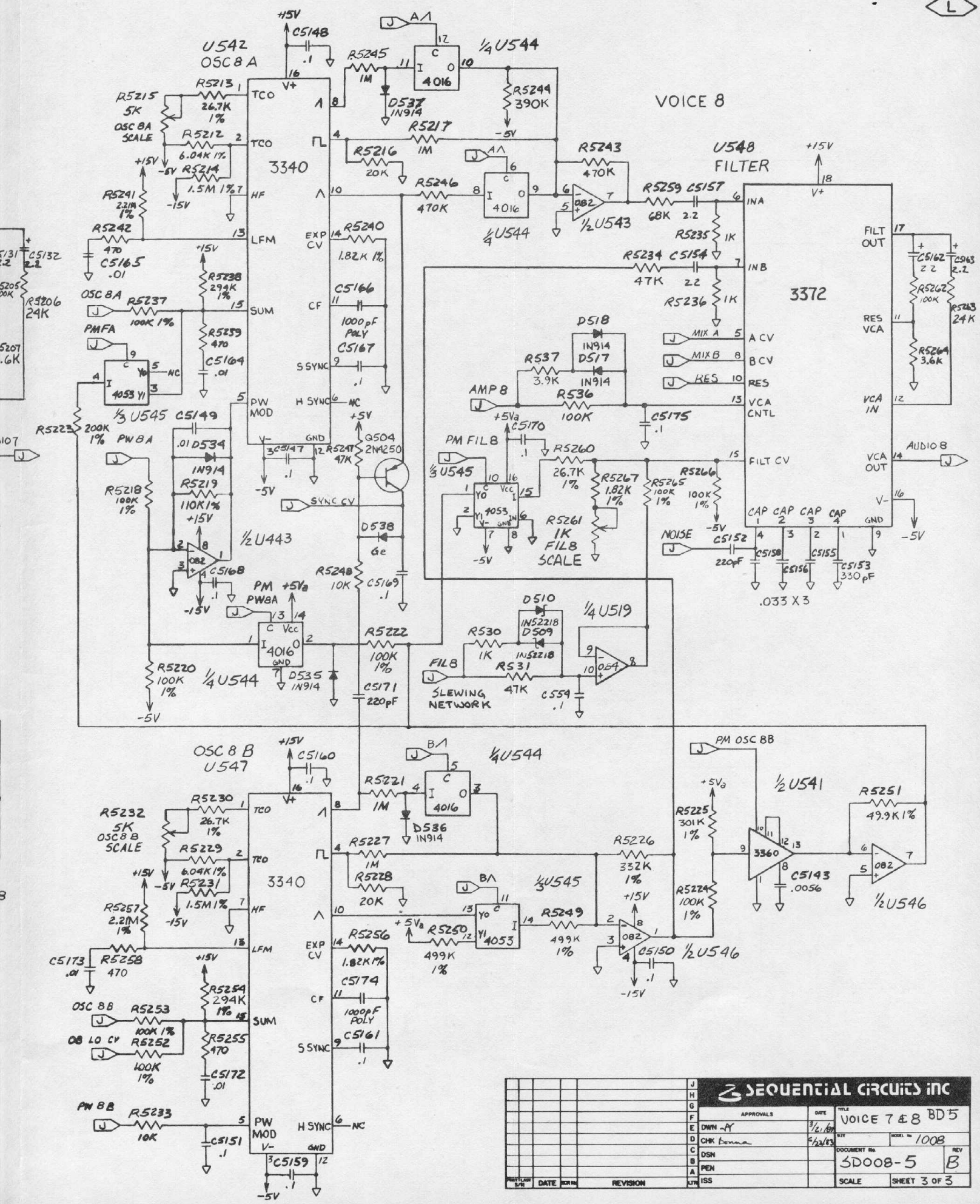






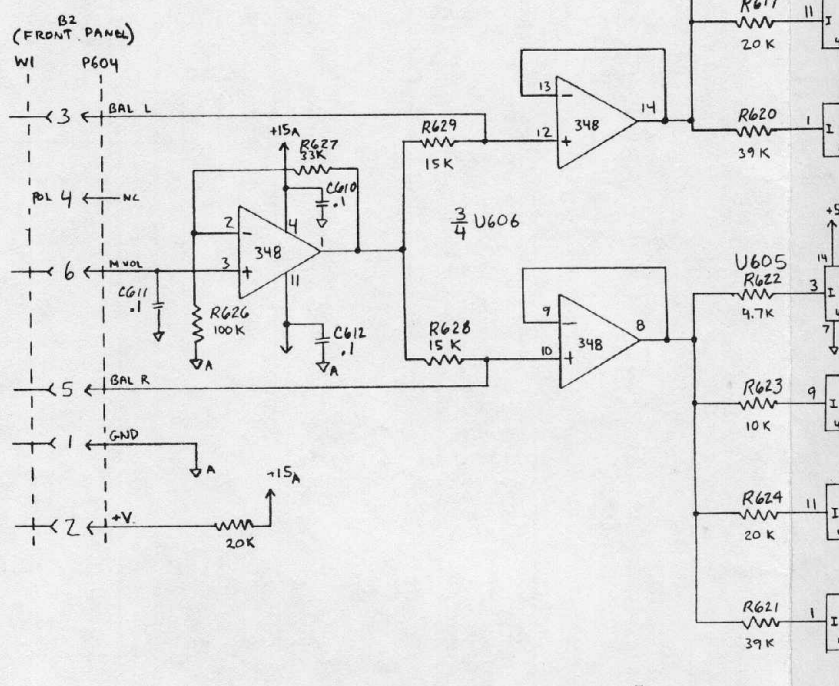
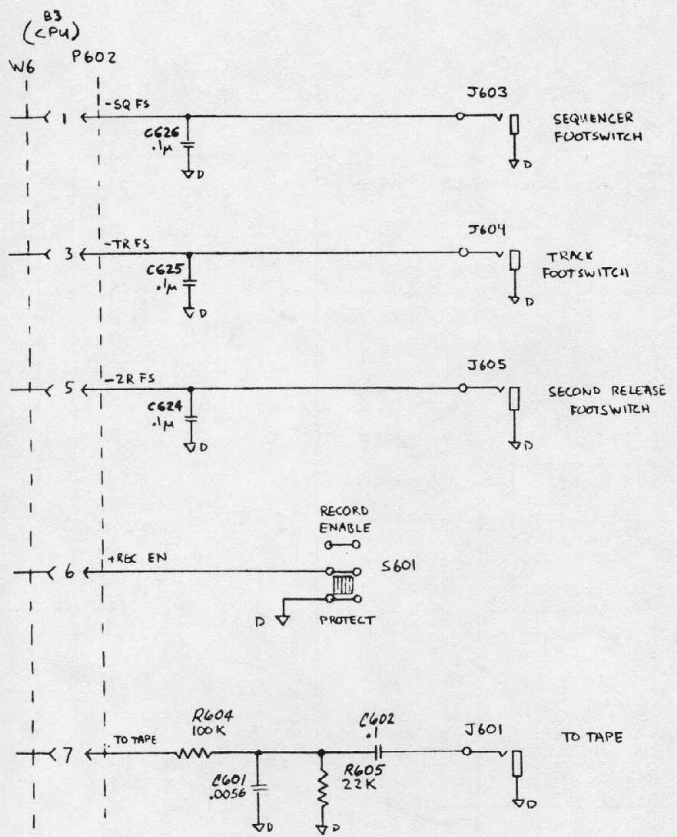




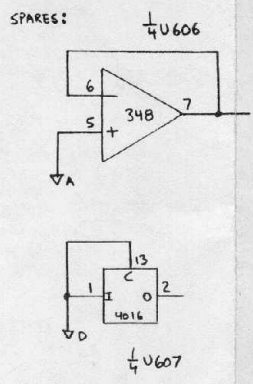
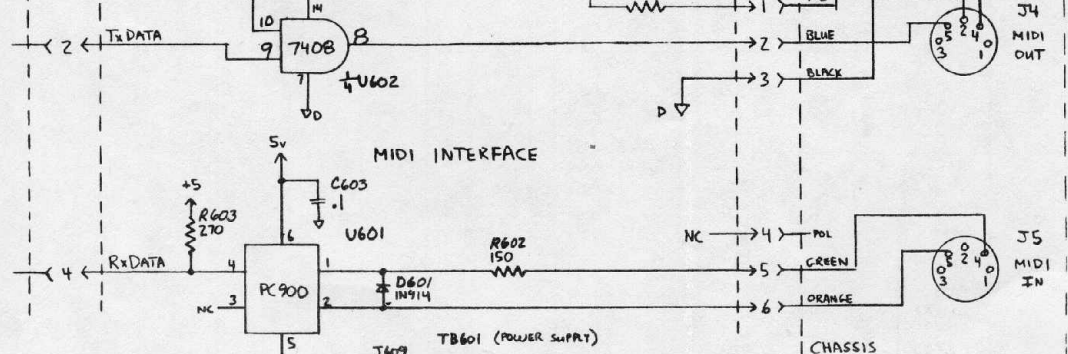
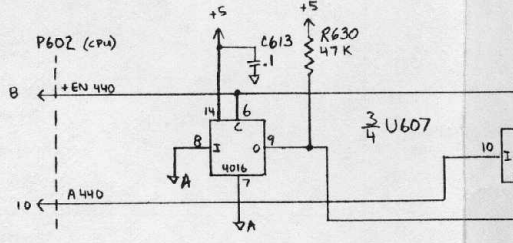
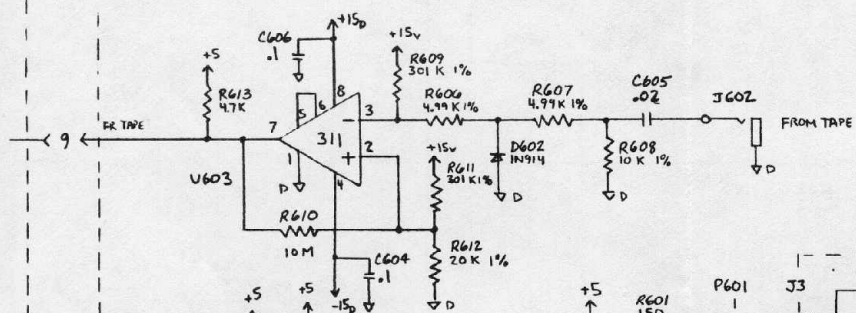


<b>SEQUENTIAL CIRCUITS INC</b>			
APPROVALS	DATE	FILE	
DWYN AY	3/2/68	VOICE 7 & 8 BD 5	
CHK <i>Tomma</i>	5/23/68	SIX	MODEL NO 1008
DSN		DOCUMENT NO	REV
PEN		SD008-5	B
ISS		SCALE	SHEET 3 OF 3

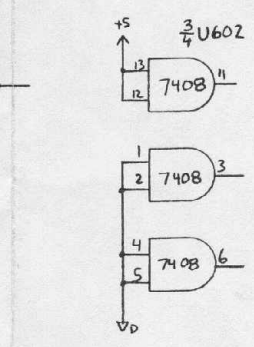
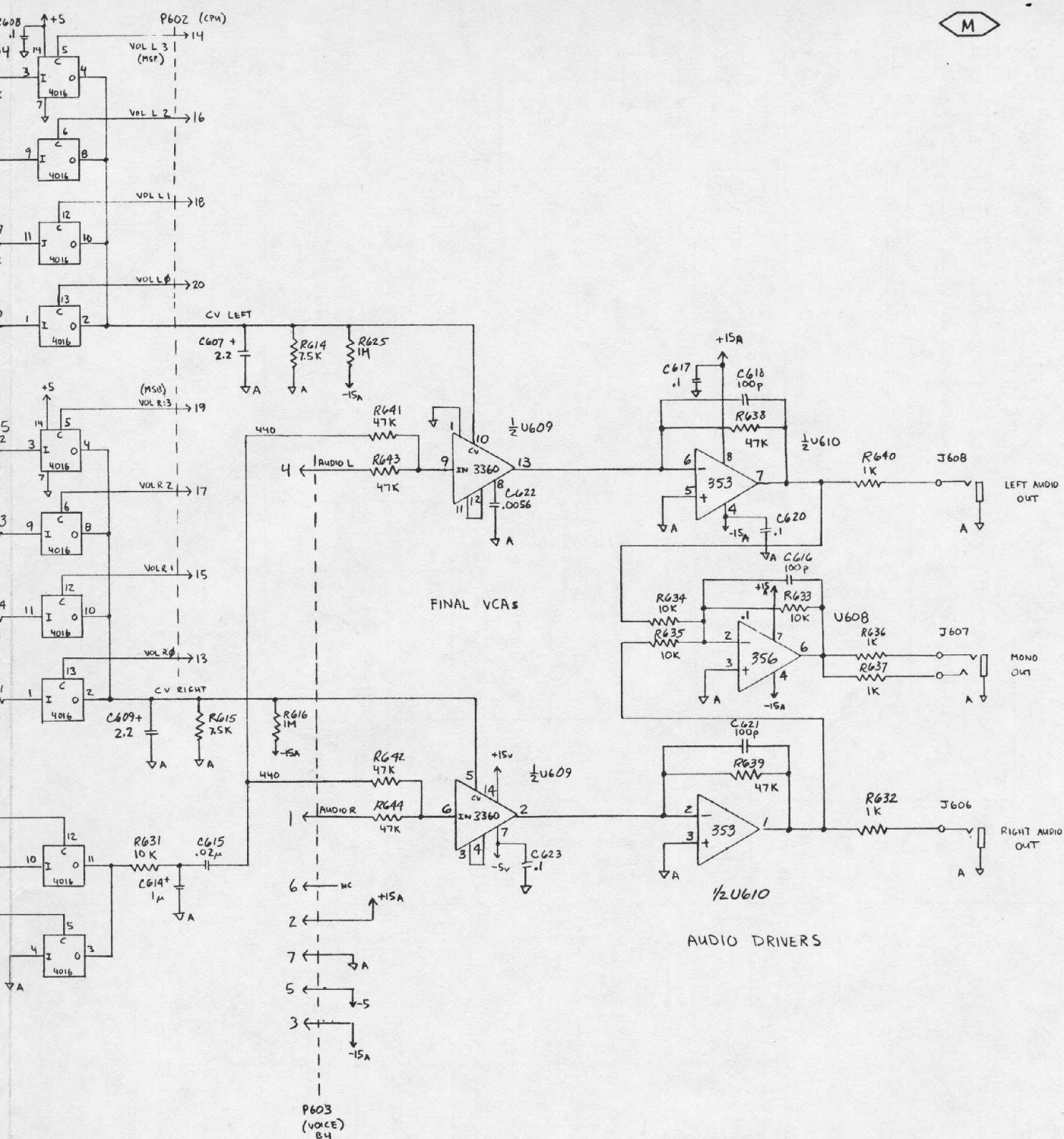
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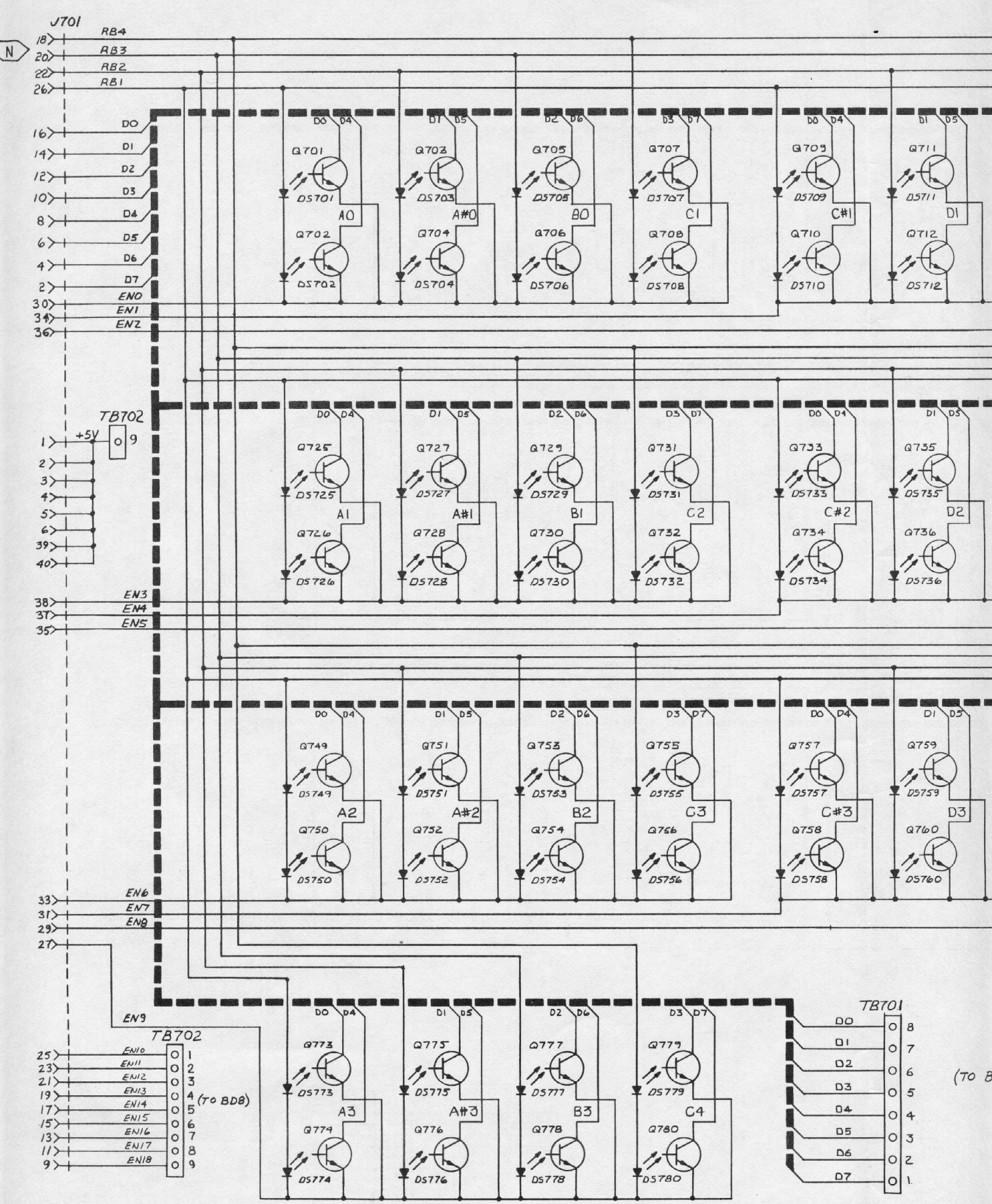
CASSETTE INTERFACE





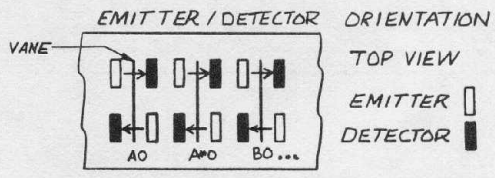
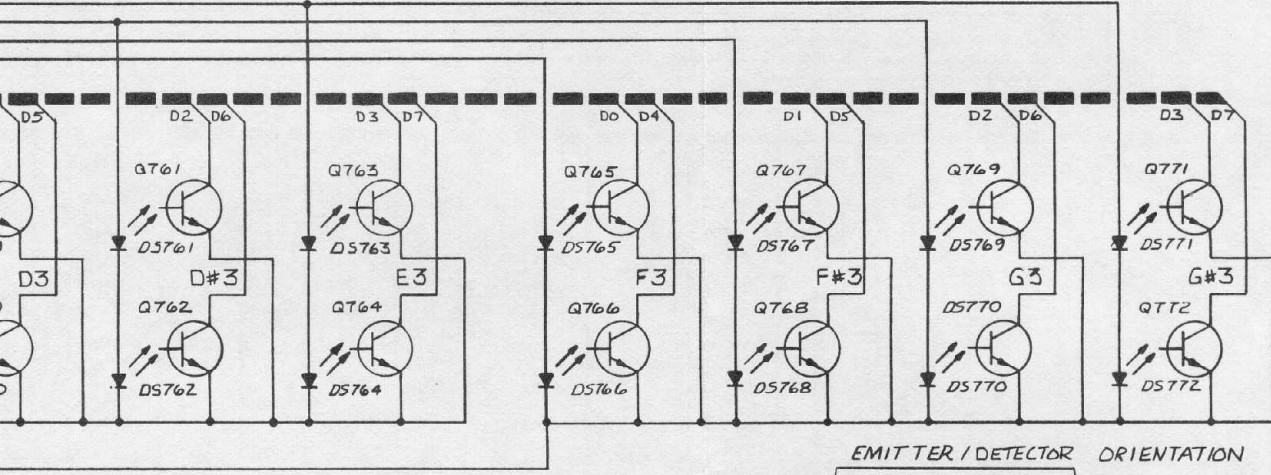
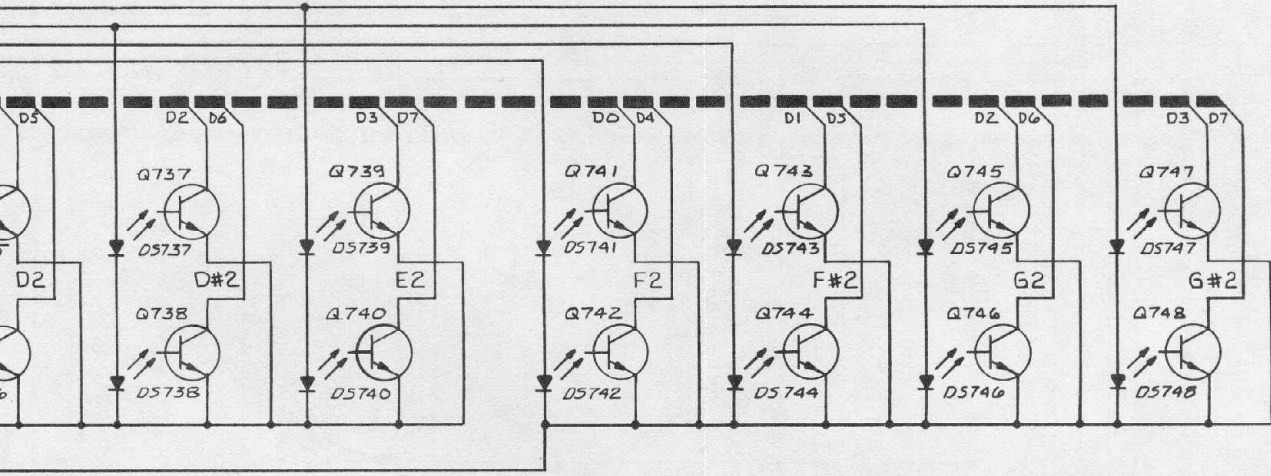
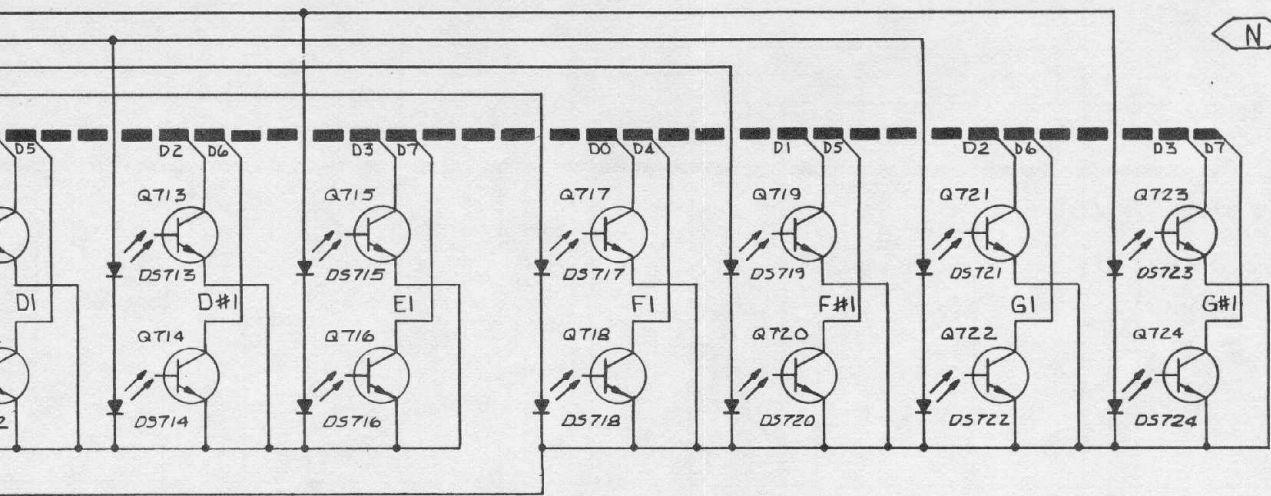


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES		J			DATE		TITLE
MATERIAL		E			APPROVALS	DATE	BOARD 6 SCHEMATIC
FINISH		D	DWN	DAVE	11/6/82	SIZE	MODEL NO
PART / LAST 2/4		C	CHK	DAVE	5/12/83	DOCUMENT NO	1008
DATE		B	DSN			DOCUMENT NO	SD008-6
DATE		A	PEN			REV	B
DATE		ISS	UTR			SCALE	SHEET 1 OF 1





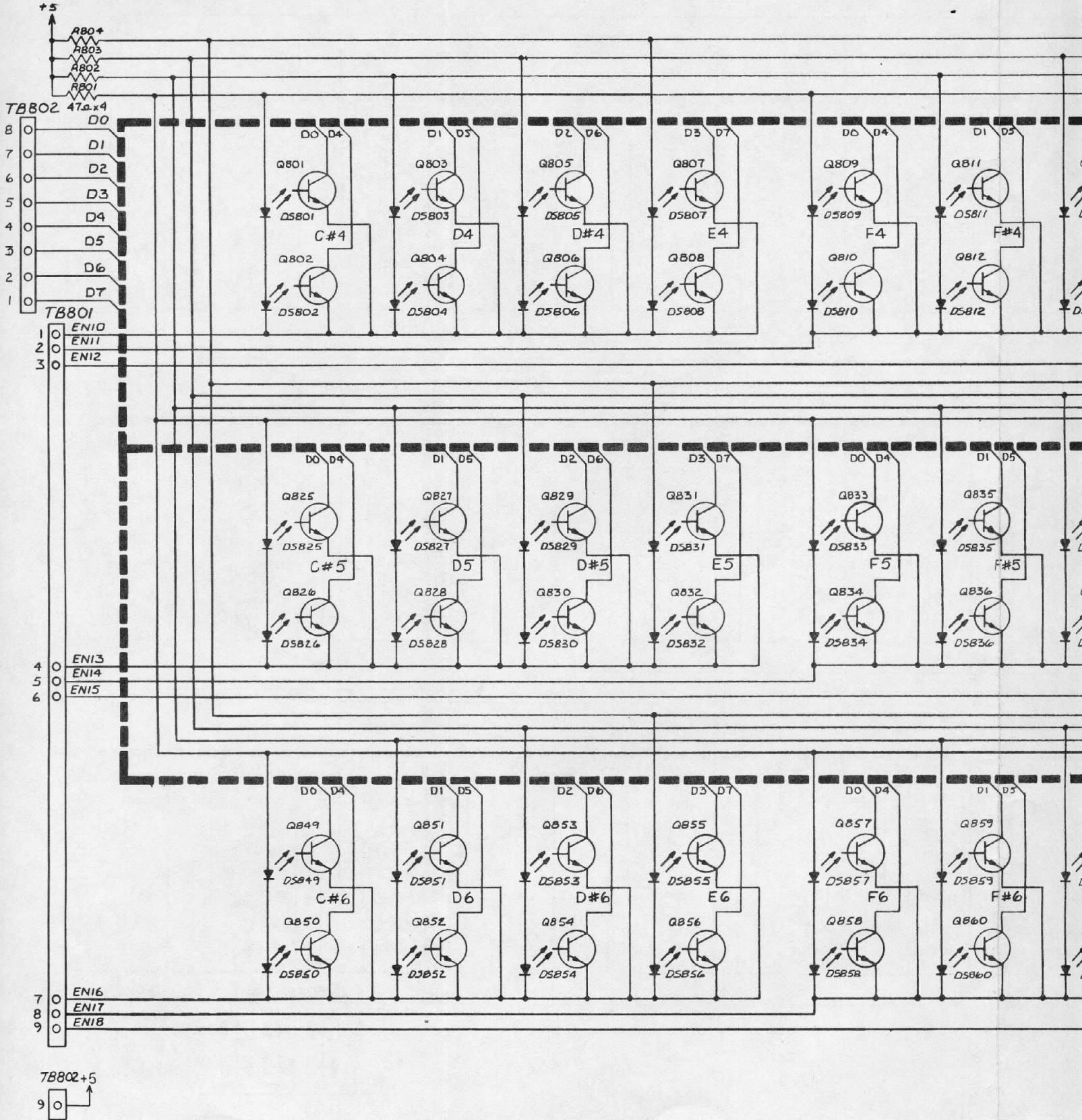
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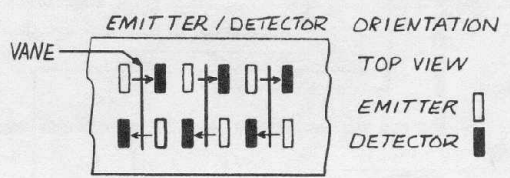
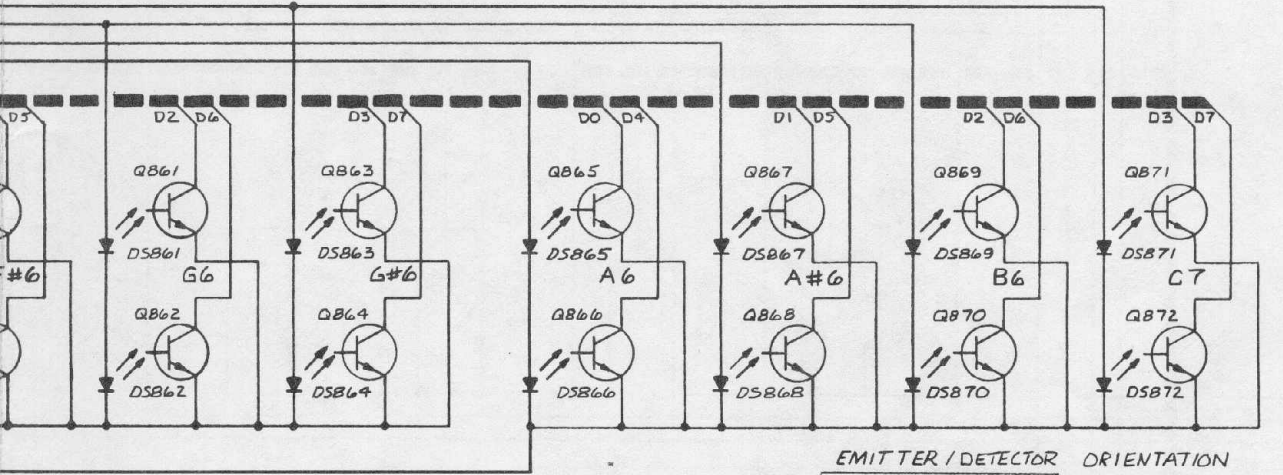
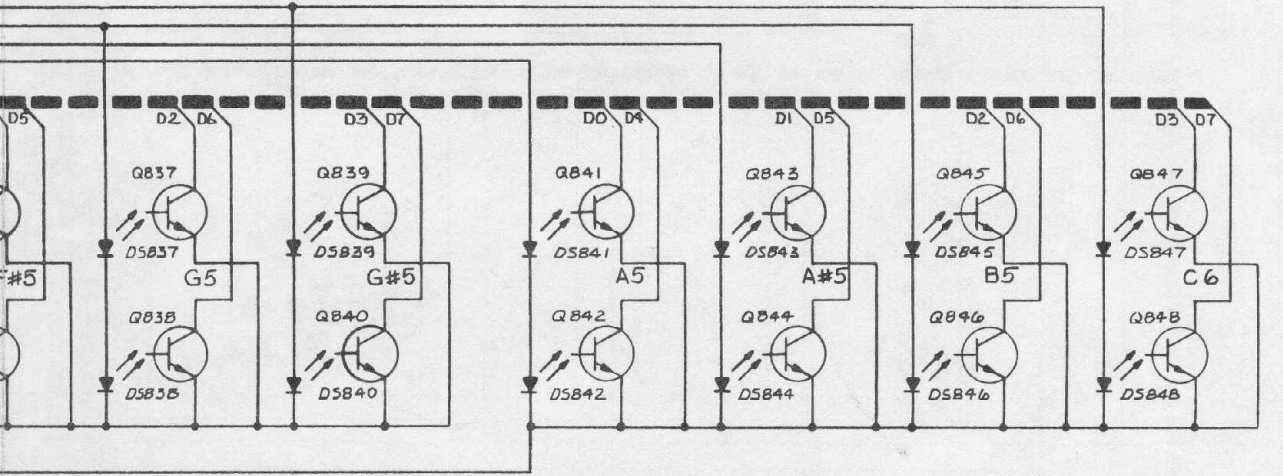
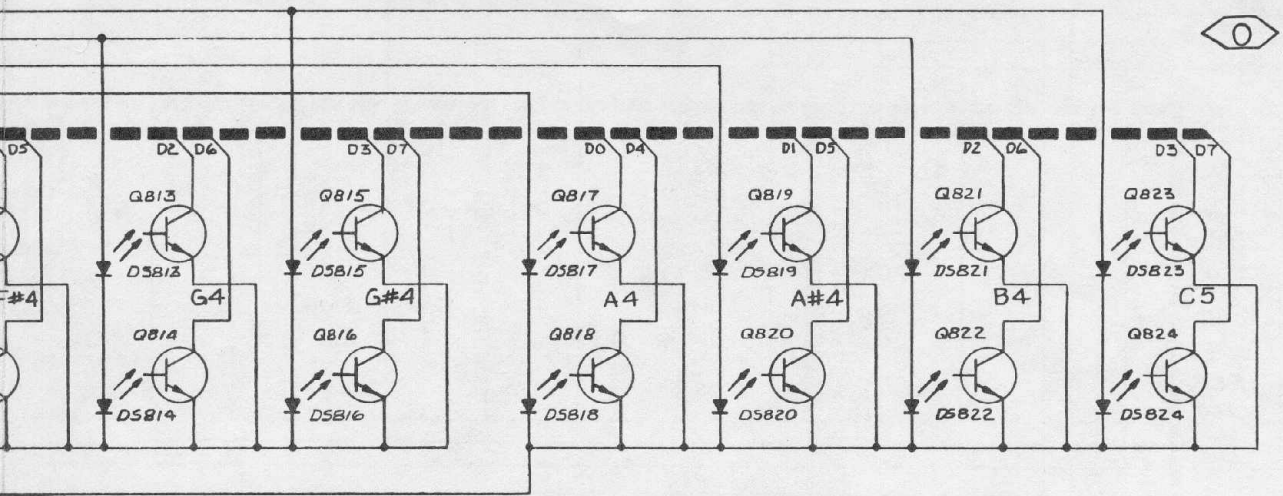
(TO BD 8)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS MILLIS		J	SEQUENTIAL CIRCUITS INC	
MATERIAL		H	APPROVALS	
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REV		F	TITLE	
DO NOT SCALE DRAWING		E	OPTICAL BD 7	
DATE		D	REV	
DATE		C	MODEL NO	
DATE		B	1008	
DATE		A	DOCUMENT NO	
DATE		ISS	3D008-7	
DATE		REV	8	
DATE		REV	SCALE	
DATE		REV	SHEET   OF	

48-283 48-PIN CONNECTOR PIN #5



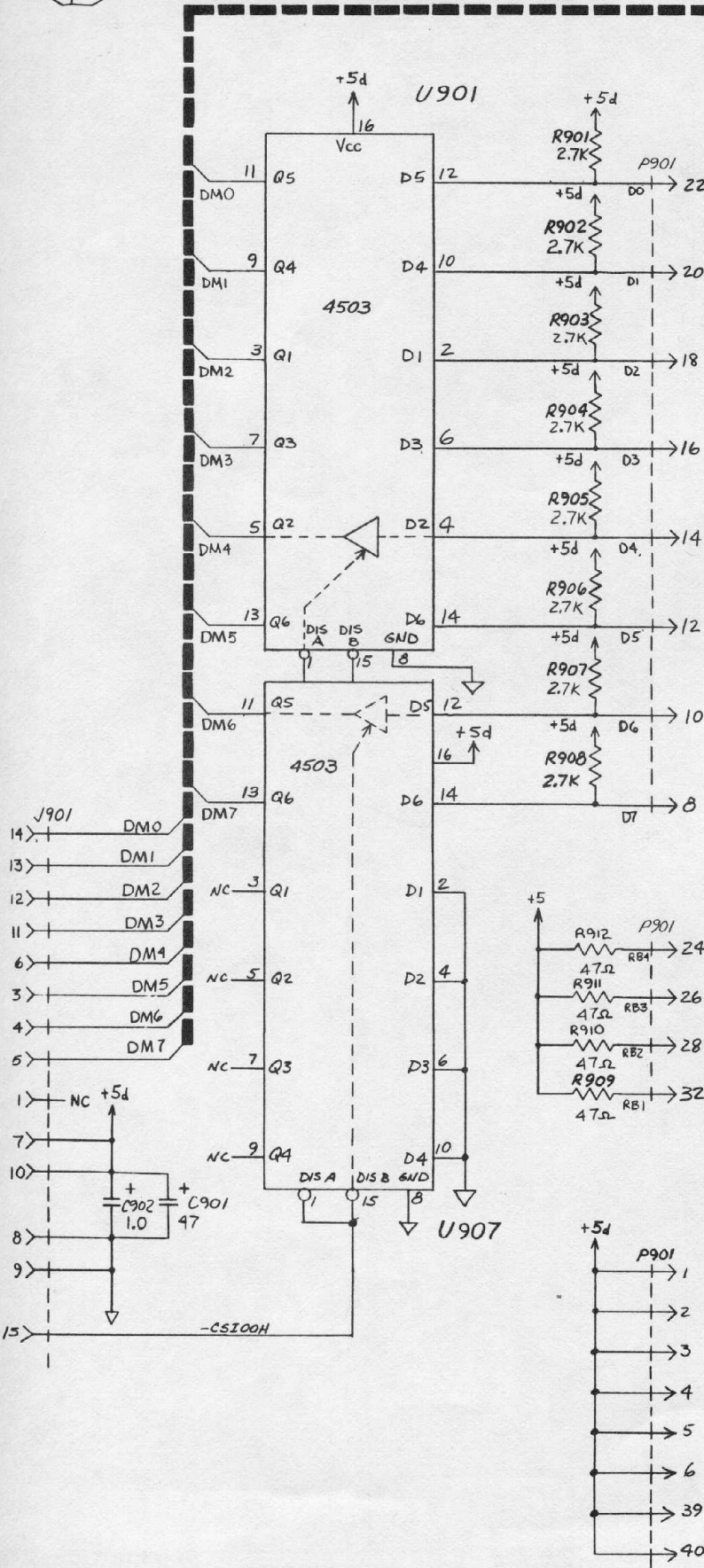




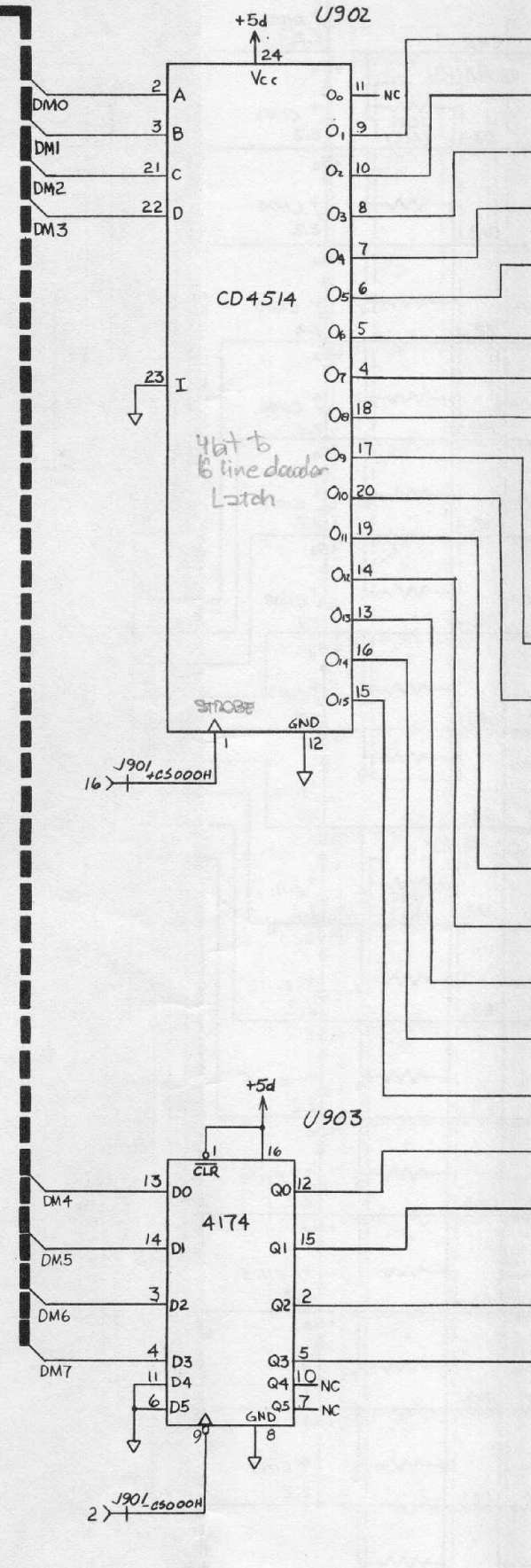
CHECK OFFSHORE DESIGN REVISIONS AND IN NOTES PARTS LIST DATE: 2-3-83 BY: [Signature]		J M O F E C B A L T	APPROVALS DATE 2-3-83 5/9/83	FILE OPTICAL BDB DRAWING NO. 1008 DOCUMENT NO. SD008-8 REV. A
SD NOT SCALE (SHEET) DATE: 2-3-83 REVISION	SCALE SHEET / OF 1	SEQUENTIAL CIRCUITS INC		

P

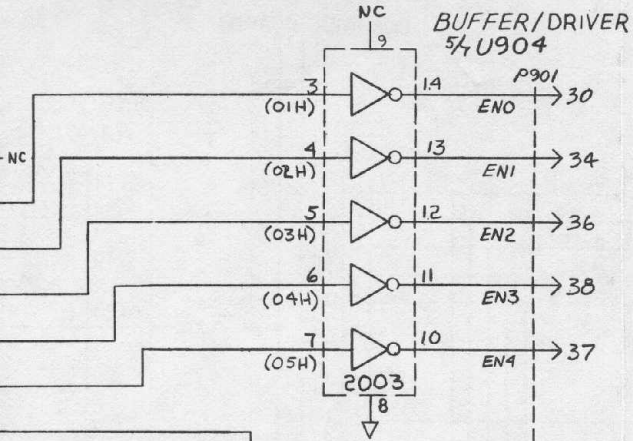
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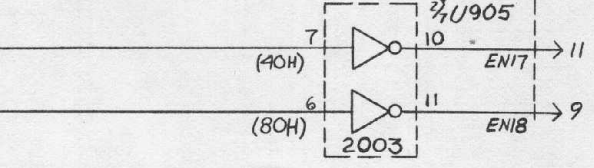
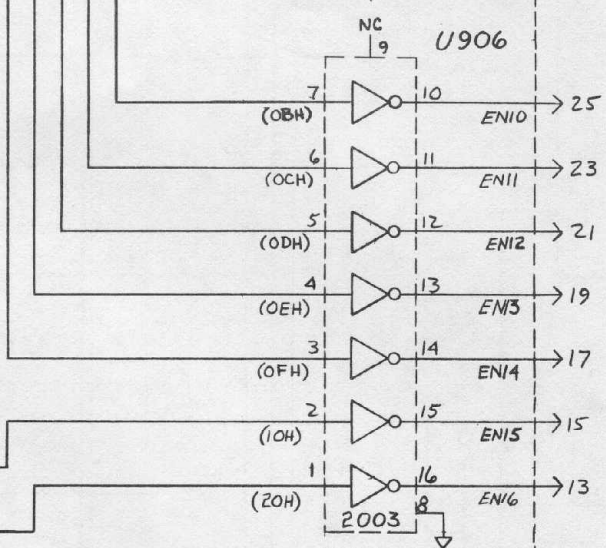
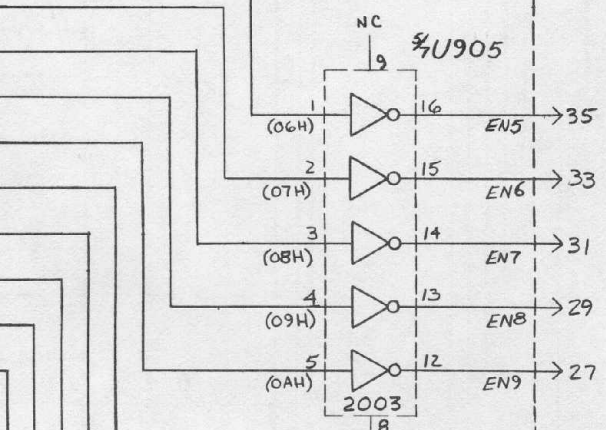
(TO BOARD 7)





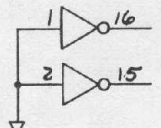


(TO BOARD T)

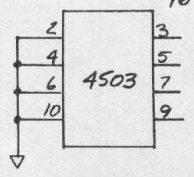


SPARES:

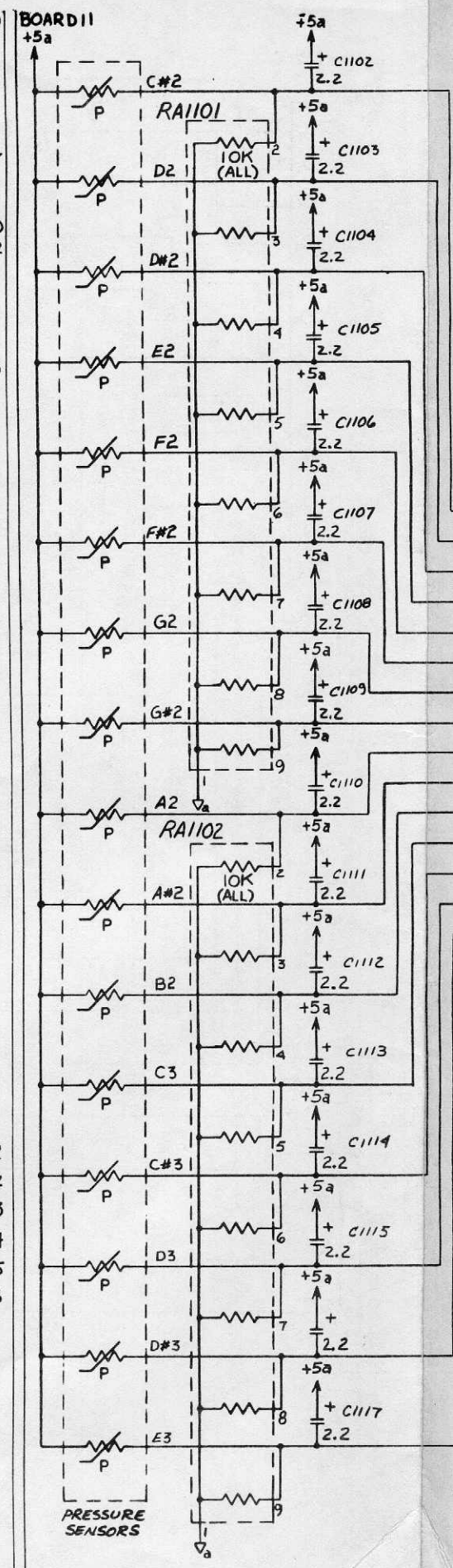
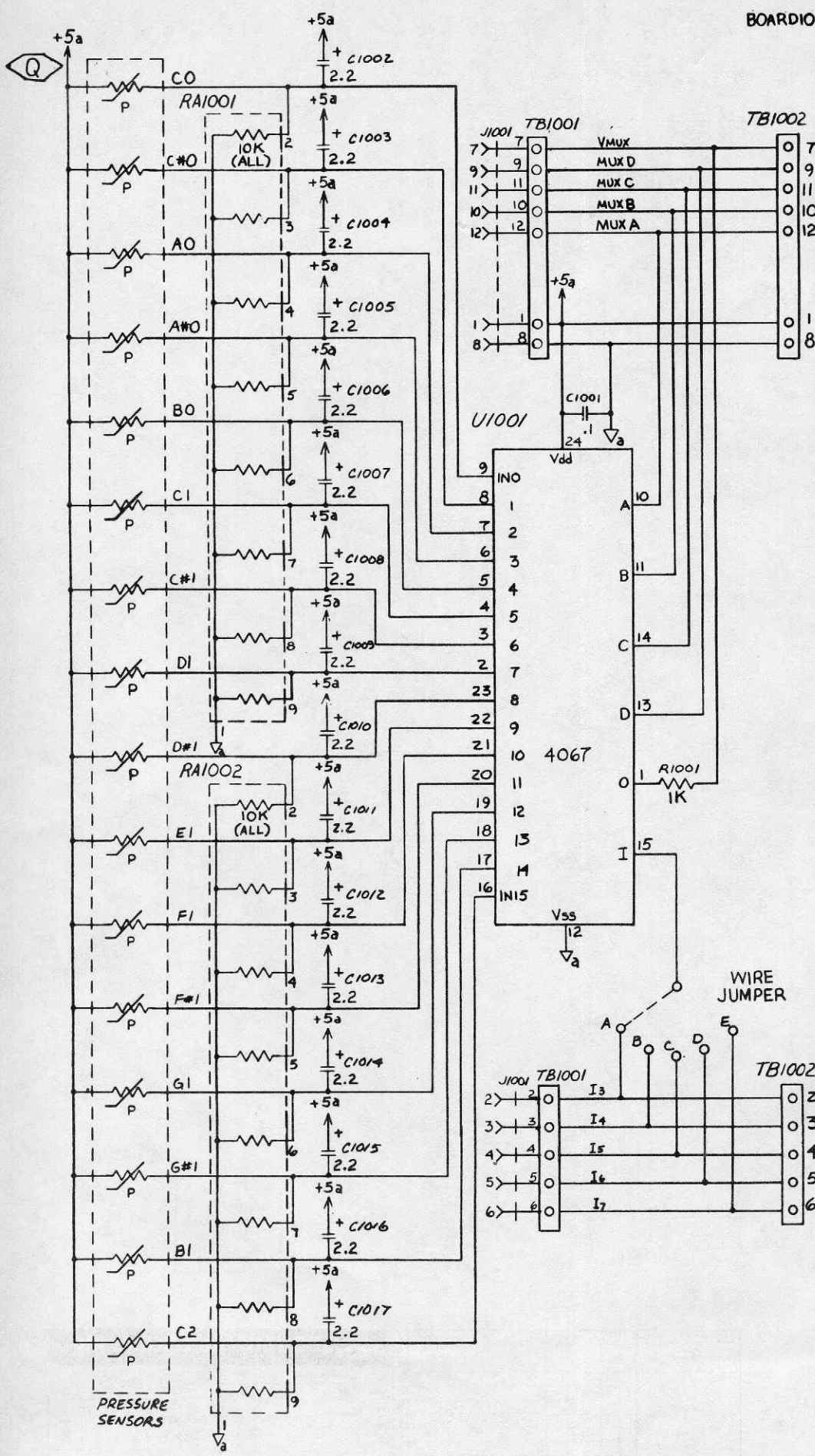
2/7 U904



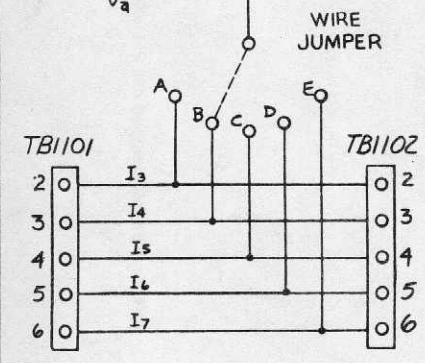
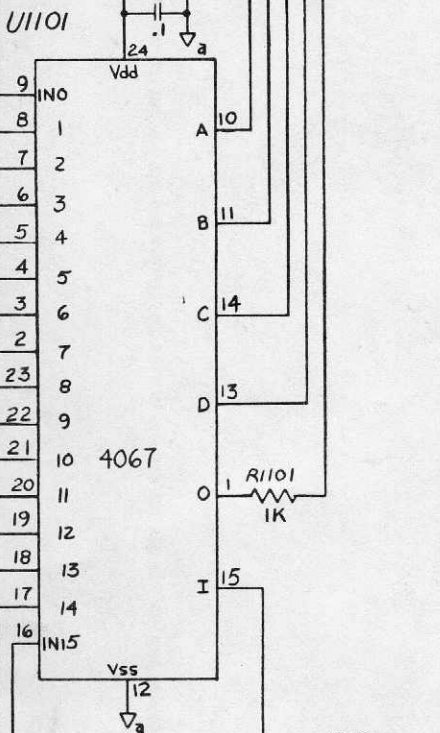
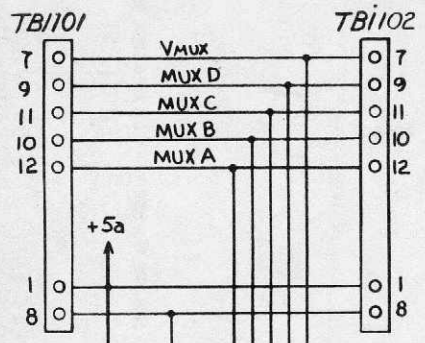
4/6 U907



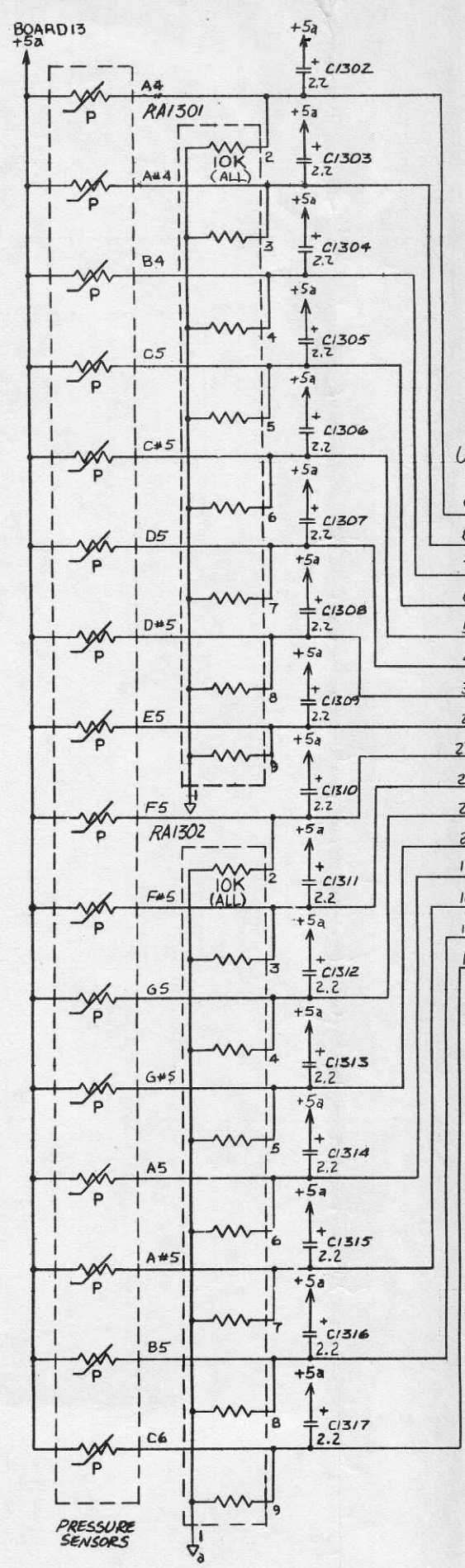
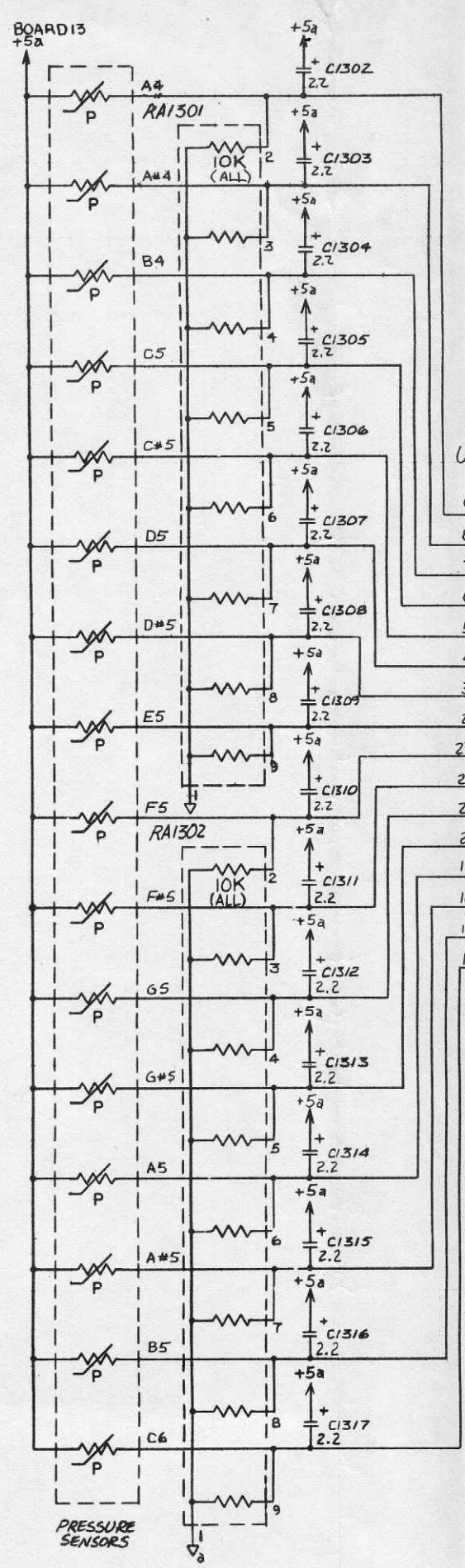
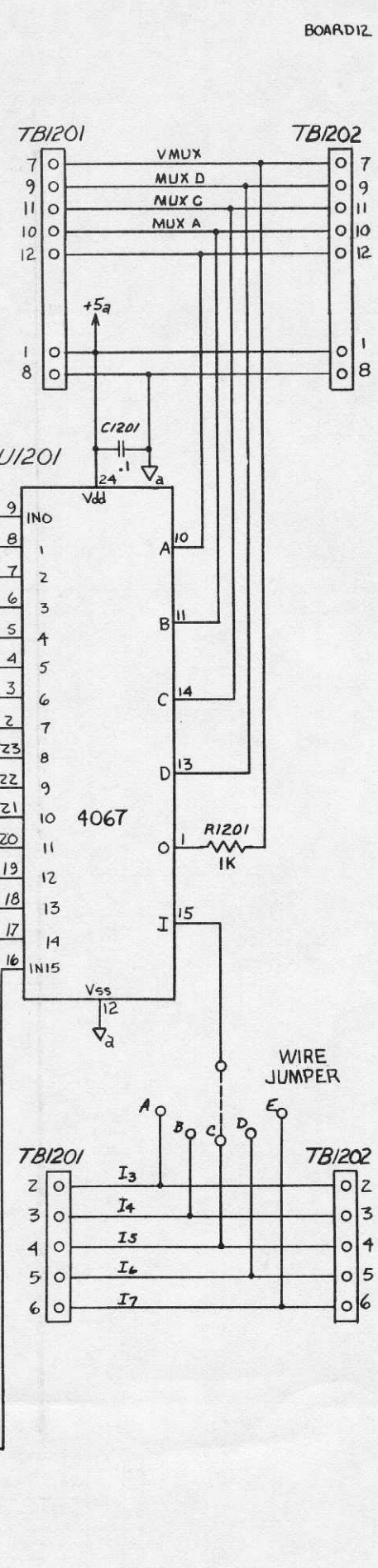
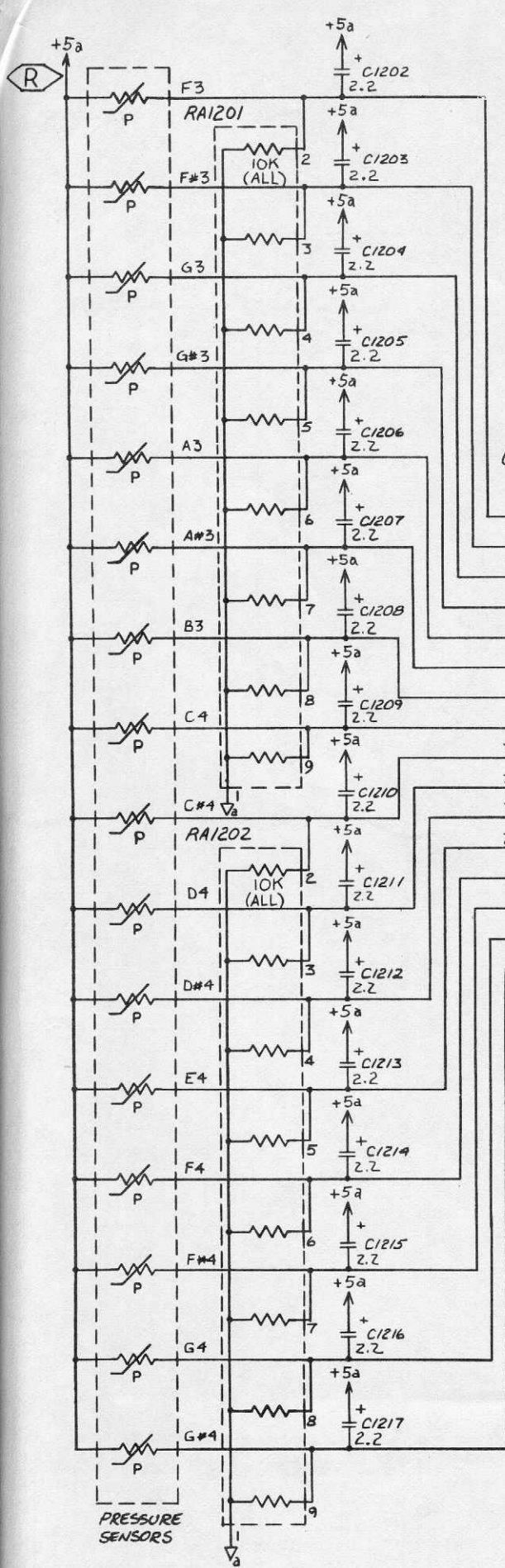
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:		J	SEQUENTIAL CIRCUITS INC	
FRACTIONS DECIMALS ANGLES		H	OPTICAL BD 9	
1 1/2 1/16 1/32 1/64		G	MODEL NO 1008	
MATERIAL:		F	APPROVALS	DATE
FINISH:		E	DWN AY	2/2/83
DO NOT SCALE DRAWING		D	CHK D...	5/1/83
FIRST LAST S/N		C	DSN	DOCUMENT NO
DATE		B	PEN	5D008-9
REV		A	ISS	REV B
REVISION		LTR	SCALE	SHEET 1 OF 1



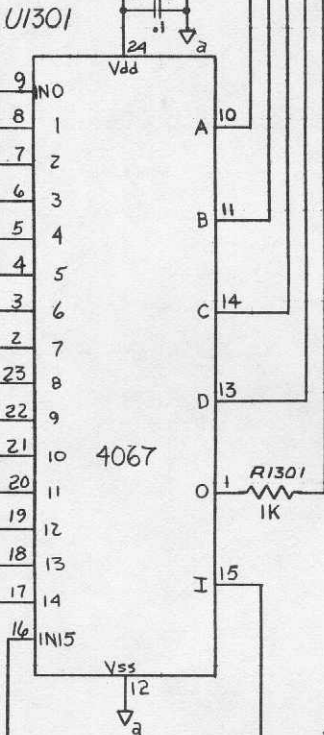
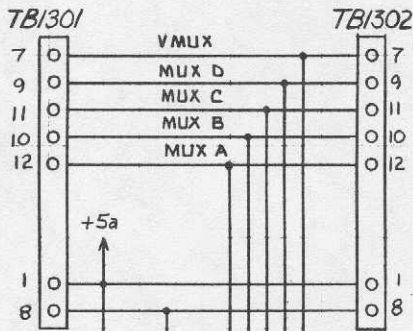




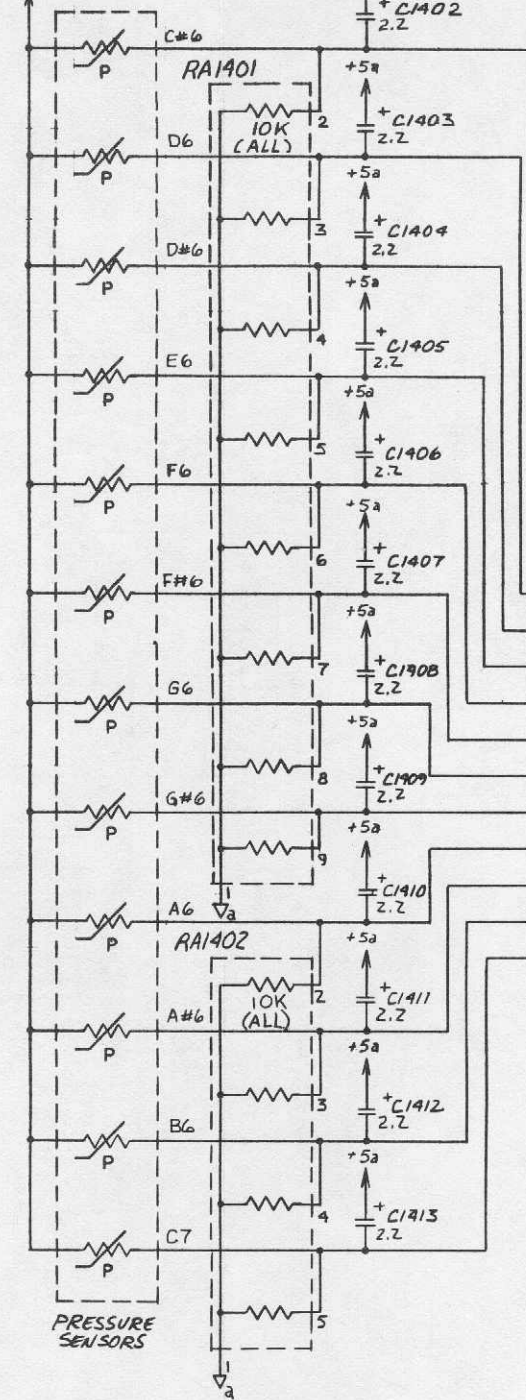
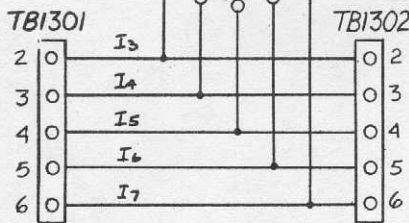
<small>ALLIED ELECTRONIC EQUIPMENT          RECOMMENDED USE IN SERIES          TO PREVENT OVERHEATING</small>		<b>SEQUENTIAL CIRCUITS INC</b>	
<small>REVISIONS</small> 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	DATE 2/1/68	APPROVALS DESIGNED BY CHECKED BY DRAWN BY PARTS BY TESTED BY REVISED BY DATE	SCALE SHEET 1 OF 1
PROJECT NO. 5443		CHANGE JUMPER DESIGNATOR	
DO NOT SCALE DRAWING		PROJECT NO. 1008 DRAWING NO. SD008-10/11 REV. B	





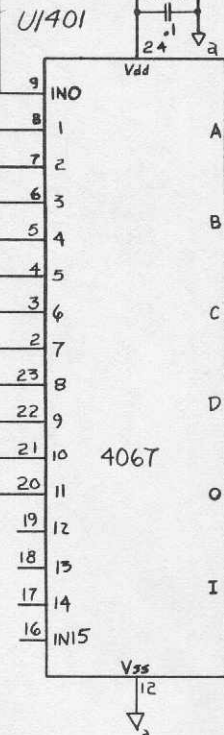
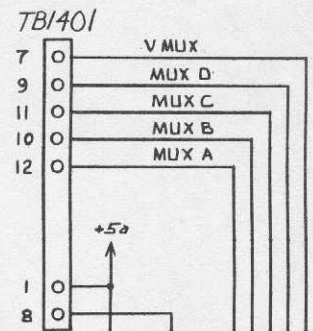
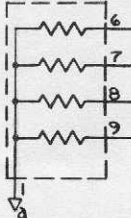


WIRE JUMPER

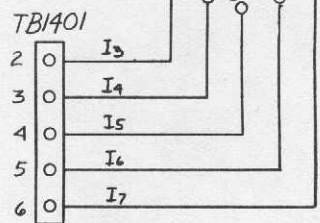


PRESSURE SENSORS

SPARES: RA1402



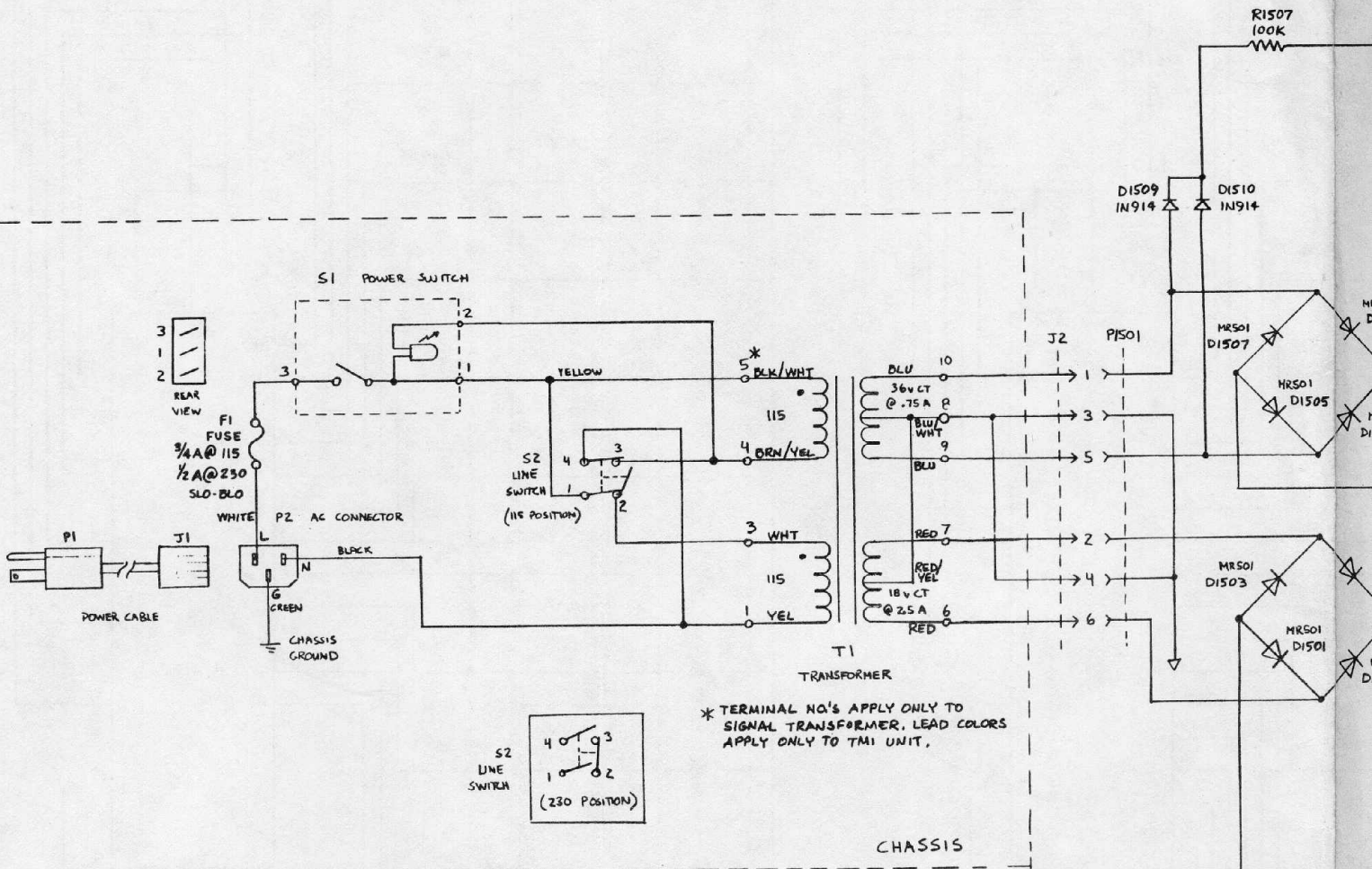
WIRE JUMPER



ALL DIMENSIONS UNLESS SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS USE 16 AS DENOMINATOR DECIMALS USE 2 AS DENOMINATOR DIMENSIONS ARE IN INCHES		J	FILE
DATE:		H	NAME
DRAWN:		G	NO. 1008
CHECKED:		F	REV
DESIGNED:		E	DATE
DATE:		D	SCALE
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CHECKED:		B	OF 1
DESIGNED:		A	
DATE:		L	
DRAWN:		RSS	

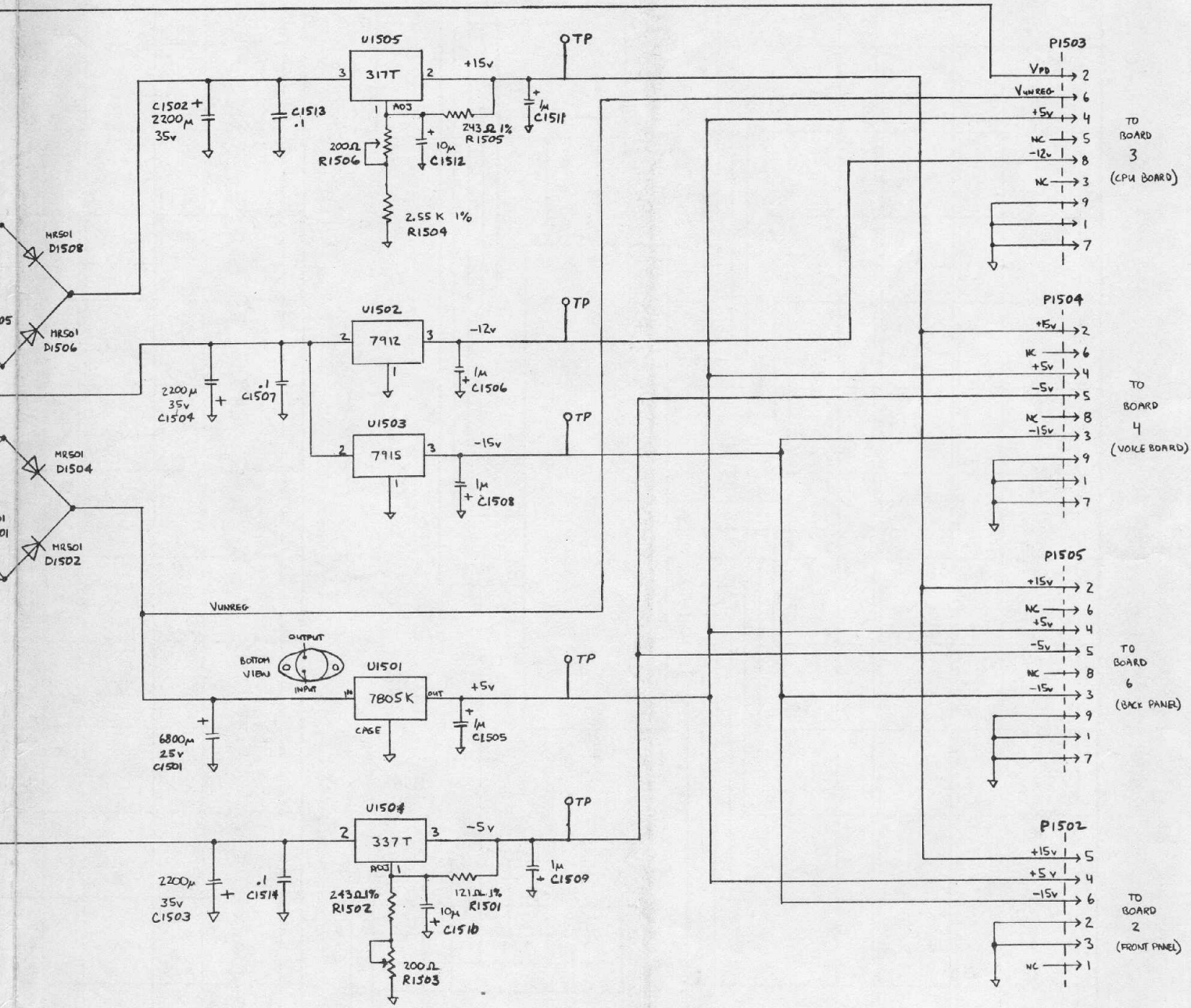
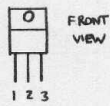
  

APPROVALS:	DATE:	FILE:
DWH -AY	6/10/83	PRESSURE BOARDS
CHK:	DATE:	NO. 1008
DSN:	6/13/83	DOCUMENT NO.
PEN:	CHANGED JUMP DESIGNATIONS	REV:
DATE:	6-9-83	5D008-12/13/14
REVISION:	1	SCALE:
DATE:	6/13/83	SHEET:



POWER SUPPLY





LAST USED :  
C1514  
D1510  
R1507  
P1505  
U1505

<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES 2 10 16</small>		<b>SEQUENTIAL CIRCUITS INC</b>	
<small>DO NOT SCALE DRAWING</small>		<small>APPROVALS</small> E DWH DAVE D CHK <i>Deane</i> C DSN B PEN A LTH ISS	<small>DATE</small> 1/6/82 6/13/82
<small>REVISION</small>		<small>TITLE</small> BOARD 15 SCHEMATIC	<small>MODEL NO.</small> 1008
<small>DATE</small>		<small>DOCUMENT NO.</small> SD 1008-15	<small>REV</small> B
<small>DATE</small>		<small>SCALE</small>	<small>SHEET 1 OF 1</small>

## T8 DIAGNOSTIC PROCEDURES

Notes: Because the normal operating software completely fills the Z80 PROM, a separate PROM is required to run these tests. The Z8002 diagnostics reside in the normal system PROMs. The diagnostics described in this procedure cover most of the digital circuitry in the machine; if a problem has been localized to a general area in hardware, portions of this procedure may be skipped.

### Z80 TESTS

Notes: Z80 tests are selected using program select buttons 1 through 5. The current test number is displayed on the right program LED display.

1. Install Z80 diagnostic PROM (DIAGT8) in IC22 socket.
2. Disable Z8002 by shorting BUSREQ test point to ground with a clip lead.
3. Power-up the machine. The Z80 is now in a loop waiting for a program select button to indicate the desired test. Execute tests 1 through 5.
4. Troubleshoot any test failures.

### Z8002 TESTS

Notes: The diagnostic software is accessed by momentarily grounding the -NMI test point (short duration less than one second; this pin is debounced in software). The program advances to the next test routine each time the pin is shorted (allow 5 seconds for the next test to begin). Disconnect the audio monitor system from the T8 before running these tests.

1. Remove the ground clip from -BUSREQ if present. Disable the Z80 using the Z80 -BUSREQ pin.
2. Start test number 1 using -NMI.
3. When test two is correctly executing, remove the Z80 -BUSREQ ground clip and select test number 4 of the Z80 diagnostics. Z80 and Z8002 common ram tests are now running simultaneously, which is a 100% test of common ram circuitry. If both tests pass, disable the Z80 again and proceed with Z8002 tests 3-17.
4. Troubleshoot any test failures,



## Z80 DIAGNOSTIC TEST DESCRIPTIONS

### TEST 1: I/O PORT TEST

This test alternately writes 55H (01010101) and AAH (10101010) to all output ports. At the same time, all input ports are being read. This test verifies all chip-select decoding circuitry.

### TEST 2: LED TEST

All LEDs on the front panel are lit in sequence.

### TEST 3: RAM TEST

A memory test is performed on Scratch Pad RAM, Program RAM, and Sequencer RAM. This test is destructive so programs and sequences should be saved to tape before executing the test. The results of the test are displayed on the PROGRAM SELECT LEDs as follows:

PROG SEL LED 1 = U312 failed RAM test.  
PROG SEL LED 2 = U316 failed RAM test.  
PROG SEL LED 3 = U311 failed RAM test.  
PROG SEL LED 4 = U313 failed RAM test.  
PROG SEL LED 5 = U317 failed RAM test.

No LEDs on except test # indicates RAM test passed.

### TEST 4: COMMON RAM TEST

A memory test is performed on the lower 1k address space of Common RAM. The results are displayed on the PROGRAM SELECT LEDs according to the following format:

PROG SEL LED 1 = U335 failed RAM test.  
PROG SEL LED 2 = U337 failed RAM test.

No LEDs on except test # indicates RAM test passed.

### TEST 5: POT AND PRESSURE SENSOR TEST

Performs ADC of all pots (except Master Volume and Balance), Pitch Wheel, Mod Wheel, and all pressure sensors. The 8 bit sum of all conversion results is displayed in hex on the right program display. With all pots initialized to zero, each pot can be rotated to check that it covers the full range from 00H to FFH. The pressure sensors are tested in the same way, although it is normal for some sensors to not quite reach FFH.

## Z8002 DIAGNOSTIC TEST DESCRIPTIONS

### TEST 1: uOUT TOGGLE

This test requires a minimal amount of hardware to pass. It verifies correct PROM access, data and address bus integrity, correct power supplies, and other minimum Z8002 operating conditions.

Pass is indicated by a continuous pulse train on the uOUT test point.

### TEST 2: COMMON RAM

This test checks the top half of common ram and associated arbitration logic. It may be run simultaneously with the Z80 common ram test, which accesses the lower half of common ram. In operation, the test writes the upper 1k of ram with a sequence of numbers. The sequence is then read and checked for errors. This cycle will continue to repeat unless an error is found.

Pass is indicated by a continuous train of widely-spaced pulses. The fail loop produces a high-frequency square wave.

### TEST 3: DAC TEST

This test verifies interrupt, FIFO, and DAC hardware. An ascending sequence of numbers is repeatedly output to the FIFO, resulting in a ramp waveform at the DAC output buffer. All bits are used, and any hardware problems affecting the data will appear as nonlinearity in the ramp waveform. Problems with the low order bits may not be visible; these bits can be checked with tests 4-17.

### TESTS 4-17: BIT TESTS

Each of these tests outputs a constant value to the DAC, which will appear on all sample holds. Starting with the DAC MSB, there is only one bit set per test. As tests are advanced, each bit value can be measured with a DVM if desired.

Note: Shorting -NMI after the last bit test will initiate test number 1. To execute the normal operating software, the power must be switched off.